Realization of ladder *EndCap* electronics for the ALICE ITS SSD.

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Abstract

In this paper the tests and realization of the control electronics for the front-end of the ALICE **S**ilicon **S**trip **D**etector (SSD) is described. The front-end hybrids are built with the HAL25 (LEPSI [1]) chip. The controls are placed at both ends of the detector ladders in the *EndCap* Modules.

The modules contain power regulators, LVDS repeaters, several JTAG bus controlled functions to monitor and control the readout functions of the detector, and buffers for the analogue signals. The system uses AC-coupling for *all* signals for the double-sided detector readout.
Two 0.25µm CMOS radiation tolerant ASIC's are designed for this module. They are tested on wafer and later bonded on kapton PCB's with an aluminium carrier. Results of wafer tests, prototype board tests (and set-ups) are described. The final design- and production tests using JTAG Boundary Scan Test is also explained.

I. Introduction

The ALICE Inner Tracker System is composed out of 6 layers, 2 Pixel-, 2 Silicon Drift-, and two Silicon Strip Detectors layers. The realization of the control-electronics for the SSD, the *EndCap* Module, will be described.

The SSD consists of two layers of carbon fiber ladders on which the detector modules are placed. They are based on Double Sided Silicon Strip Detectors and these are readout by the HAL25 front-end chip that is developed by LEPSI in Strasbourg [1].

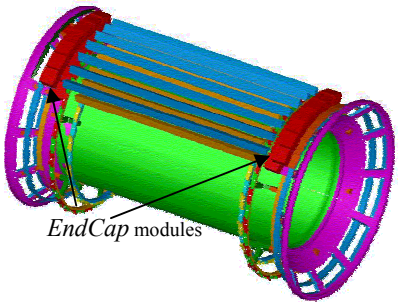

Figure 1: ALICE ITS with SSD

The detector modules with their front-end chips are connected to the DAQ- & Control system (FEROM [2]) by means of the *EndCap* Modules. These are placed at both ends of each ladder, inside the detector volume (fig. 1 & 2). The available space for one *EndCap* is ~7x7x5 cm, and it must house 9 PCB's to control 28 front-end hybrids. The limited available space and the temperature constraints of the detectors (and environment) require a low power design with good heat transfer to the cooling system.

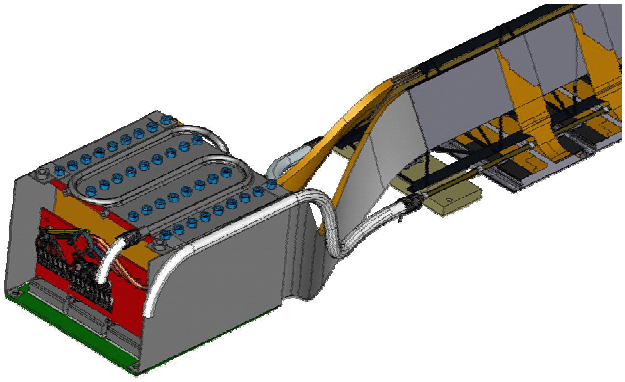

Figure 2: EndCap with ladder connected with kapton cables.

In the ALICE experiment the electronics must be able to survive Single Event Effects (SEE) and about 50krad total ionizing dose. Therefore the front-end chip and the electronics inside the *EndCap* must be protected against latch-up. Radiation tolerant design techniques [3] must protect the system against malfunctions during its life time.

Due to the use of double-sided detectors, the readout electronics on both sides operate at different potentials. To avoid data acquisition- and control electronics to operate at these bias potentials, all signals are AC coupled to the corresponding voltage level.

The control functions for the front-end and the *EndCap*, like power regulation and latch-up protection, signal coupling, readout control etc., are integrated in an ASIC, the ALCAPONE.

The analogue signals from the front-end must be buffered. For the readout of the two detector sides an analogue multiplexer is required. These two functions are integrated in a second ASIC, the ALABUF. This chip is produced and tested.

The Front-end electronics is controlled via the serial JTAG (IEEE 1149.1) bus. This bus is also used to monitor and control the *EndCap* functions. Errors like latch-up and high detector current can be monitored, and appropriate action can then be taken. Disabled or broken front-end chips, hybrids, and *EndCap* PCB's can be bypassed and this information is available for the DAQ system. During the production phase, the JTAG bus is used for its intended purpose; connectivity test of assembled PCB's.

Both IC's are designed in a commercial CMOS technology (0.25um) with radiation tolerant design techniques. Two dedicated IC test setups were developed for the prototype- and production test of the chips. The wafer tests of the production series should be completed during the fall of 2004.

The IC's were tested individually and later as a complete system. All functional and performance tests were performed before the miniaturization step was taken.

II. System

A. Requirements

The *EndCap* module must fit in a relatively small space. First estimates did foresee major difficulties when using commercial discrete components. Therefore the use of ASIC's was mandatory. Second is a power budget of 10W for each module, and no heat up of surrounding components is allowed. A cooling system is available for the detector hybrids and therefore also for the *EndCap* modules. The water temperature is ~18ºC.

The *EndCap* must be radiation tolerant, fail safe in case of Single Event Upsets and fail safe in case a detector or a hybrids breaks down. A broken part may not affect good parts.

All connections to the *EndCap* must be free of any detector bias potential, this means that all signals (except power and bias) are at ground level.

The ALICE SSD must be equipped with 144 *EndCap* modules. Each EndCap must be able to control 11 to 14 detector modules.

B. Architecture

The *EndCap* is an intermediate module and therefore signals must be repeated, power regulated and it must be remote controllable via the serial bus that is used for the front-end.

The signals that enter the *EndCap* are buffered by the first control chip (Fig. 3). This is the communication between the DAQ and control system and the detector, and it is connected at ground level. After this the signals cross the bias potential and are buffered again. These buffers and controls are placed on the Interface-Card in 3 ALCAPONE IC's. These chips regulate the power for the next series of controllers

The next ALCAPONE IC's are connected to the hybrids (max. 28 per *EndCap*) and control each hybrid and its power supply (+latch-up protection). The analogue signals coming from the front-end chips enter the *EndCap* and are multiplexed and buffered by the ALABUF chip. The last mentioned functions are placed on the Supply-Card. It can connect to 4 front-end hybrids (= 2 detector modules). This means a SupplyCard has 4 ALCAPONE IC's and one ALABUF. The buffered differential analog signals go directly to ADC cards at about 30m from the detector.

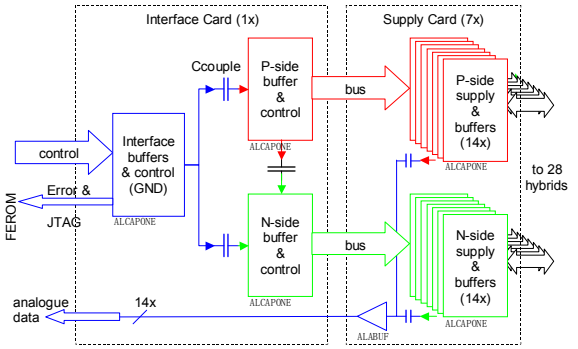

Figure 3: EndCap Architecture.

The *EndCap* module is composed out of 1 Interface-Card, 1 to 7 SupplyCards (usually 7), a backplane PCB, and a CableCard which has all cables for the connections to the DAQ & control system.

The power supplies for the detectors, for the *EndCap* ground level electronics and the bias level electronics are all floating supplies with sense wires up to the *EndCap*. The connections between the real ground and local "grounds", like ground P-side and ground N-Side are made inside the *EndCap*. The mechanics is at real ground level, and forms a shield around each *EndCap*. In this way the analogue buffer is very close to the signals source and ground reference, and it is shielded. This approach should prevent electromagnetic interference.

C. Detector readout

To start the readout, the front-end chip requires a token and a clock signal. These signals are distributed by the ALCAPONE chips. By generating a delay in the token to one of the two sides, it is possible to readout a detector module via one single differential line. For this an AC coupled multi-

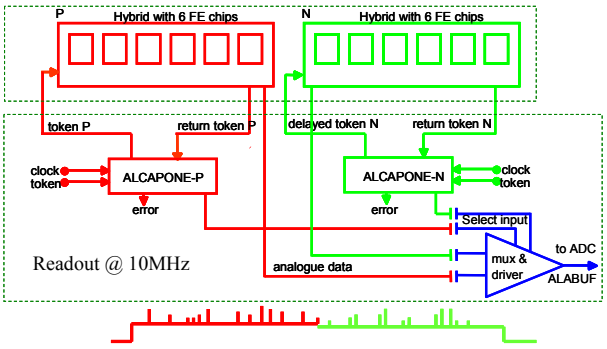

Figure 4: *EndCap* detector readout.

plexer must switch from one side to the other at the right time.

The token delay is implemented in the ALCAPONE and is programmable to deal with broken front-end chips. The token

can bypass broken chips, but then the readout length is changed. The control of the analogue multiplexer is also implemented in this chip (Fig. 4) because it depends on the token delay.

D. ALCAPONE

The ALCAPONE chip is a 2 x 4 mm IC designed in 0.25um CMOS technology. It has LVDS and CMOS receivers which are suited to us AC-coupling at the input. This is achieved by adding positive feedback to the receivers.

The chip has a shunt-regulator to generate its own power and a programmable power regulator for the hybrids. There is an internal Band-gap circuit for voltage reference.

All digital functions like control for the token delay, control for the analogue multiplexer, power supply control, status monitoring, error handling and JTAG are synthesized into a logic block.

An 8 bit SAR-ADC (+oscillator) is available to monitor the detector current and PCB temperature with an NTC resistor.

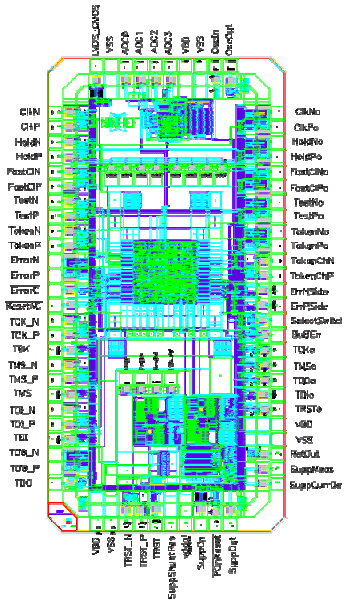

Figure 5: ALCAPONE chip

E. ALABUF

The analogue buffer and multiplexer are integrated in this 2 x 2 mm chip. It has 2 differential drivers (gain 5.6) for 100Ω twisted pair cables, with each 2 input channels. The selection of the inputs can be done via AC coupled CMOS signals. The power current is 91mA in enabled state and ~10mA when disabled. The settling time is <20ns and the non-linearity error is <1% at maximum 1.85V differential output voltage. Chips irradiated up to 300krad showed no change in the specifications of the signal transfer.

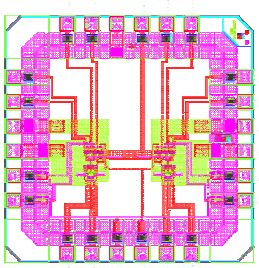

Figure 6: ALABUF chip

F. Power functions

Due to the distance of the *EndCap* to its power supplies, it is required to regulate the power locally for the 2.5V front-ends. The power for the detector modules must be controlled to protect the modules from single event latch-up. Therefore the ALCAPONE has a regulator that, with the use of external transistors, can guarantee a good supply voltage for all electronics in- and behind the *EndCap*.

Since the front-end chip is very sensitive to noise from the power supply special precautions were made. Inside the ALCAPONE, the voltage reference has 2nd order low-pass filter. An additional external decoupling capacitor was added after measurements with the first prototype. The measured RMS noise (0-30MHz) at the supply output is now less then 65µV at the 2.5V output.

The power can be regulated from 2.1 to 2.9V via a JTAG register, and the current limits are fixed at ~.35A and ~1.5A (resistors) for the hybrid- and the internal supplies. All supplies can be switched except for the first one's which supply the I/O controllers of the *EndCap* (on InterfaceCard). These supplies switch on after power-up, and recover automatically after a current limit is exceeded. This is determined by a control pin.

G. JTAG control (IEEE 1149.1)

The ALCAPONE chip makes all connections in- and out of the *EndCap* and is therefore provided with ***B***oundary ***S***can ***T***est cells at each logic I/O port. These cells are programmable according to the IEEE1149.1 standard. In this way the wire-bonds to all BST I/O's can be tested after PCB assembly.

The configuration bits for the control functions are available in special function registers added to the ***T***est ***A***ccess ***P***ort (TAP) of the JTAG interface. Registers like Status, TokenDelay, PowerControl etc. are available via the JTAG bus.

Since the JTAG signals (TCK, TDI, TDO, TMS and TRST) are buffered by the ALCAPONE, they can also be manipulated. The chip can function as a JTAG switch. This means that the ALCAPONE can switch on or off the serial chain behind it. This is done to prevent that broken parts break the JTAG chain. After power-up the *EndCap* has only the first ALCAPONE chips powered on the Interface Card (see fig. 3), and only the first chip is connected to JTAG. Via the JTAG port the other sub-chains can be added by switching on the corresponding supplies and JTAG bits. This creates a safe method for the serial chain, and one can determine if there is a failure and where the problem can be.

III. DEVELOPMENT

1) Start Development

The use of AC coupling for the analogue data had to be verified. The constraint is that an increase of noise of 5% of the basic detector noise is allowed. This "noise" comes from AC-coupling plus the driver at the expected detector occupancy and trigger rate. Calculations and measurements indicated that a 560nF couple capacitor (+2kΩ buffer input impedance) is sufficient for the 10MHz readout with a maximum of 7.5% channel occupancy. Effects which influence the position resolution and signal amplitude are negligible with this time constant and the capacitor fits in the available space.

2) *ASIC Prototyping*

After 2 prototypes of the power and shunt regulator, LVDS receiver for AC-coupling and the analogue buffer, the first version of the ALCAPONE was submitted. For this chip a test board was developed on which all functions could be verified. All I/O's of the ALCAPONE are made available to connectors. The purpose of this is that with these boards and cables, a complete functional *EndCap* could be composed, 3 boards for the InterfaceCard and 4 plus one ALABUF board for a SupplyCard. See the *EndCap* Architecture in figure 3.

With the use of 11 "stacked" cards and 4 detector modules, a beam test is performed. No signal degradation is observed when using the "*EndCap*" compared to basic measurements of the hybrids, *EndCap* noise is negligible. Power supply sensitivity of the front-end was detected and using additional capacitance at the power supply reference the noise was further reduced. After this the ALABUF and ALCAPONE were ready for production. This is done using two shared production runs with other institutes related to LHC experiments.

3) *EndCap Mechanics*

The mechanical design includes mainly electronics PCB's, cooling tubes and the connection between the two. The RVS cooling tube is soldered on a RVS plate. On this plate thin aluminum rails are bolted. By adding a long treaded bolt thru all rails and the PCB's, all parts can be clamped together and are then be tightened to the cooling plate. In this way the *EndCap* is closed, fixed and good thermal contact is guaranteed.

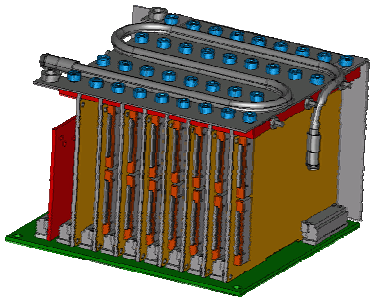

Figure 7: *EndCap* mechanics.

4) *PCB Prototyping*

The prototypes of the InterfaceCard and the SupplyCard showed no severe difficulties. For test purposes special "extender" boards are required to reach test-points on the small PCB's (fig. 8). The 2-layer kapton (flex) PCB's glued on aluminum plates could be produced without major problems.

Figure 8: *EndCap* Prototype with extender boards

Improvements were necessary on the PCB etching procedure of the 200µm pitch copper lines (17.5µm thickness) to improve wire-bonding.

Temperature measurements with a thermal camera showed good heat transfer to the cooling strip (fig. 9).

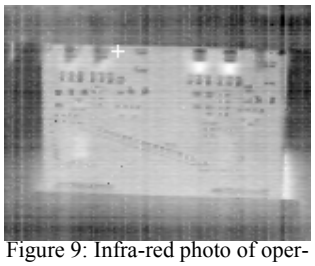

Figure 9: Infra-red photo of operating SupplyCard

5) *PCB production test*

In order to be able to test ~200 InterfaceCards and 1200 SupplyCards, an automated setup is required. The test is based on JTAG connectivity test for the ALCAPONE I/O's. In addition some analogue functions must be tested to verify proper assembly of components and good quality of all wire bonds.

Since each PCB has backplane connectors, and the Supply card has additional ZIF connectors to connect the detector hybrids, the tester must be able to test all these connections. For the JTAG BST connectivity test a special "connection" board is designed to be able to connect all connectors of the cards (fig. 10). This connector board is replaceable in case the connectors wear out. The board is connected to a FPGA board which is the controller of the test.

Figure 10 SupplyCard in pcb test setup.

In order to be able to do the BST connectivity test, the net lists of the separate boards need to be merged to one. With this net list the ATPG software can **A**utomatically **G**enerate the **T**est **P**attern. Now the JTAG test software can perform the connectivity test of the connected boards, and the diagnose tool can indicate if there is a wrong connection (short, open, stuck at) in the system. This test will be performed before the ASIC's will be provided with glop-top.

After all *EndCap* boards are tested the final module can be assembled. Again in this stage the JTAG BST will be applied. All interconnects of the complete module between the cards and the backplane can be verified. The functionality of the individual boards is already tested, so only the interconnects could give errors. In this way we are able to test a complete module in a very short time, which is necessary to meet the production time schedule for the experiment.

IV. ASIC TESTS.

As mentioned before, the ASIC's were first tested on the test boards for the first prototype tests. But to test larger number of chips a more sophisticated setup is required. It is build around a PC with a digital and analogue I/O PCI Card. The supply voltages are delivered by programmable power supplies (one also serves as programmable load). An oscilloscope is used to measure fast signals (fig. 10).

The test electronics consist of a FPGA and programmable switches. The test patterns are programmed in the FPGA and activated by the software. Low frequency signals are verified by the analogue I/O card and faster signals (rise time, amplitude and pulse width) by an oscilloscope. This approach results in a test setup that can easily be moved, first in the laboratory for prototype tests, and later to a clean room where the wafers are tested. By replacing the Chip Socket Adapter with the Probe Card, the wafers can be tested. For both ASIC's is such a tester developed.

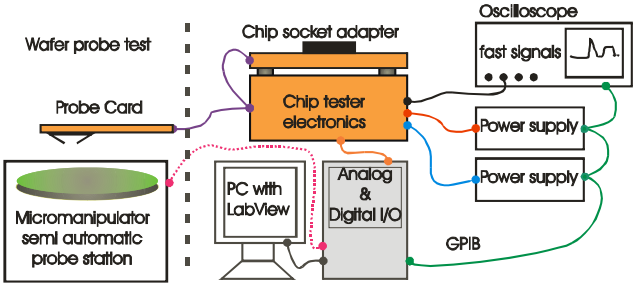

Figure 11: ASIC test setup.

Test limits, -data and -results are saved in XML data format. This gives the advantage of using a commercial tool and with the use of "style sheets" one can easily select specific data out of the result files. For example to generate a histogram of the power consumption of all 720 ALABUF chips on a wafer (fig.12). The post processing of the selected data is done using MathCAD. After the selection of the required data the result of a tested wafer is generated in a few seconds. This approach turned out to be quick and flexible.

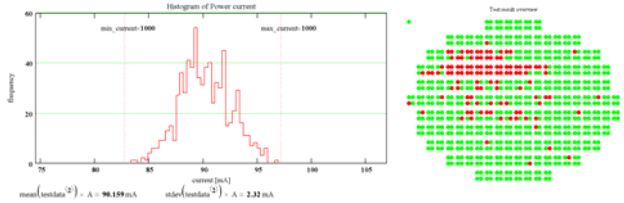

Figure 12: Wafer Power dissipation distribution.

The test time for one ALABUF is about ~45 seconds and for one ALCAPONE ~30 seconds. The probe station is also controlled by the LabView program, and the time required for testing one wafer automatically is about 10 hours. The tester was programmed to do maximal 3 retries in case the first connectivity test failed, this to be less sensitive to probe contact problems.

The contact resistance during the test varied between chips. Therefore the results of some parameters are not reliable, in particular when the voltage drop due to the current thru a pin becomes significant with respect to the measured value. This should be taken into account when discussing the testability of future designs. The contact resistance varied between 2.5 and 8Ω. The measured yield for 4320 ALABUF chips is ~85% with a gain within 2%. The ALCAPONE wafers are not tested at the time of writing this document.

V. CONCLUSION

With the design of this module, we demonstrated the use of full custom ASIC's. The development this module with the given constraints for space, radiation tolerance and power, was not possible without the use of the ASIC's.

The prototype- and beam tests have demonstrated that the use of AC coupling for the digital- and analogue signals is a robust method for signals to cross different voltage potentials.

Because of the large number of interconnects inside the module, and on the individual boards, the use of Boundary Scan Test saves a lot of test time during the production phase. Additional test features via the JTAG port ease the prototyping and debugging work. The preparation though of the BST is very time consuming.

The use of reprogrammable FPGA's in the testers has been very useful, reuse of logic cells and quick adaptation to beam test- and production test setups which can be done in a short time. This makes the test setup very flexible for different tests and users.

VI. ACKNOWLEDGEMENTS

For the development of this module, the support for MPW's for the ASIC prototypes and the mass production run by the microelectronics group at CERN has been of great value.

VII. REFERENCES

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