ALEPH 94-176
MINIV 94-007
24 November 1994

User's Guide for the MPI ALEPH VDET Test Stand

Version 1.00

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November 23, 1994

1 Introduction

This guide describes the operation of the VDET test stand at the MPI. It begins in Section 2 with a block diagram of the DAQ system following signals from the silicon detectors to the VAX. This is followed by a timing diagram for the various signals in Section 3. In Section 4 one finds the definitions of the various voltages that must be applied, the sequence in which to turn them on, and instructions for tuning those voltages which need adjustment. Section 5 closes this note with a description of the data acquisition procedure and analysis. Some parts of this description hold also for the ALEPH setup. This will be mentioned explicitly.

2 Basic Readout Block Diagram

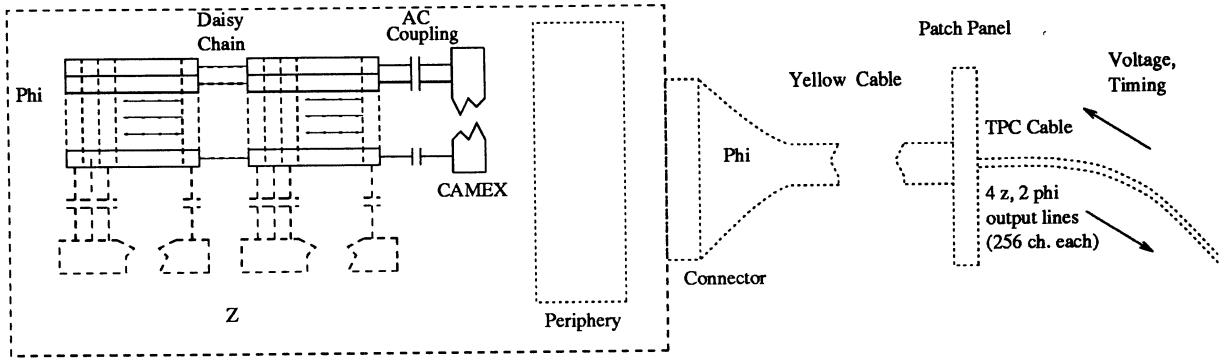

Figure 1: Schematic view of physical layout of a detector module. The phi strips and readout are indicated by solid lines. The z strips and readouts are on the opposite side of the detector module and are indicated by dashed lines.

Figure 1 shows a schematic view of an ALEPH VDET module. A module is composed of two detectors and two electrically independent modules compose a VDET face. The

physical location of the VDET MPI teststand is divided into the cleanroom that contains the silicon detector and the lab which contains the rack electronics and computers. Logically these simulate the pit and counting room. The counting room modules and their connections are illustrated in a block schematic in Fig. 2. Figures 3 and 4 show the lab configuration.

For the two detectors mounted in a module the phi strips are daisy-chained as shown in Fig. 1. (Details on the electrical readout may be found in Section 4 and Fig. 7). The strip signals go to the AC coupling chips and arrive at the CAMEX preamplifier. The z readout is not daisy chained, but follows the same path from strips to AC coupling to CAMEX. As a result, there are twice as many Z channels as phi channels. Additional periphery electronics mounted to a module include and support line drivers, control signals, voltages and filtered voltages. The phi strips appear as 256 $\times$ 2 sets of channels and the z strips appear as 256 $\times$ 4 sets of channels[1]. Hence, given the number of strips and the daisy chaining, one arrives at 6 parallel lines of signals coming from the detector. These six signals pass through a specialized connector into the "yellow cable". This yellow cable goes to one side of a patch panel. On the other side a TPC cable runs into the counting room. Those two cables not only carries signals from the pit to the counting room, but they also carry voltages and timing back to the pit from the counting room.

In ALEPH the yellow cables go from the detector to the patch panels which are located on the TPC endplates. From there the TPC cables go to the C3 barrack.

The interface between the counting room and the pit is the ADAC (Analog Distribution Card). A bank of voltage supplies feeds into the ADAC to provide the necessary power. This bank is described in more detail in Section 4. Test, timing and sequencing pulses come from the AFAC (Analog Fanout Card) and are conveyed to the pit by the ADAC.

Since there are several paths to follow, we take these one at a time:

1. Signal Path
   We begin with the signal path. This path runs from the pit to the counting room. The 6 signals are carried by the TPC cable to the ADAC, then carried by ribbon cable to a switchbox. This box allows one to feed the signal to a MUX or a scope output (In ALEPH this switchbox does not exist in this form. There is a switch panel which allows to connect a scope to the signal outputs). If the green switch is pushed in on the switchbox, the signals go through a ribbon cable coming from the back of the switchbox to the MUX which serializes the six signals and sends them to the ADC and storage unit, the SIROCCO.

   If the switch on the switchbox is left out, the signals go to the output lemo connectors on the front of the box. There are two sets of two lemo connectors to allow for testing of the differential signals from two channels coming from the module. Hence, one has two pairs of two coaxial cables carrying the signals for these two channels. Two cables for one channel are typically sent to two channels of the oscilloscope where one signal is inverted and then the two are summed. Other combinations of viewing

[1]The grouping in this way is connected with the expectation that signals would finally be processed by a TPD which had a memory depth of 256. This fact is now historical since we don't use TPD's.

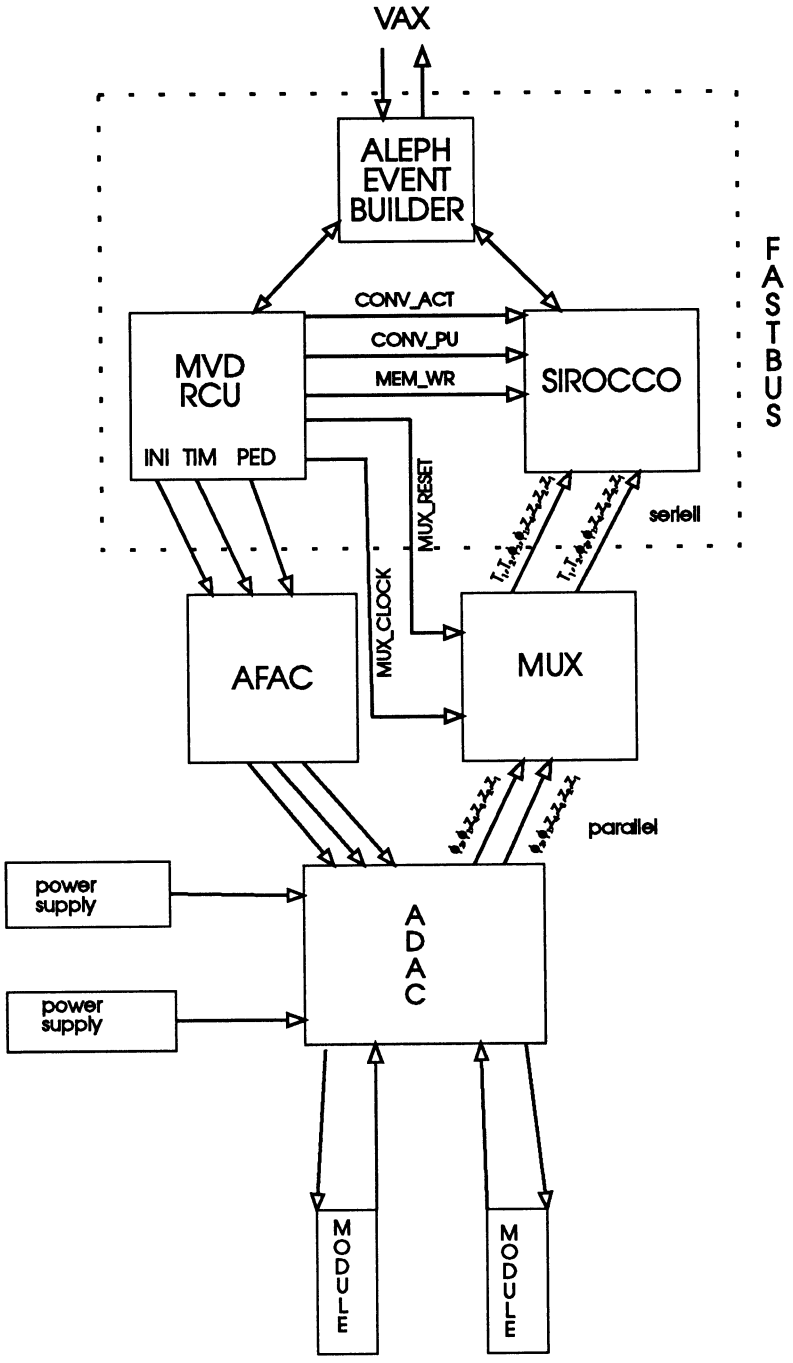

Figure 2: Block diagram of the components for reading out the silicon detector.

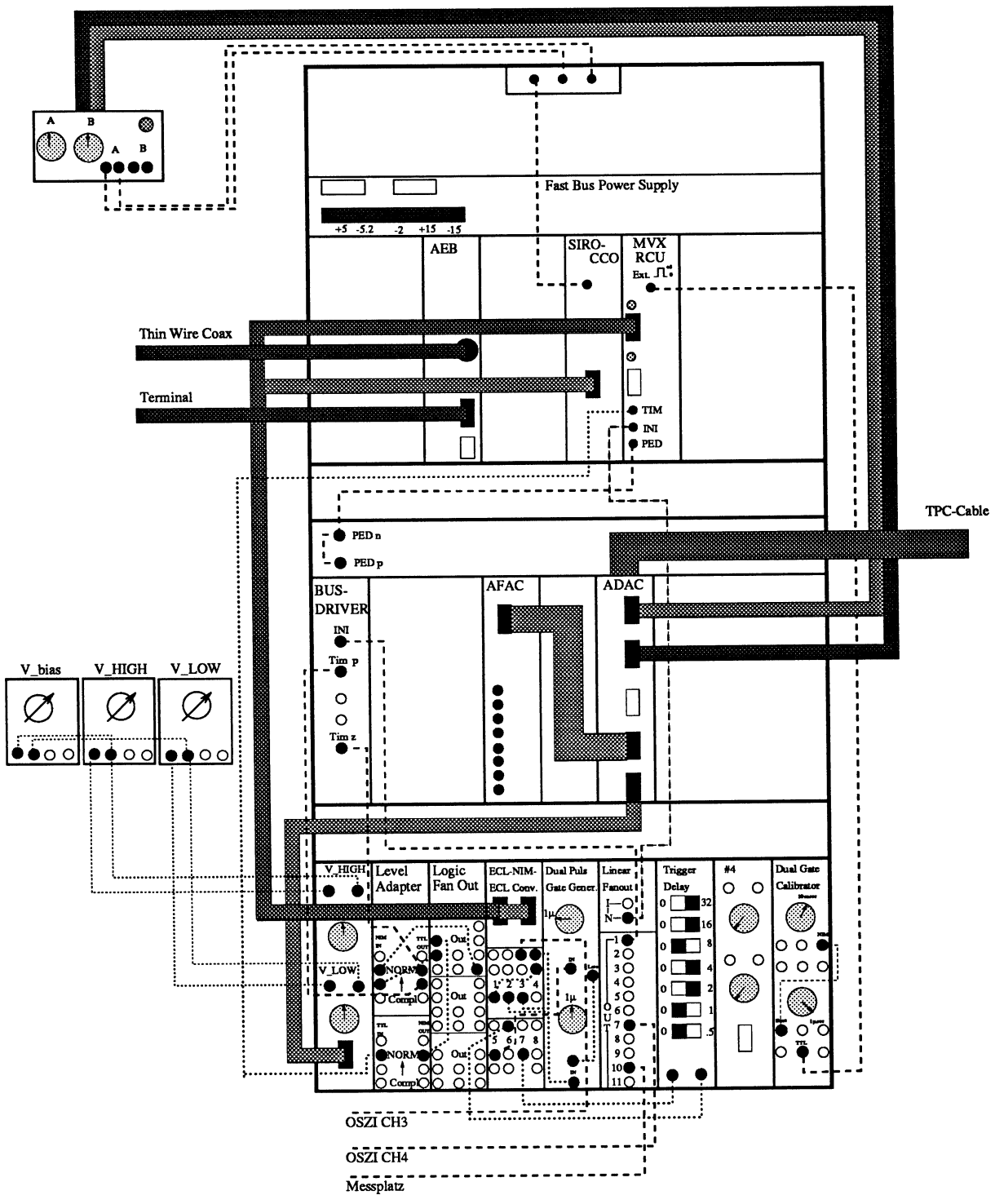

Figure 3: Sketch of the NIM rack electronics found in the test lab.

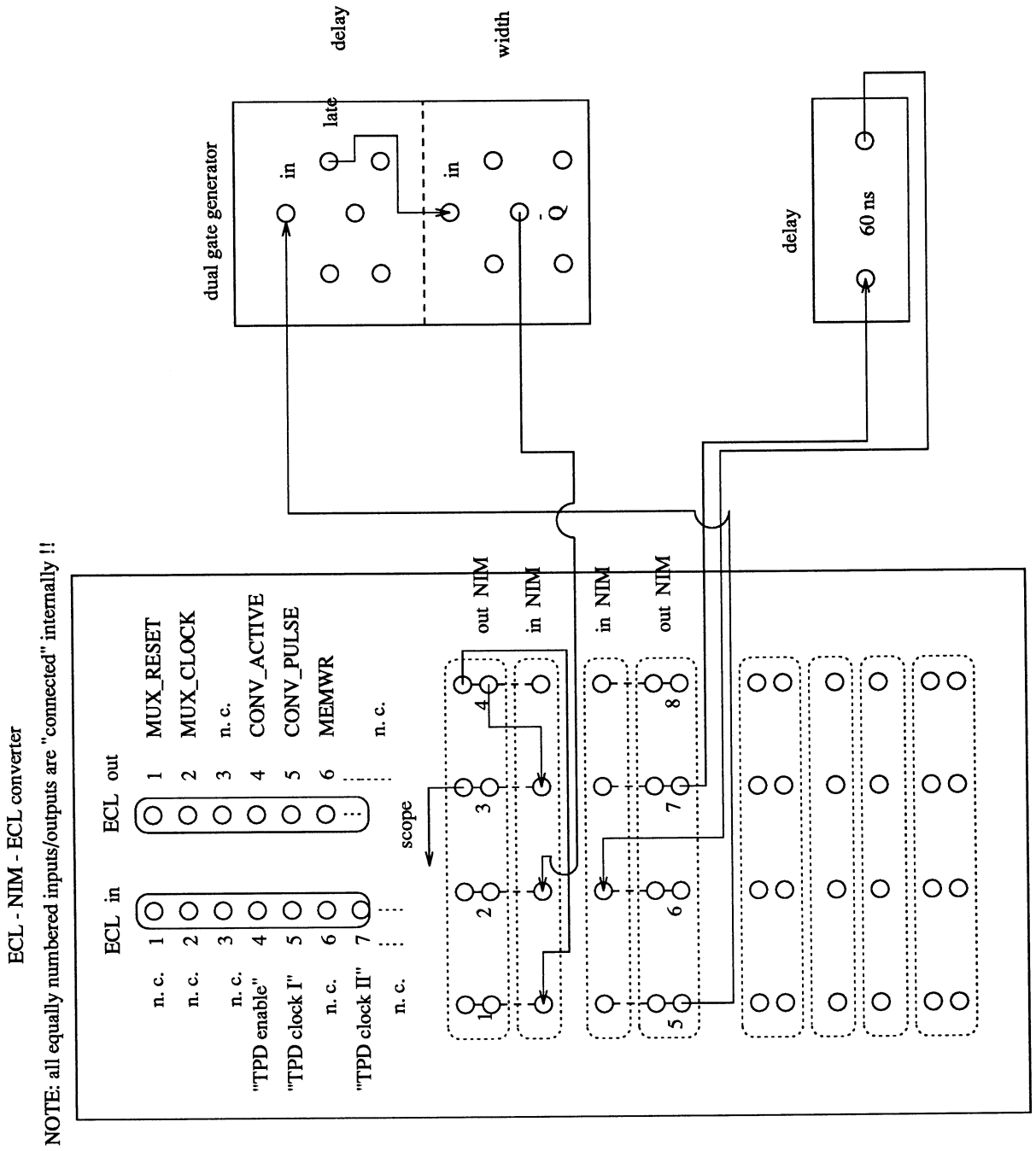

Figure 4: Detail of ECL-NIM convertor diagram in the electronics rack in the test lab.

are possible, such as looking at one of the two differential signals for each of two differnent channels.

The INI pulse from the MVDRCU (MicroVertex Detector Readout Clock Unit) goes to a fanout and is used to trigger the scope. (The actual path, the MVDRCU and its pulses are described in detail below.) In this configuration only one of the six outputs may be viewed. The choice is made by setting the dial to a number between 1 and 6, corresponding to the four Z strips and two phi strips, respectively.

At this time we have no MUX; on the top of the relay rack is a small recepticle for the same two cables that would run to the oscilloscope. The signal from this box goes directly to the SIROCCO front panel. However, this means that only one of the six signals is available for further processing. The consequence of this is that we would have to repeat the data taking six times to get a complete measurement. In the present conditions, one can use a second set of cables terminated into the oscilloscope with 1 MΩ so that switching to DAQ mode from free running mode may be done without unplugging cables.

After digitization, the data are read out from the SIROCCO to the ALEPH event builder (AEB). In ALEPH the AEB has been replaced by a FASTBUS-VME interface (FSVBI) and a VME-processor (FIC).

2. Voltages
This path goes from the counting room to the pit. The bank of voltage supplies controls the operating voltages on the CAMEX as well as the bias voltages on the detectors. Details of the layout, the meanings of the various voltages and the procedure for turning on the detector are given in Section 4. Here we only point out that the voltages coming from this bank are connected the module indicated in Fig. 3 in the bottom left corner of the rack (marked V HIGH and V LOW in the figure). This module has connections for voltage montoring (also described later in Sect. 4) and a cable that carries the voltages to the ADAC so that they may be conveyed to the TPC cable. In ALEPH the voltages are generated by special computer controlled power supplies.

3. Pulses
There are three pulses needed for operation. These pulses originate in the MVDRCU, a FASTBUS device which is controlled via FASTBUS transfers from the AEB. The three pulses are:

   - Initialize (INI) – Resets all switches at the start of a data taking cycle;
   - Timing (TIM) – Step-by-step control of the actions of the various chips on the module;
   - Pedestal or Test Pulse (PED): Prepulses the CAMEX chips for better use of the dynamic range and to cope with the offset in the line driver voltage.

   Each of these pulses follow various paths to a number of destinations.

   (a) The Path of INI
   The INI signal goes to a linear fanout and is split to three locations. One

location is used for viewing on a scope; another is used to trigger channel 4 of the scope, allowing for timing to be set up for the remaining logic. The third channel is sent to the AFAC BUS DRIVER which then feeds the ADAC cards so that the INI signal may be taken to the pit via the TPC cable.

(b) The Trek of TIM
The TIM signal eventually ends up in the AFAC BUS DRIVER and from there goes to the ADAC, through the TPC cable to the pit. However, it needs to be fanned out to the phi and Z strips. Therefore the signal goes first to a Level Adapator where it is converted from TTL to NIM. A Logic Fan Out takes the Nim signal and fans it out to the two signals needed. These signals are sent into the NIM to TTL convertor and finally to the BUS DRIVER.

(c) The Perils of PED
The PED pulse goes to a flat box on top of the crate holding the AFAC and ADAC. This pulse is sent into two inputs, one for the n–side and the other the p–side. It is then fed from the back of the box into the AFAC BUS. The AFAC allows for two modules to be pulsed with two different test pulses. The potentiometers accessible with a screwdriver from the front panel adjust the pulses according to the following pattern:

Module 1	ϕ	Test 1
Module 2	ϕ	Test 1
Module 1	ϕ	Test 2
Module 2	ϕ	Test 2
Module 1	z	Test 1
Module 2	z	Test 1
Module 1	z	Test 2
Module 2	z	Test 2

These pulses are handed to the ADAC for accumulation and transmission through the TPC cable. (In ALEPH the ADACs are realized using different hardware, but have the same functionality).

4. MVDRCU – SIROCCO timing communication
The CONV_AC, CONV_PU, and MEMWR timing signals are carried by a ribbon cable that runs from the MVDRCU to an ECL-NIM convertor and then to the SIROCCO. The general path of the ribbon cables from the MVDRCU and SIROCCO to the ECL-NIM unit is indicated in Fig. 3; details of the connections at the ECL-NIM unit may be found in Fig. 4.

5. External triggering
A Dual Gate Calibrator is available to send a external trigger to the MVDRCU but is not presently used. Use of this external trigger would require reprogramming of the MVDRCU.

3 Timing Profile and Readout

At this point is worth looking at the timing sequence shown in Figures 5 and 6. The timing sequence divides naturally into four parts. These have no official names so we take the liberty of assigning names.

1. Pre and Post-Crossing
   The cycle begins (t=0) with the EGBX (Early Gated Beam Crossing) where the INI signal coming from the MVDRCU clears the capacitors in the CAMEX. A series of timing pulses, the second signal from the MVDRCU, is fired before BX (t=2.5μs). Four of the timing pulses are used to sample the signal before the beam crossing. A further sequence of signals fires after the beam crossing. There are 800 ns between the last pre-crossing signal and the first post-crossing signal. Among the post-crossing signals are four samplings of the detector outputs.

2. Trigger-wait Interlude
   All signals are quiet while waiting for a trigger to come. The detector waits for a "NO" in a predefined time interval. If it receives a "NO" signal, then the cycle goes back to the beginning of the Pre and Post-Crossing period with the INI pulse. In ALEPH these trigger pulses (EGBX, NO, YES) are generated by the trigger supervisor reciever (TSR). The logic is the same, the timing may be slightly different.

3. Readout sequence
   If the readout is not inhibited, a sequence of 256 TIM pulses follow, signalling the series readout of 6 parallel lines, the 6 signals consisting of 4 z and 2 phi readouts. Each of these pulses takes 5.3 microseconds. The MUX_RESET line drops and the CONV_ACT line goes high so that the MUX is enabled and the conversion in the SIROCCO is enabled. A word of caution to those trying to duplicate the timing pattern without an MVDRCU: The waveform for TIM shown in Fig. 6 must be a sequence of short pulses having a duration significantly shorter than the 5.3 microsecond period. Using a pulse shape which is high for 50% of the cycle (2.65 microseconds in this case) while easier to generate, causes enormous pedestal shifts.

   Within each of these 256 time pulses, the six outputs are sampled and serialized as indicated by the CONV_PU timing in Figure 6. There are two dummy pulses (T1,T2) to allow for the rather long rise time of the line drivers against the transmission cable. Then the readout occurs for the two phi and four z strips. These signals are carried by the MUX under control of a set of MUX_CLOCK pulses that are synchronized with the CONV_PU timing. The signals are digitized by the SIROCCO and stored in memory under control of the MEM_WR pulses which are coordinated with the CONV_PU and MUX_CLOCK pulses by the MVDRCU. Details of the relative timings may be found in Fig. 6.

   After the last memory write pulse, at least 200 ns is allowed to elapse and the CONV_ACT line is dropped.

4. Wait for next BX
   All signals are once again quiet as we wait for the next beam crossing. In the test

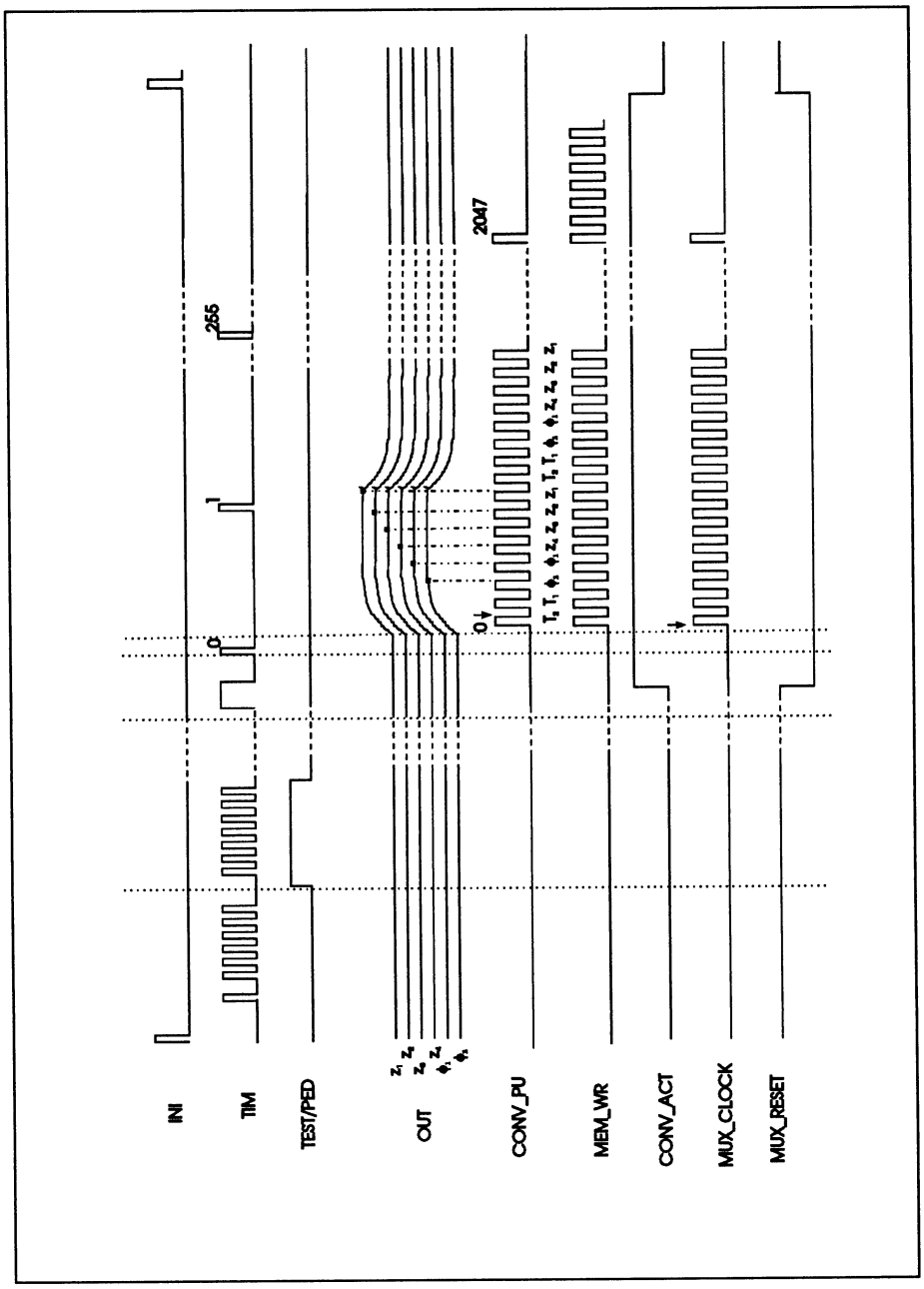

Figure 5: Timing diagram for the VDET.

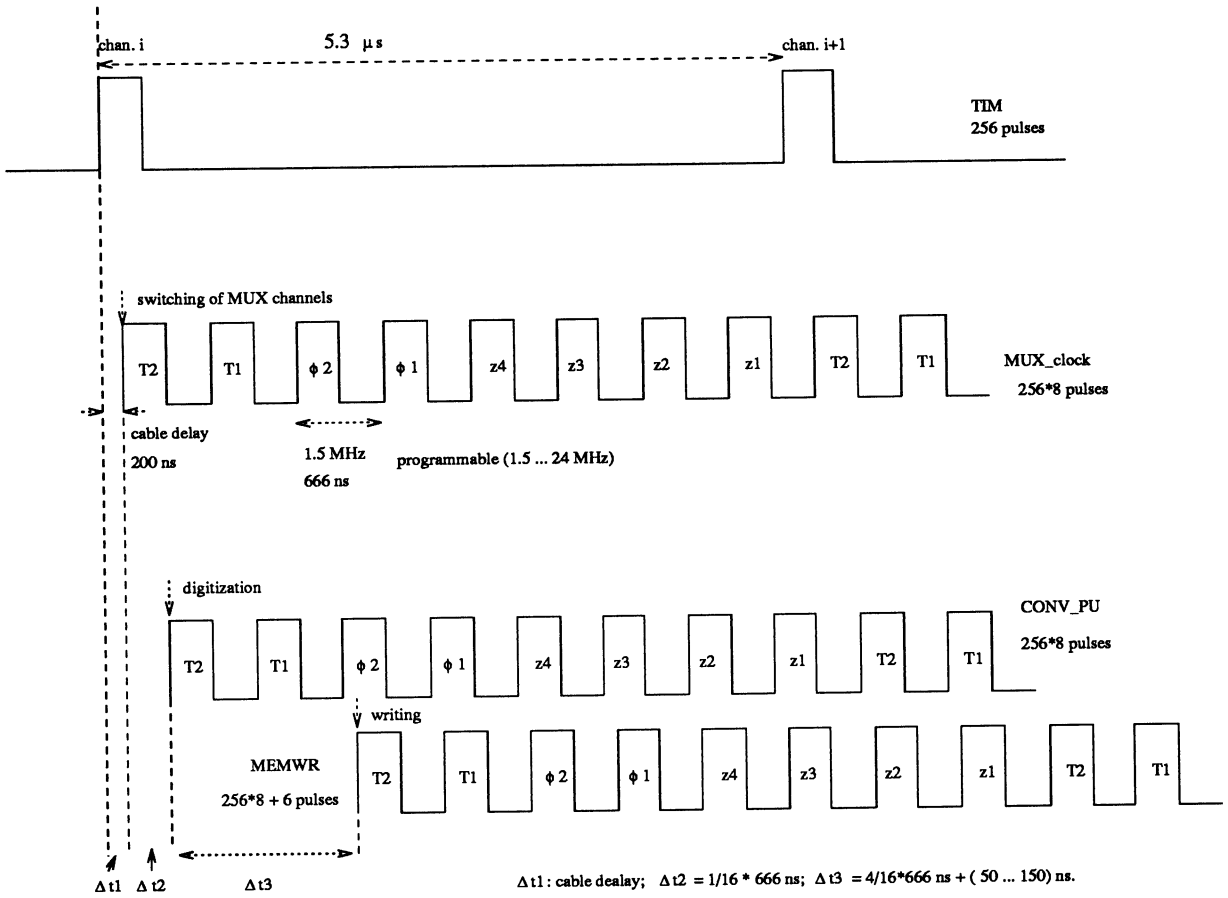

Figure 6: Further details of the timing diagram for the VDET, showing the timing between two pulses of the 256 TIM pulse train.

setup, there is no EGBX and no BX. As soon as the readout is finished, the entire clocking is reset and the sequence started again.

The time sequence is programmed into the MVDRCU. Hints on how this is done may be found in Sec. 4.3.

4 Voltages and the Power Bank

Here we describe the function of each of the voltages, the location of their supplies and the procedure for turning them on.

4.1 Functional Description of Voltages

In order to describe the various power supplies and their operation, it is necessary to examine the layout of a single strip in the detector. This is shown in Fig 7 as an oblique cut through the detector. For most voltages, there are two values, one each for

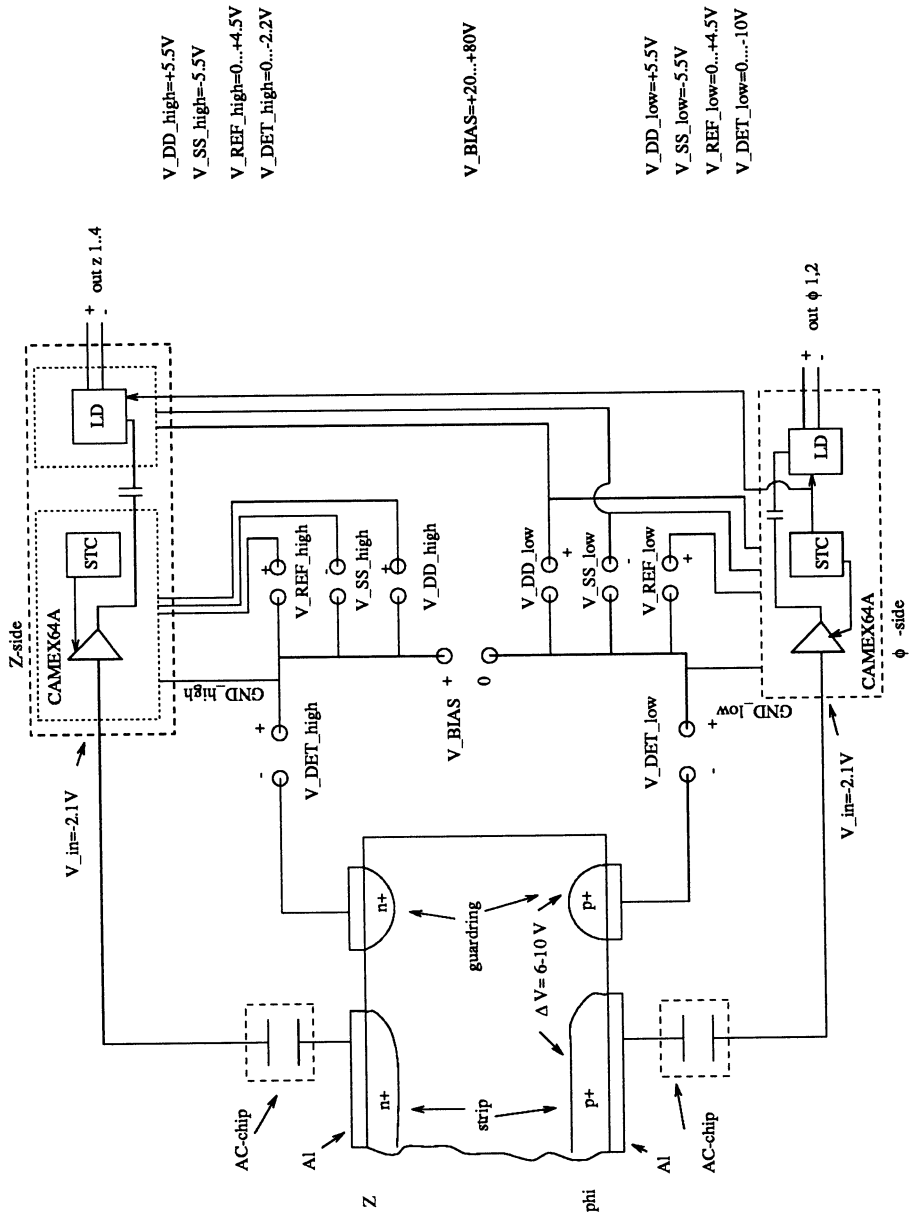

Figure 7: Circuit diagram for the silicon showing the voltages.

the p and n material in the detector. These correspond to the ϕ strip and z strip voltages respectively. The phi strip voltages are designated by the label "low" and the z strips by the label "high". In Fig 7, a single strip and its guard ring are illustrated. The strip is capacitively coupled to the CAMEX amplifier. One reason that coupling is necessary is that the CAMEX amplifier is offset at the input by $-2.1V$. The amplifier requires voltages $V_{DD} = +5.5V$ and $V_{SS} = -5.5V$. An additional voltage, V_{ref}, is tuned to minimize the noise but at the smallest possible power consumption. It is normally between 0 and 1 Volt; running at 4V gives 25% less noise.

A separate voltage for the guard ring, V_{det}, is usually set to zero but may be set to a negative value. It is tuned in order to recover channels where the blocking capacitor has shorted due to "pin holes". These are caused when excessive ionization in the detector induces a large voltage drop across the capacitors coupling the strip to the CAMEX. These voltages cannot be handled and a short is produced, placing the strip at -2.1 volts relative to the guardring and neighboring strips. For the z strips only, V_{det} allows one to tune away this voltage difference and recover the pulses from this and about 10 neighboring channels. These other channels are affected by coupling through the failed channel. When the tuning is done, one observes first that these neighboring channels recover and finally the faulty channel recovers.

It is important that V_{det}^{high} not be turned on before other power supplies because the voltage is opposite that of the bias voltage: the diode will turn on and cause a short circuit.

The bias between the p and n strips is held by the depletion voltage, V_{bias}. This voltage is different for each detector. The proper voltages for the ALEPH detectors are set in Pisa and the database of voltages is kept in a reference folder. If the proper V_{bias} value cannot be located for a module, it can be tuned as described below. V_{bias} takes on a value between 20 and 80 volts.

The timing sequence is handled by the STC logic. This controls timing in the CAMEX. For the phi side (p strips) the STC also provides reset signals to the two line drivers (LD). Each line driver is servicing 256 strips. These line drivers are capacitively coupled to the output of the CAMEX because V_{bias} places the CAMEX output at the bias voltage. V_{DD}^{low} and V_{SS}^{low} power the line drivers. It is important to be sure to power the "low voltages" first so that the STC can clear the line drivers and prevent potentially damaging charge buildup.

The test pulse signal is injected into the input of the CAMEX amplifiers and used to diagnose the readout as well as to provide a well–defined pedestal.

4.2 Physical Location of Voltages

The physical layout of the voltages is shown in Figure 8. (This section applies for the test stand only.) The bank of voltage supplies on the far right is used to power the AFAC crate. Immediately to the left of these are two banks. The lower bank of supplies are V_{DD}^{low}, V_{SS}^{low}, and V_{ref}^{low}, corresponding to voltages for the p side. The supply on top provides V_{DD}^{high}, V_{SS}^{high}, and V_{ref}^{high}, corresponding to voltages for the z side. Left of these two supplies are those for V_{bias} and below it, that for V_{det}^{high} and V_{det}^{low}. Note that there is also a mulitimeter on top of these supplies. This measures the detector current and is

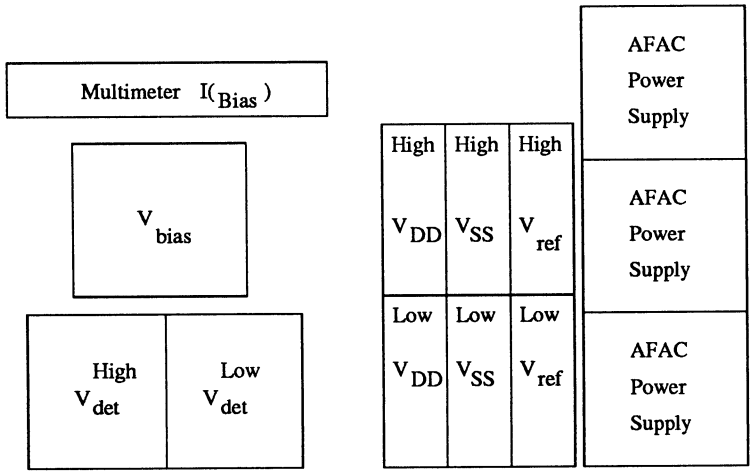

Figure 8: Sketch of the power supply locations found in the test lab.

in series with the supply providing V_{bias}. It must therefore be on for the voltage to be supplied.

4.3 Voltage Ramping Sequence

The voltage ramping sequence must be carefully followed. If not, damage to the CAMEX/LD is likely. At this point the monitoring of the detector via scope is recommended. (See Figs. 3 and 4 for the proper electrical connections.)

1. The FASTBUS and NIM power supplies must be turned on. The location of these supplies is shown in the drawing of the rack layout in Figs. 3 and 4. Use the buttons for monitoring the FASTBUS voltage to be sure all is well. If not, cycle the FASTBUS supply.

2. Check that there is no detector plugged into the yellow cable. Then turn on the power supplies for the module operation. These are shown in Fig. 8. The voltages should be left at zero. This procedure of turning on the power supplies to zero volts with the detector unplugged ensures that no harmful transient pulses reach the module when the power supplies are switched on.

3. Start the AEB

   (a) Check the network disks that will be needed by the AEB. Log into the OS9 account on the MPI VAX cluster and look to see if the job DISKS is running by typing:

   $ SHOW ENTRY/USER=OS9

   If it is not running execute the following procedure:

$start_disks

This procedure starts the network disks for the AEB.

(b) Wait 60 seconds and then push the AEB reset. This increases the chances that the needed network disks are available and the AEB will boot properly. As the AEB is booted, the default timing sequence for scope running is established. This means that the time at which the readout pulses arrive are programmed into the MVDRCU.

(c) From the OS9 account connect to ALEB52 by typing:

OS9 ALEB52

OR it is also possible to use the terminal that is connected to the event builder.

(d) type zsh to log into the AEB.

(e) ignore the bus trap signal; the AEB is now active.

4. The green panel lights on the AFAC should be lit. This indicates that the INI pulse is being sent to the detector. One must not proceed any further unless these lights are lit.

The reason for this was pointed out above, but bears repeating. The line driver may have charge build up on the input. The only way to release this is to cycle the before/after circuits. This is done regularly by the MVDRCU timing or by the AFAC if the MVDRCU is hung. If the lights are not on, the timing may be started by initializing the MVDRCU. This is accomplished by typing the following command on the AEB:

scope

5. At this point, the module may be plugged in in the "pit". Choose the module from the drawer marked 1994 detectors, open the shielded hood and plug in the yellow cable with the side marked ϕ up; the ϕ side of the detector is that which has an unobstructed view of the silicon; the z side is parially obscured by electronics.

6. Place the module on the small vacuum table under the microscope and open the vacuum valve to hold the detector in place. Make sure that the hood is closed and there is no light inside before turning on V_{bias}.

7. The voltages may be raised in the sequence given here. The power supply channels for V_{DD}^{low} and V_{SS}^{low} are coupled, so only the leftmost knob in each supply must be

turned. Three voltage meters are available to monitor V_{DD}^{low}, V_{DD}^{high}, and V_{bias}. They pick up these voltages from the box, V, in the NIM crate which receives the power supply voltages and conveys them by ribbon cable to the ADAC. This box has taps for each of the voltages. The voltages are directed to the taps according to switches on the front panel of the box. Note that one must turn through two clicks in order to change the voltage being monitored.

(a) Turn on the Multimeter. This must be done or the detector bias voltage will not be delivered. Furthermore, the circuit is left open when this is off.

(b) Turn on the LOW voltages, V_{DD}^{low} and V_{SS}^{low}. The current on the power supply ampmeter should be less than 250 mA.

(c) Turn on the HIGH voltages, V_{DD}^{high} and V_{SS}^{high}. The current on the power supply ampmeter should be less than 250 mA. Note that if the HIGH voltages are turned on first the detector will be shorted!

(d) Turn on the bias voltage, V_{bias}, to 20 V or the value indicated for the detector in hand. The current on the Multimeter should not exceed 100 μA and is typically between 1 and 10 μA.

(e) Turn on V_{det}^{low} and V_{det}^{high} – as needed.

At this point the module is on and my be tuned. It is worth emphasizing that the order given above must be followed exactly when turning on the module. This is critical if the detector is not to be damaged. Also, when turning off the voltages, the order should be reversed exactly. Finally, if the INI pulse is not present, no voltages should be changed.

4.4 Tuning Voltages

The tuning of V_{bias} is the first thing to do, but should only be necessary if there is not already a documented setting available. This is really an item that is for experts only. The oscilloscope trace should show a series of 256 pulses. If these pulses are not regular or are fuzzy, increase the bias voltage, V_{bias}, until no change occurs for about a 5 to 10 volt increase. Then dial the voltage back to the lowest possible value.

The voltage tuning of the test pulses may be done now using the potentiometer screws in the AFAC. The meaning of each screw is giving in the table in item 3c of Sec. 2. By cycling through the six signals, the test pulse levels for 256 channels can be tuned such that in the best case one gets a single level. Furthermore, if there are dead channels arising from pinholes, it is possible to tune them to the level of the other channels with V_{det}. Because the precise failure mechanism is not the same for each channel, and because there is only one V_{det} for all channels of a (module) side, it may not be possible to recover all channels satisfactorily: some compromise may be necessary.

Once the tuning is complete, one may proceed to the readout.

5 DAQ and Analysis

The DAQ is run on the AEB. The event builder has set the MVDRCU into scope mode when one issued the commands that were executed when powering the detector. (The

command "scope", typed onto a terminal connected to the AEB was used to put the MV-DRCU into scope mode.) The mode may be switched to take data. Execute the following procedure using the terminal connected to the AEB:
/n8/cmds/new_daq
This will start up the consumer and producer processes standalone_receive and standalone_send. It is best to take data to RAM disk because this is the fastest. There is room for about 100 events on the RAM disk. It is the default directory and should be cleaned up before running the DAQ program. After starting the DAQ program, one is prompted in the following manner and the responses are listed as well:

Give OS9 filename	any name does, like foo.dat (goes on RAM disk)
	(overwrites previous file)
Number Events	100 is max for RAM disk
Do you want to compress data	0 (=no)
Give Number Triggers	about 4 × number of events for RAM disk
	10 to 20 × the number of events for network disk
Give DAQ setting	0

Note that the exact command sequence may not be the same as given above because it depends on the synchronization of consumer and producer tasks. At this point the data will be taken. When this is done, you must copy the ram disk file to a VAX accessible location with the command:

copy foo.dat /n14/foo.dat

This scratch area should be cleaned up after use. On the VAX, this file is picked up by:

$OSGET /scratch4/foo.dat foo.dat

The program to analyze may be used now. Note that if one is logged in remotely, one must:

$SET DISPLAY/CREATE/NODE=MPIW06

Then to run the analysis:

$EXE ANA3 ana

The programs are in [os9.ana]. A typical dialog for running the analysis is given here. Please note that one probably never wants to answer yes to the question "Want the paper histograms?". This does a tree-consuming HISTDO.

```
OS9_mpiw01 > exe ana3 ana
---> CL: compile again RD: run w/ debugger D: D-lines
---> CL,RD,D ? [R] ?
---> Run without debugger
%DCL-I-SUPERSEDE, previous value of FOR008 has been superseded
%DCL-I-SUPERSEDE, previous value of FOR009 has been superseded


device type:  1 ?


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```

```
=                                                      =
=     A  N  A  3 :     Calculate pedestals             =
=                      and sigmas                      =
=     Version 4.0      5-08-89  asw bad channel list   =
=                                                      =
========================================================


filename :  $DISKB:[OS9.os9-5]dadel.dat ? foo.dat
Does data file contain calibration data ? (Y/N):  Y ? n
Give # of units (adcs or detectors):  8 ?
Give # of channels per unit:  256 ?
Is bad channel list existing? (Y/N):  N ?
# good strips:            1         256
 # good strips:            2         256
 # good strips:            3         256
 # good strips:            4         256
 # good strips:            5         256
 # good strips:            6         256
 # good strips:            7         256
 # good strips:            8         256
header    0 com        195.6       195.2       194.7       194.1       193.7
   194.9
      213.2       193.5         0.0         0.0
header    0 com        198.5       198.1       197.7       197.1       196.8
   198.0
      215.7       197.4         0.0         0.0
header    0 com        192.2       192.0       191.6       190.9       190.5
   192.0
      208.1       191.2         0.0         0.0
header    0 com        206.2       205.9       205.4       204.8       204.4
   205.6
      224.6       204.2         0.0         0.0
header    0 com        202.0       201.7       201.2       200.5       200.1
   201.5
      220.1       201.6         0.0         0.0
header    0 com        185.5       185.3       184.8       184.2       183.8
   185.2
      201.3       183.5         0.0         0.0
header    0 com        197.1       196.8       196.3       195.7       195.3
   196.6
      214.0       196.3         0.0         0.0
header    0 com        188.6       188.4       188.0       187.4       187.2
```

```
   188.4
      201.5       186.5         0.0         0.0
header    0 com        190.9       190.6       190.2       189.5       189.2
  190.5
      206.0       188.9         0.0         0.0
header    0 com        192.5       192.4       191.9       191.3       190.9
   192.2
      205.3       191.5         0.0         0.0
 ================================================

 read w/o calib             10 events
 read w/  calib              0 events

 ================================================
Det        1 mean/sigma of com  194.905   6.254
Det        2 mean/sigma of com  194.639   6.226
Det        3 mean/sigma of com  194.187   6.205
Det        4 mean/sigma of com  193.566   6.203
Det        5 mean/sigma of com  193.180   6.185
Det        6 mean/sigma of com  194.489   6.146
Det        7 mean/sigma of com  210.963   7.858
Det        8 mean/sigma of com  193.448   6.523
Do you want to proceed with the rest? (Y/N):  Y ?
ow (ANA3 proudly presents): THE STANDARD PLOTS !
Want the next plots ? (Y/N):  Y ?
make postscript file? (Y/N):  N ?
Want to zoom ? (Y/N):  N ?
new plot wanted? (Y/N):  Y ?
Want to zoom ? (Y/N):  N ?
new plot wanted? (Y/N):  Y ?
Want to zoom ? (Y/N):  N ?
new plot wanted? (Y/N):  Y ?
Want to zoom ? (Y/N):  N ?
new plot wanted? (Y/N):  Y ?
want same plots once again ? (Y/N):  N ?
Want some more plots ? (Y/N):  N ?
Want the paper histograms? (Y/N):  N ?  (NEVER say yes here!)
do you want hisfile for PAW analysis (Y/N):  N ?
want to analyse new data file (Y/N):  Y ? n
Now finish HPLOT stuff
Finished plot stuff
```