Modeling of an Integrated Active Feedback Preamplifier in a 0.25 μm CMOS Technology at Cryogenic Temperatures

Shahyar Saramad, Giovanni Anelli, Matthias Bucher, Matthieu Despeisse, Pierre Jarron, Nicolas Pelloux, and Angelo Rivetti

***Abstract*—This paper describes the modeling of a standard 0.25 μm CMOS technology at cryogenic temperatures. In the first step of the work, the parameters of the EKV v2.6 model were extracted at different temperatures (300, 150, and 70 K). The extracted parameters were then used to optimize the performance of a room temperature designed active feedback front-end preamplifier (AFP) at 130 K. The results show that with a small adjustment of the extracted parameters it is possible to have a reasonable model at low temperatures. By optimizing the bias conditions at 130 K, a fall time down to 1.5 ns and a double pulse resolution of 6.5 ns were measured for NA60 proton beamscope. The proposed approach will also allow a low temperature design optimization for future projects, which will not be possible using only standard models provided by the foundry.**

***Index Terms*—Active feed-back, cryogenic temperatures, EKV model, front-end amplifier, transistor modeling.**

I. Introduction

It is well known that the performance of a silicon detector can be seriously affected if the device is used in a harsh radiation environment. For this reason, intensive research and development (R&D) efforts have been devoted to improving the radiation resistance of silicon sensors. In this framework, the R&D 39 collaboration has shown that heavily damaged detectors can be fully recovered by operating them at cryogenic temperatures (Lazarus effect) [1].

In the recent past, it has also been demonstrated that it is feasible to implement radiation-tolerant front-end electronics in commercial deep submicron CMOS technologies [2], [3]. As a consequence, a possible option for future high luminosity HEP experiments is to use cryogenically cooled detectors, readout by deep submicron CMOS ASICs. Since the front-end electronics is usually located very close to the detector and shares with it, the same cooling system, the integrated circuits designed in commercial technologies must also have a reasonable performance at low temperatures.

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TABLE I
VARIATIONS OF TRANSCONDUCTANCE PARAMETER (K_p) AT DIFFERENT TEMPERATURES

Temperature	NMOS (A/V^2)	PMOS (A/V^2)
300 K	261×10^{-6}	62×10^{-6}
150 K	741×10^{-6}	122×10^{-6}
70 K	1300×10^{-6}	177×10^{-6}

TABLE II
VARIATIONS OF THRESHOLD VOLTAGE WITH TEMPERATURE FOR LONG ($W/L = 10/5$), SHORT ($W/L = 10/0.28$), AND NARROW ($W/L = 2/20$) NMOS AND PMOS TRANSISTORS (L. = LONG, S. = SHORT, N. = NARROW)

T	20 K	70 K	150 K	300 K
L.NMOS	717 mV	715 mV	668 mV	586 mV
S.NMOS	686 mV	685 mV	652 mV	567 mV
L.PMOS$_a$	-682 mV	-643 mV	-583 mV	-479 mV
S.PMOS$_a$	-625 mV	-608 mV	-552 mV	-449 mV
L.PMOS$_b$	-727 mV	-702 mV	-662 mV	-576 mV
N.PMOS$_b$	-700 mV	-660 mV	-605 mV	-498 mV

In principle, the operation of a CMOS device at cryogenic temperatures brings some advantages, which are described in more detail in Section II of this paper. However, the design of circuits that have to work in such an environment entails also a fundamental issue. In fact, since the model parameters provided for commercial CMOS processes are not intended for use in cryogenic conditions, an additional modeling effort is necessary. This, unfortunately, adds a significant burden to the design activity. An appropriate choice of the model is therefore of crucial importance to minimize the extra work required, so the use of a model with a small number of free parameters becomes an important asset. Hence, in this study, we have preferred to use the EKV v2.6 model [4]–[6], which has fewer parameters than the more common BSIM3 counterpart.

The first step of our work has been to extract the EKV SPICE parameters at different temperatures (70 K, 150 K and 300 K). The extraction has been carried out by performing systematic measurements on test structure containing a number of NMOS and PMOS transistors with different W/L ratios [5]. This part of the work is described in Section III of the paper.

In order to verify the theoretical predictions, this model has then been used to optimize the performance of a room temperature designed front-end amplifier at 130 K, which has been manufactured and tested for CERN NA60 proton Beamscope.

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The results achieved on this prototype are discussed in Section IV. Section V draws the main conclusion of this experience.

II. CMOS Transistors at Low Temperatures

The are several advantages in operating a CMOS circuit at very low temperatures. In fact, on one hand, the carrier mobility, the metal conductivity and the latchup immunity are increased; on the other hand the subthreshold slope and the leakage currents are reduced [7]. In addition, in cryogenic conditions, the thermal noise sources become less effective and the problem of electro migration is less important. Since the thermal conductivity of silicon is found to have improvements at lower temperatures, the dissipated heat can be more easily removed from the chip and the devices could be made smaller and more highly integrated. It must be pointed out, however, that to fully exploit all these benefits, some changes to the technology are required [8]. However, in this paper we concentrate only on the cryogenic performance of a room temperature technology designed for commercial standard conditions.

A. Carrier Mobility

The mobility behavior can be described by three scattering mechanisms, which have different dependence on the temperature and on the electric field.

The first mechanism is Coulomb scattering [9], that is related to ionized impurity atoms and oxide charges. For quarter micrometer CMOS transistors, it is important at low fields even at room temperature. If the electric field increases the inversion layer charge becomes significant and tends to screen the impurities and the oxide charges. As a consequence, mobility shows an initial increase when the transverse electrical field increases. Further increase of the field will however decrease the mobility because phonon scattering will start to play an important role.

Phonon scattering is due to lattice vibrations. This effect is important at intermediate fields and is the dominant mechanism that limits the mobility at room temperature. Phonon scattering is reduced as temperature is lowered and becomes insignificant at 77 K. At this temperature, Coulomb scattering becomes dominant.

Surface roughness scattering [10] is important at high fields and like the Coulomb scattering, it is a weak function of temperature. It is negligible at room temperature but it becomes important at 77 K.

Deep submicron CMOS technologies have high substrate doping and hence relatively low mobility. The most significant advantage of low-temperature CMOS operation is therefore the increase of this parameter. By doing some measurements on single MOS transistor and extracting the transconductance parameter ($\mathrm{K_p} = \mu * \mathrm{C_{ox}}$), it is found that by decreasing the temperature from 300 to 70 K, the mobility increases by a factor of 5 for NMOS transistors and by a factor of 2.85 for PMOS transistors, as shown in Table I. The suggested empirical models for mobility at low temperatures can be found in [11].

B. Subthreshold Slope and Threshold Voltage

Another interesting effect that occurs at low temperature is the reduction of the subthreshold slope, which determines the efficiency to turn off a transistor by reducing its VGS. In principle, a steeper subthreshold slope would allow the use of smaller threshold voltages, thereby enabling the operation of the devices at a lower power supply. It is clear, however, that to exploit this advantage a special process should be designed for cryogenic conditions.

In fact, the absolute value of the threshold voltage increases as the temperature decreases for both PMOS and NMOS transistors and this limits the improvement in the current driving determined by the larger mobility.

The threshold voltage for PMOS devices increases at a faster rate than that of NMOS ones. The temperature coefficient of the threshold voltage for this technology is $+0.55$ mV/K for NMOS and -0.7 mV/K for PMOS transistors, which is in the typical range of absolute value of temperature coefficient of threshold voltage (0.5 mV/K–3 mV/K) [12]. The effect of different $\mathrm{W/L}$ ratio on experimental threshold voltage for long $(\mathrm{W/L} = 10/5)$ and short $(\mathrm{W/L} = 10/0.28)$ and narrow $(\mathrm{W/L} = 2/20)$ devices is clearly shown in Table II.

III. Model Choice and Parameters Extraction

To design circuits that have to operate at cryogenic temperatures, it is necessary to extract the SPICE parameters of the transistors. The parameters provided by the foundry are usually intended for standard conditions and cannot be used to predict in a reliable way the behavior of the circuit at very low temperatures. The temperature behavior of some parameter of BSIM3 model [13], for instance, is not so well known to allow a straightforward extension to such extreme situations. Moreover, the huge number of parameters required by this model discourages a custom extraction.

We have therefore preferred to work with the EKV model [5] because of the smaller number of needed parameters. The simplicity of the model, the continuity of the large and small signal characteristics from weak to strong inversion and the possibility of performing statistical circuit simulation including matching, are other interesting aspects of the EKV model. In EKV model all aspects regarding the static, the quasi-static, and nonquasi-static dynamic and noise models are all derived in a coherent way from a single characteristics, the normalized transconductance to current ratio.

The block diagram in Fig. 1 gives an idea of the extraction strategy, which has to be adopted for the EKV parameter extraction [5], [6]. For this purpose some measurement must be done in different suitable conditions (strong, moderate and weak inversion and also conduction and saturation regimes) for different $\mathrm{W/L}$ ratios.

In our case we have used a set of NMOS and PMOS devices having the following aspect ratio: $\mathrm{W/L} = 10/0.28, 10/1, 10/5, 2/20$. The extraction procedure has been repeated at 300, 150, and 70 K, respectively. The cooling system, the PCB and cold stage instruments used in these experiments are shown in Figs. 2 and 3. This system uses super fluid helium under pressure in a cylindrical tank, which can be used to cool the system till 1.8 K. By adjusting the position of PCB inside the tank and monitoring with a suitable thermal sensor, it is possible to stabilize the temperature at any given point with an electrical heater.

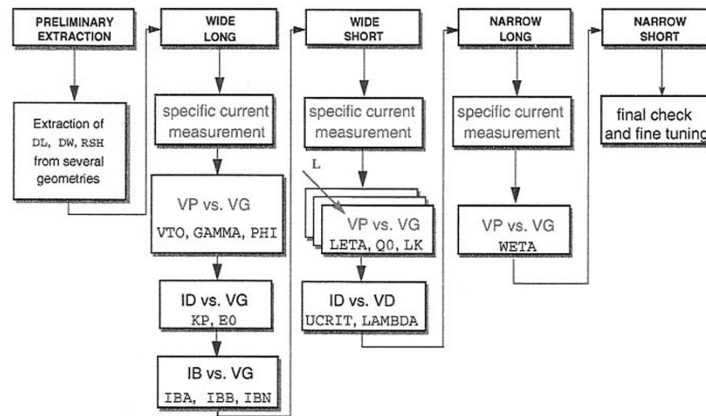

Fig. 1. EKV v2.6 parameters extraction methodology [6].

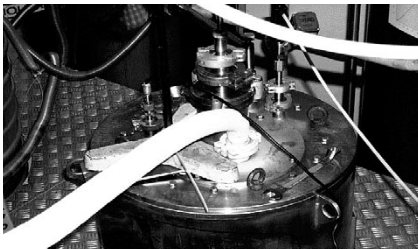

Fig. 2. Photography of cold stage for parameter extraction of EKV model.

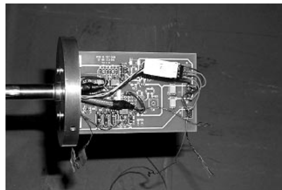

Fig. 3. Photography of PCB connected to cold stage instruments (temperature sensor, controllable heater, and especial cryogenic cables).

The EKV v2.6 model has 18 intrinsic parameters and the parameters were extracted at the temperature close to the foreseen operating condition of the circuit that must be modeled.

The parameter extraction methodology established for EKV v2.6 model is well described in [5] and will not be discussed in detail here.

For the purpose of this paper, it is sufficient to remember that the extraction of the parameters is based on nonlinear optimization algorithms, which strongly depend on the amount of data used and on the complexity of the equations to be evaluated. This may be a source of errors and if some improvement in a particular region of operation is needed the extracted parameters can be refined. The temperature dependence of some parameter is known theoretically or experimentally and this can be used as a double check to test the correctness of the extracted quantities.

The values found for the main EKV parameters are shown in Table III. Some important conclusions about the extracted parameters are summarized hereafter.

1) The lateral diffusion length correction (DL) of the source and drain junction, which is needed for extracting the effective channel length and also the total resistance of the MOS transistors is dependent on the gate voltage. For a Gaussian profile, DL, and the total resistance will decrease by decreasing temperature and both of them are less gate dependent at lower temperatures [14]. For example for PMOS transistors, DL decreases from −96 nm at 300 K to −63 nm at 150 K. The same behavior is expected for NMOS transistors.

TABLE III
IMPORTANT INTRINSIC EKV MODEL PARAMETERS

	Units	NMOS		PMOS	
T	K	300	150	300	150
LETA	-	0.14	0.15	0.10	0.09
KP	A/V^2	261μ	741μ	62μ	122μ
THETA	1/V	0.26	0.539	0.25	0.4
UCRIT	MV/m	4	1.8	25.2	10.3
LAMBDA	-	0.36	0.39	0.95	0.71
RSH	Ω/sq	609	263	124	79
GAMMA	$V^{1/2}$	0.78	0.84	0.95	0.96
PHI	V	0.91	1.29	1.22	1.45

2) The bulk Fermi potential $(2 * \mathrm{PHI})$ increases by decreasing temperature as theoretical relations predict. Increase in PHI increases the threshold voltage, as expected at cryogenic temperatures.
3) The method of extraction of threshold voltage (Fig. 4) is not very sensitive to variations of specific current $(\mathrm{I_s})$ and this sensitivity decreases with temperature (Tables IV and V). $\mathrm{I_s} = 2\mathrm{n}\beta\mathrm{U_t^2}$, where n is the weak inversion slope factor, the transconductance factor β includes mobility reduction due to the vertical field, channel length modulation and velocity saturation and $\mathrm{U_t} = \mathrm{kT/q}$. Specific current depends on the device size and is determined from the strong inversion slope of square root of Id versus $\mathrm{V_s}$ $(\mathrm{Id} = \mathrm{I_s}[(\mathrm{VP} - \mathrm{V_s})/2\mathrm{U_t}]^2)$.
4) Body factor (GAMMA) is approximately constant. Because substrate and oxide capacitance are virtually temperature independent, which is consistent with experimental data.
5) Since the mobility increases by decreasing temperature and velocity saturation (UCRIT) occurs at lower fields,

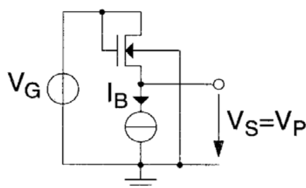

Fig. 4. Circuit for measurement of pinch-off voltage ($\mathrm{IB} = 0.7 * \mathrm{I_s}$). Threshold voltage (VTO) is measured at particular value of VG corresponding to the $\mathrm{VP} = 0$ cross point.

TABLE IV
VARIATION OF SPECIFIC CURRENT ($\mathrm{I_s}$) WITH TEMPERATURE FOR LONG ($\mathrm{W/L} = 10/5$) AND SHORT ($\mathrm{W/L} = 10/0.28$) NMOS AND PMOS TRANSISTORS (L. = LONG, S. = SHORT)

T	20 K	70 k	150 K	300 K
L.NMOS	16.5 nA	175.5 nA	499.3 nA	751.8 nA
S.NMOS	0.213 µA	2.2 µA	6.8 µA	13 µA
L.PMOS	3.4 nA	28.2 nA	85.6 nA	186.5 nA
S.PMOS	0.071 µA	0.684µA	2.1 µA	4.8 µA

TABLE V
EXTRACTED VALUES OF VTO AND VARIATIONS FOR CHANGES OF IB WITH RESPECT TO ITS NOMINAL VALUE (BOLD) FOR LONG ($\mathrm{W/L} = 10/5$) AND SHORT ($\mathrm{W/L} = 10/0.28$) NMOS AND PMOS TRANSISTORS (L.N. = LONG NMOS, S.N. = SHORT NMOS, L.P. = LONG PMOS, S.P. = SHORT PMOS)

	T (K)	0.5×Is	0.6×Is	**0.7×Is**	0.8×Is	0.9×Is
VTO (mV) L.N.	20	715	716	717	717	718
	70	708	710	715	716	718
	150	658	662	668	670	673
	300	570	578	586	593	597
VTO (mV) S.N.	20	684	685	686	687	688
	70	680	683	685	687	690
	150	642	647	652	655	658
	300	552	560	567	575	580
VTO (mV) L.P.	20	-680	-681	-682	-685	-686
	70	-638	-641	-643	-645	-647
	150	-575	-578	-583	-587	-590
	300	-465	-472	-479	-485	-492
VTO (mV) S.P.	20	-622	-623	-625	-627	-627
	70	-602	-605	-608	-610	-612
	150	-545	-548	-552	-557	-560
	300	-436	-442	-449	-455	-460

the energy of the carriers may exceed the lattice thermal energy. In addition, the effect of vertical electric field (THETA) increases by decreasing temperature, so impact ionization (hot carrier effect) will be more important at low temperatures.

6) Short channel effect factor (LETA) is temperature independent both for NMOS and PMOS. For channel length modulation factor (LAMBDA) only for PMOS transistors the temperature dependence is seen. For these results we think that more experimental data are needed to fully understand this behavior.

As can be seen in Figs. 5–10, the EKV model simulation provide good descriptions of both PMOS and NMOS transistors at 300 and at 150 K, and of PMOS transistors at 70 K. However,

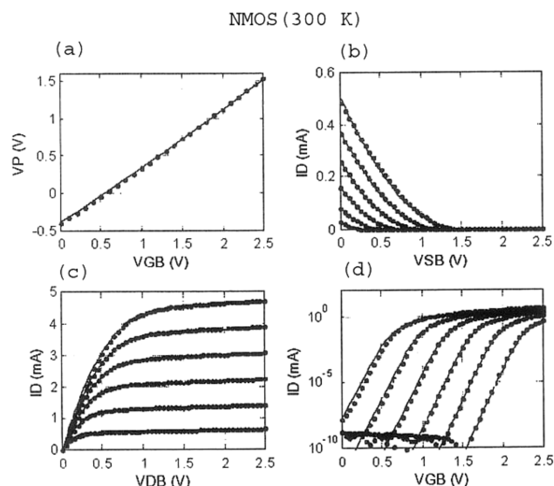

Fig. 5. (a) Variations of VP versus VGB ($\mathrm{W/L} = 10/0.28$), (b) ID-VSB for $\mathrm{VGB} = 1$–2.5 V step 0.3 V ($\mathrm{W/L} = 10/5$), (c) ID-VDB for $\mathrm{VGB} = 1$–2.5 V step 0.3 V and $\mathrm{VSB} = 0 (\mathrm{W/L} = 10/0.28)$, (d) ID-VGB and $\mathrm{VSB} = 0$–1.25 V step 0.25 V ($\mathrm{W/L} = 10/0.28$) at $\mathrm{T} = 300$ K for NMOS transistors (``o'' = measured, ``_'' = simulation).

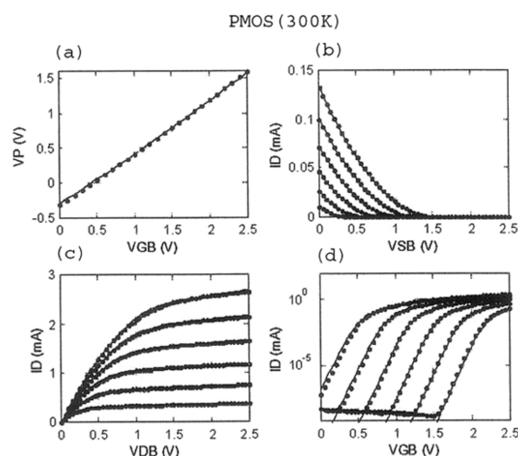

Fig. 6. (a)Variations of VP versus VGB ($\mathrm{W/L} = 10/0.28$), (b) ID-VSB for $\mathrm{VGB} = 1$–2.5 V step 0.3 V ($\mathrm{W/L} = 10/5$), (c) ID-VDB for $\mathrm{VGB} = 1$–2.5 V step 0.3 V and $\mathrm{VSB} = 0$ ($\mathrm{W/L} = 10/0.28$),(d) ID-VGB for $\mathrm{VSB} = 0$–1.25 V step 0.25 V ($\mathrm{W/L} = 10/0.28$) at $\mathrm{T} = 300$ K for PMOS transistors (``o'' = measured, ``_'' = simulation and all the voltages are considered with negative sign in PMOS characteristics).

the model does not accurately simulate NMOS characteristics at 70 K. This discrepancy is probably due to impact ionization.

Using experimental measurements and two-dimensional numerical simulation, it is shown that the impact of channel potential gradient on transconductance (gm) becomes significant for deep submicron MOS transistors at low temperatures. Up to now, the increase of gm was mainly ascribed to the mobility or velocity enhancement at low temperatures, but the increase of channel potential gradient can also leads to larger gm enhancement for short channel devices, which must be considered for more accurate modeling.

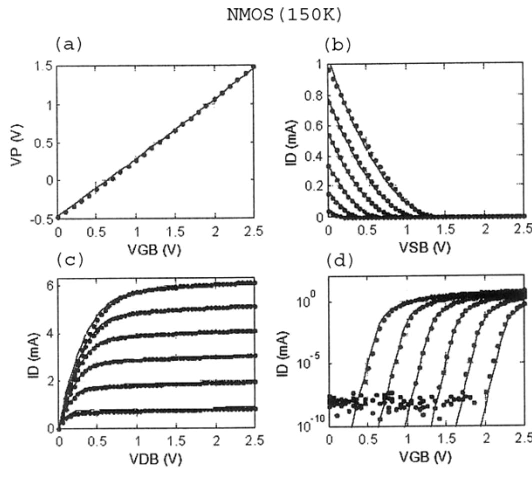

Fig. 7. (a) Variations of VP versus VGB $(\mathrm{W/L} = 10/0.28)$, (b) ID-VSB for $\mathrm{VGB} = 1$–2.5 V step 0.3 V $(\mathrm{W/L} = 10/5)$, (c) ID-VDB for $\mathrm{VGB} = 1$–2.5 V step 0.3 V and $\mathrm{VSB} = 0(\mathrm{W/L} = 10/0.28)$, (d) ID-VGB and $\mathrm{VSB} = 0$–1.25 V step 0.25 V $(\mathrm{W/L} = 10/0.28)$ at $\mathrm{T} = 150$ K for NMOS transistors (``o'' = measured, ``-'' = simulation).

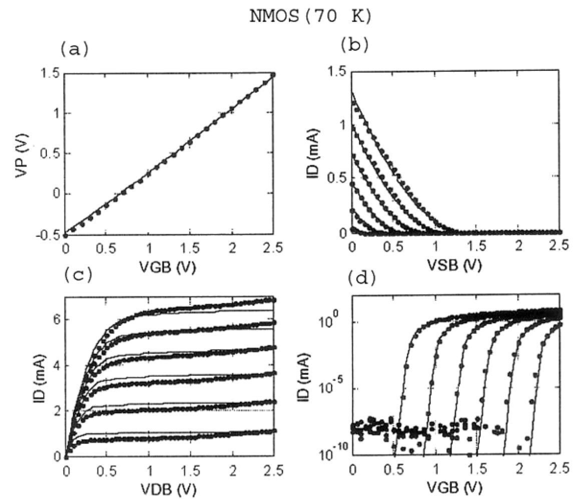

Fig. 9. (a) Variations of VP versus VGB $(\mathrm{W/L} = 10/0.28)$, (b) ID-VSB for $\mathrm{VGB} = 1$–2.5 V step 0.3 V $(\mathrm{W/L} = 10/5)$, (c) ID-VDB for $\mathrm{VGB} = 1$–2.5 V step 0.3 V and $\mathrm{VSB} = 0(\mathrm{W/L} = 10/0.28)$, (d) ID-VGB and $\mathrm{VSB} = 0$–1.25 V step 0.25 V $(\mathrm{W/L} = 10/0.28)$ at $\mathrm{T} = 70$ K for NMOS transistors (``o'' = measured, ``-'' = simulation).

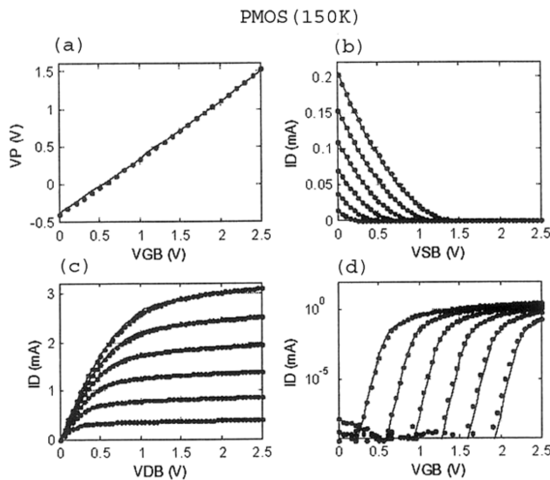

Fig. 8. (a) Variations of VP versus VGB $(\mathrm{W/L} = 10/0.28)$, (b) ID-VSB for $\mathrm{VGB} = 1$–2.5 V step 0.3 V $(\mathrm{W/L} = 10/5)$, (c) ID-VDB for $\mathrm{VGB} = 1$–2.5 V step 0.3 V and $\mathrm{VSB} = 0(\mathrm{W/L} = 10/0.28)$, (d) ID-VGB for $\mathrm{VSB} = 0$–1.25 V step 0.25 V $(\mathrm{W/L} = 10/0.28)$ at $\mathrm{T} = 150$ K for PMOS transistors (``o'' = measured, ``-'' = simulation and all the voltages are considered with negative sign in PMOS characteristics).

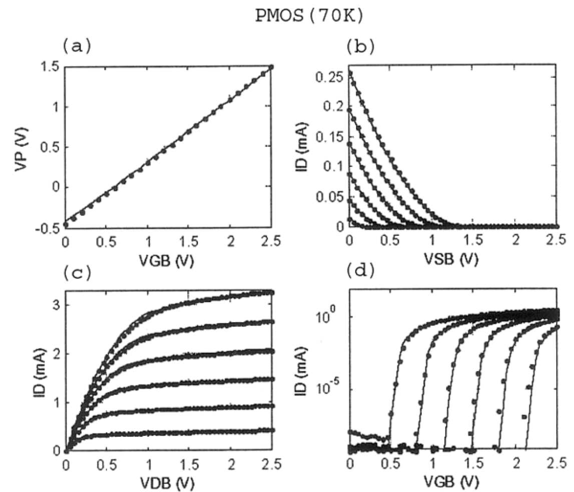

Fig. 10. (a) Variations of VP versus VGB $(\mathrm{W/L} = 10/0.28)$, (b) ID-VSB for $\mathrm{VGB} = 1$–2.5 V step 0.3 V $(\mathrm{W/L} = 10/5)$, (c) ID-VDB for $\mathrm{VGB} = 1$–2.5 V step 0.3 V and $\mathrm{VSB} = 0(\mathrm{W/L} = 10/0.28)$, (d) ID-VGB for $\mathrm{VSB} = 0$–1.25 V step 0.25 V $(\mathrm{W/L} = 10/0.28)$ at $\mathrm{T} = 70$ K for PMOS transistors (``o'' = measured, ``-'' = simulation and all the voltages are considered with negative sign in PMOS characteristics).

IV. Optimizing the Peformance of the AFP Chip by Presented Model

The second step of our work was the modeling of a front-end amplifier using the extracted EKV parameters. We have chosen, as a test vehicle, the active feedback preamplifier (AFP) described in [15], although in future we plan to do such measurements with a different configuration, to prove further the correctness of our modeling. The circuit, shown in Fig. 11 is a transimpedance amplifier in which the feedback element is implemented by a MOS transistor biased in weak inversion and operating in saturation. The transimpedance gain is $1/\mathrm{gmf}$, where gmf is the transconductance of the feedback device and can be adjusted by the current source $\mathrm{I_{FEED}}$.

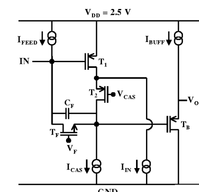

Fig. 11. Schematic of the AFP circuit.

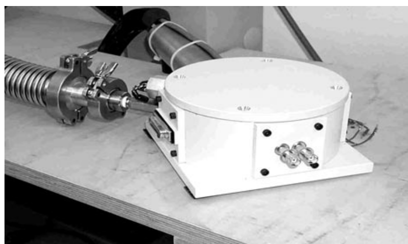

Fig. 12. Photography of cold stage and vacuum chamber for testing the AFP chip.

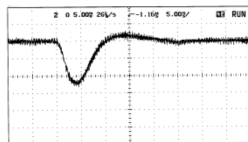

Fig. 13. Experimental response of AFP chip for 4 fC input signal with $I_{FEED} = 250$ nA at 130 K. Horizontal scale was 5 nS/div and vertical scale was 5 mV/div.

A key advantage of this design for our study is that it implements in a single stage a second order transfer function without requiring critical passive components. The only passive device is C_F, obtained as parasitic capacitors between two layers of metal. The core amplifier is a single ended cascode, whereas the output is buffered by a simple PMOS source follower.

All the current of current mirrors $I_{FEED}, I_{CAS}, I_{IN}$ and I_{BUF} and also V_F, V_{CAS} have their reference outside the chip. This is exploited for changing the bias points, optimizing the performance of the chip and controlling the stability of the circuit at low temperature. The cooling system, which consist of a vacuum chamber and a compressor module is shown in Fig. 12.

For accurate simulation, the input and output capacitance of the preamplifier must be considered and the parasitic contributions from the detector, the PCB tracks, the bonding wires and the test instruments must be considered. Since in this configuration the output response is expected to be very sensitive especially to the input capacitance of the amplifier, for a reasonable simulation accurate information about the total input capacitance is necessary. The input capacitance was estimated by matching the simulated and experimental fall time and gain at room temperature.

In addition, because of mismatches between the parameters of single transistors and the integrated ones, the threshold voltage and mobility were adjusted (with 20% variation) for the best dc matching between experimental and modeling results for a given bias point.

The measured output pulse of this preamplifier at 130 K with a feed-back current of 250 nA, an input capacitance of 4 pF and a 50 Ω output load connected via a decoupling capacitor is shown in Fig. 13. The amplitude and the fall time of the signal are consistent with the EKV model predictions (Table VI). Although the gain and fall time are in good agreement, the overshoot of the simulation is higher than the experimental one. In order to understand if this can be attributed to some inaccuracy in the extracted model parameters, we have performed several simulations. In each simulation, the value of some critical parameter was changed, in an attempt to reproduce the experimental data.

TABLE VI
MEASURED AND SIMULATION AMPLITUDE AND FALL TIMES WITH DIFFERENT FEEDBACK CURRENTS AT 130 K

I_{feed} [nA]	Exp. Amplitude [mV/fC]	Sim. Amplitude [mV/fC]	Exp. Fall time [ns]	Sim. Fall time [ns]
79	3.75	3.6	2.5	2.4
250	2.9	2.9	2	2
500	2.5	2.45	1.8	1.85
876	2.25	2.15	1.5	1.6

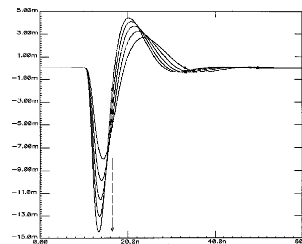

Fig. 14. Simulation of the transient response of the AFP chips with $\pm 35\%$ variation of K_p of the PMOS transistors at 130 K. The direction of arrow shows the increase of mobility and the middle response has the same condition of the experimental output shown in Fig. 13.

Fig. 14 shows, for instance, the effect of the variations of mobility for PMOS transistors on the performance of the AFP chip. The direction of the arrow in the figure indicates the increase of mobility. It is clear from this figure that increasing the mobility will decrease the fall time and increase the gain of the preamplifier. However, also the overshoot of the output will increase. In Fig. 14, the middle response is in the same bias condition as the experimental result, shown in Fig. 13.

The same strategy has been applied for the other parameters. We have seen that, for instance, the variation of Kp for NMOS transistors has not important effects on the gain, but it makes small improvements in the fall time. By changing the threshold voltage of the NMOS transistors in the range of ± 60 mV, a small variation of fall time is seen. For PMOS transistors this effect is negligible.

The discrepancy between the experimental and the simulated pulse shape cannot therefore be explained just by a "fine tuning" of the extracted parameters. At the time of writing there is not conclusive evidence if this disagreement has to be ascribed to some physical effect not adequately modeled or to some contribution of the external environment, which has not been taken properly into account.

Despite these difficulties, the modeling effort with EKV has allowed a fairly good optimization of the circuit at 130 K, which would have not been possible using only the models provided by the foundry. This model can also be used for low temperature design optimization in future projects.

Concerning the noise, no improvement was seen at low temperatures. Actually, at 130 K a moderate degradation (10%) in noise performance was observed. This measurement has been repeated several times with different cooler setups, finding always coherent results. The worsening of the noise figure could be explained with hot carrier effects, which may become more severe at the lower temperatures.

V. Conclusion

The use of a standard CMOS technology to design circuits that have to operate at cryogenic temperatures requires a dedicated modeling. In this paper, the strategy for modeling a 0.25 μm CMOS technology at cryogenic temperatures has been presented.

In the first phase of the study the parameters of the EKV model have been extracted by measuring individual transistors. These parameters have then been used to model a front-end amplifier and to optimize its performance at 130 K. The agreement between the gain and the fall time of the circuit calculated with SPICE and the ones found in the experimental measurements is excellent. However, some discrepancy between the pulse shapes has been observed. In particular, in the computer simulation the phase margin of the circuit is clearly underestimated and an overshoot bigger than the one observed is predicted. This effect cannot be explained with a simple adjustment of the extracted parameters. Despite this difficulty, the overall agreement between simulation and results is acceptable and the proposed approach will allow a design optimization, which will not have been possible using only the standard model provided by the foundry.

Amongst other applications, the designed chip has been used to read out the microstrip detectors of the NA60 beam hodoscope. For the optimal bias condition the fall time reduced from 3 ns at room temperature to 1.5 ns at 130 K with ENC around 350 electrons rms for an input capacitance of 4 pF. When the sensors and the ASICs were cooled down at 130 K a double pulse resolution of 6.5 ns has been observed [16]. As expected this proton Beamscope, which is tested in fall 2001 after total fluence of 10^{14} protons per cm^2 did not show any degradation in the performance.

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