System Level Radiation Validation Studies for the CMS HCAL Front-End Electronics

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Abstract

Over a 10 year operating period, the CMS Hadron Calorimeter (HCAL) detector will be exposed to radiation fields of approximately 1 kRad of total ionizing dose (TID) and a neutron fluence of 4E11 n/cm^2. All front-end electronics must be qualified to survive this radiation environment with no degradation in performance. In addition, digital components in this environment can experience single-event upset (SEU) and single-event latch-up (SEL). A measurement of these single-event effects (SEE) for all components is necessary in order to understand the level that will be encountered. System level studies of the performance of the front-end boards in a 200 MeV proton beam are presented. Limits on the latch-up immunity along with the expected SEU rate for the full front-end system have been measured. The first results from studies of the performance of the two Fermilab custom-designed chips in a radiation environment also are shown.

I. THE CMS HCAL RADIATION ENVIRONMENT

The CMS experiment is scheduled to run for 10 years. During this period, some detector elements will be irradiated with a total ionizing dose (TID) above 10 MRad and a neutron fluence in excess of 1E15 n/cm^2. However, the HCAL detector will see a much smaller dose. The highest doses that sections of the HCAL detector will see are a total ionizing dose of 330 rads and a neutron flux of 1.3E11 n/cm^2 [1,2]. Since these estimates have uncertainties on the order of a factor of three and do not include any safety factor, the total dose studies performed probed fluences of 5E11 n/cm^2 and over 1 kRad. High energy neutrons that interact in the silicon are expected to produce SEE such as SEU or SEL. The level expected for these type of events, determined by the fluence of neutrons with energy greater than 20MeV, is ~1E11 n/cm2 after taking into account the additional factor of three uncertainty. A SEU is defined as a non-destructive event that causes a flip-flop to change state. A SEL is a potentially catastrophic event resulting from triggering a silicon controlled rectifier (SCR) formed from the parasitics of the bulk silicon.

The HCAL detector [3] is a sampling calorimeter of brass absorber and scintillating tile with embedded fiber readout. The front-end electronics chain [4] is shown in Figure 1. A hybrid photo-diode (HPD) [5] converts light into current that is presented to a multi-ranging ADC (the QIE - Charge Integrating and Encoding ASIC) [6,7,8] running at 40 MHz. The QIE is a floating-point ADC, with 4 ranges and 5 piece-wise linear sensitivities per range. In normal operation, the lowest range has 1fC/ct, 2fC/ct,…,5fC/ct. Each subsequent range is five times less sensitive, such that the most sensitive region of the lowest range (range 0) is 1fC/ct, range 1 is 5fC/ct, range 2 is 25fC/ct and range 3 is 125fC/ct. The QIE also has a "calibration" mode, used for source calibration of the detector, that allows the QIE sensitivity to be increased to 1/3fC/ct. The QIE functions (integration, range selection, multiplexing of capacitor charge, and reset) are pipelined, with 4 capacitors per range needed to achieve dead-timeless integration. The input of the QIE is "pseudo-differential," with signal and reference inputs for noise cancellation, and parallel capacitor banks for the reference circuit. Unlike earlier versions of the QIE [9] where a commercial FADC was used to digitize a voltage output from the QIE, in this
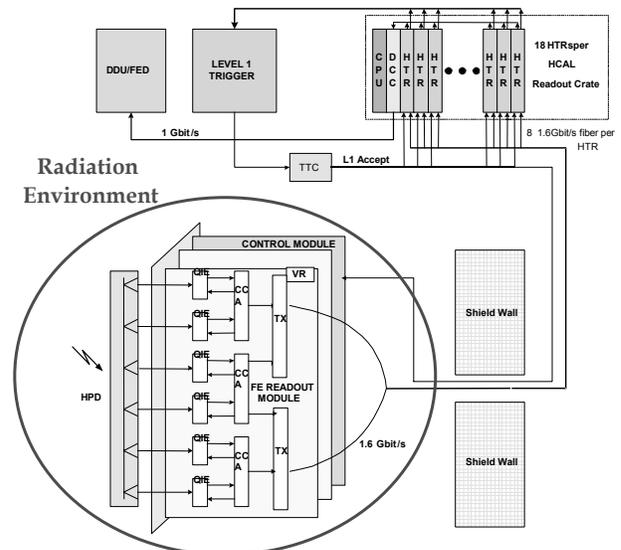

Figure 1: HCAL Front-End Electronics Schematic. TX represents the Gigabit Optical Link and the VCSEL.

version the ADC is incorporated on the device. For each 25ns clock cycle, nine bits of data (5 mantissa, 2 exponent, and 2 capacitor identification bits) are produced and sent to the CCA (Channel Control ASIC) [10]. The CCA provides clocks to the QIE and synchronizes and monitors data from two QIEs. The GOL (Gigabit Optical Link) performs a parallel-to-serial conversion and drives data from three QIEs to a commercial Vertical Cavity Surface Emitting Laser (VCSEL). The data is then optically transmitted out of the radiation area at 1.6 Gbps to the HCAL trigger and readout boards (HTR).

A picture of a prototype 6-channel front-end board is shown in Figure 2. The major components of the 6-channel board are (from left to right) six QIEs, three CCAs, two GOL transmitters, two low voltage regulators, and two VCSELS (mounted on the back side of the board). In addition to the front-end boards, Clock Control Monitoring (CCM) modules distribute clocks to the front-end boards, monitor temperatures and low voltages, and provide slow control communication paths for downloading control registers.

The QIE and CCA are Fermilab designed ASICs. The QIE is fabricated in the Austria Micro Systems (AMS) 0.8μm BiCMOS process. The CCA is fabricated in the Agilent (formerly HP) 0.5 μm micron bulk-CMOS process. The QIE has bipolar and MOS transistors, while the CCA uses only MOS. Bipolar transistors in the AMS process have been studied previously [11], and circuits have been proven tolerant up to an ionizing dose of ~10 MRad. Studies of SEU susceptibility and displacement damage effects for test shift registers in both the AMS and Agilent processes have been reported on previously [12]. This report focuses on the SEL immunity of the CCM module and the performance in a radiation environment of the 6-channel front-end board with production-version ASICs.
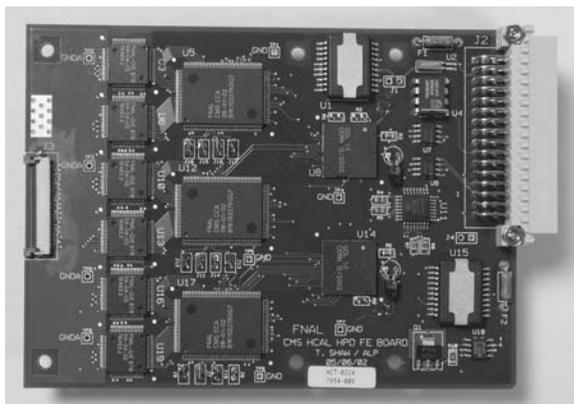

Figure 2: HCAL Six Channel Front-End P.C. Board.

II. RADIATION FACILITY AND PROCEDURE

The radiation effects studies reported here were performed using the Indiana University Cyclotron Facility's (IUCF) 200 MeV proton beam in Bloomington, Indiana. The IUCF was selected because the proton beam is energetic enough to induce SEU and SEL events while delivering tolerable ionizing doses to the devices under study. A full description of the IUCF facility can be found in reference [13].

Front-end boards (8.85 cm x 12 cm) were placed at the end of the beam line and were illuminated with a 7 cm diameter beam spot (See Fig. 3). Because the boards were too large to be fully illuminated and since the GOL and LV regulators were developed to be radiation tolerant, the beam spot was focused on the QIE and the CCA section of the card. The clocking and controlling of the front-end board was achieved with a CCM module, which was kept out of the beam and shielded by Pb bricks. Approximately 25 feet away and behind a shielding wall were power supplies that could be monitored for over-currents from SEL and were controlled remotely by a PC. A data acquisition system developed for HCAL beam tests was used to record data from the front-end boards and sense errors such as synchronization problems [14]. Data were taken with either one or three boards in the beam, corresponding to 6 or 18 QIE channels, respectively. Each QIE produced nine bits of data per 25 ns clock cycle. Data from three QIEs were digitally combined, converted from parallel to serial data in the GOL and were optically transmitted by the VCSELs at 1.6 Gbps to VME based HTR boards, which have the capacity of buffering data from 24 channels (8 fibers). The data were then transferred to a Data
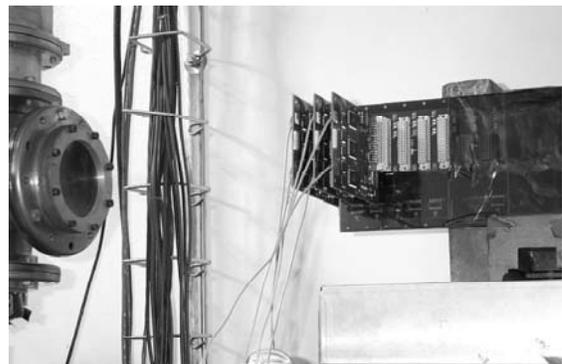

Figure 3: Three front-end boards in the IUCF beam line.

Concentrator Card (DCC) upon a Level-1 Accept. The DCC collects data from up to 18 HTR boards and transmits events to a PC via VME readout. The system triggering was random, with an average event rate of ~125 Hz which was limited by the VME single-word transmission rate. In CMS, the DCC will transmit the data via 64-bit SLINK. The VME crate and the DAQ PCs were located out of the radiation zone at the experimenter's hut, approximately 75 feet from the boards in the beam. Twenty time slices per event per QIE channel were recorded by the DAQ and were used for SEU studies.

III. SEL STUDIES OF THE 6-CHANNEL BOARD

In order to determine SEU and SEL probabilities with adequate statistics, front-end boards were irradiated to levels much higher than the neutron fluence expected for 10 years of operation. The SEE probabilities were assessed using the number of SEE occurrences per proton times the neutron equivalency factor for the predicted energy spectrum. The expected SEE rate in the HCAL system was determined via the customary formula [(# SEE/board)/fluence x (1E11 n/cm^2/10yr) x # boards], where the number of boards in the system is ~1650 front-end boards and ~130 CCM modules. In the case of SEL, where an incidence can damage electronic components, high exposures over many boards were needed to achieve conservative SEL limits. The front-end board currents on the 6.5V supply were seen to slowly increase due to ionizing radiation affecting the digital sections of the QIEs. This phenomenon was seen in chip level studies of AMS shift registers. The current for the 5V supply that provided power to the other digital chips in the system held steady. In our board level studies, no SEL events were detected and a limit of less than one radiation induced failure per 10 year interval is expected for the system.

IV. SEU STUDIES OF THE 6-CHANNEL BOARD

Several different types of data runs were taken to study single event effects. The boards that were studied were in "inverting mode," i.e. set up for a positive signal from an HPD. The QIE also has a "non-inverting mode" that is used for PMT inputs. In these radiation studies, HPDs were not attached to the cards, leaving the input open. This was done to minimize noise and to simplify testing. set Each set of new boards underwent an initial run without beam to confirm pedestal stability of the channels. Typical pedestal RMS was 0.3ct. The boards were then exposed to the beam. The proton beam intensity was selected so that a statistically significant number of single event upsets could be observed; a typical flux was ~5E9 p/(cm^2-s). The
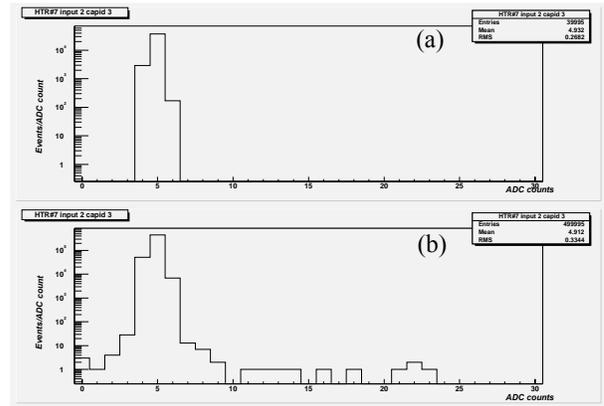
Figure 4: Pedestal reading for one capacitor of a single channel (a) without any beam, (b) with beam. Note: y-axis is a log-scale.

system triggering was random, at ~1% of the trigger rate expected in the experiment. During data taking, pedestals and board currents were monitored. Pedestal distributions during beam exposure showed wide non-Gaussian tails (See Fig. 4). Single event upset events were distinguished by one bit flip per digitization cycle (25ns time slice) of either the mantissa or range data. Analysis of individual events from the tails of the pedestal distribution revealed that the majority of these events were due to pulses in the QIE that span multiple time slices and were consistent with charge deposition before the splitter section of the QIE. In addition to events with positive pulses (similar to events that would be seen from an HPD) , negative signals were found that were consistent with charge being deposited on the reference input of the QIE, thus explaining the events below pedestal in Fig 4(b). Single time slice events were seen, but few events were consistent with a single bit being flipped in the mantissa or range. These events are most likely from protons interacting in the QIE silicon after the splitter and amplifier area of the chip. The charge is then
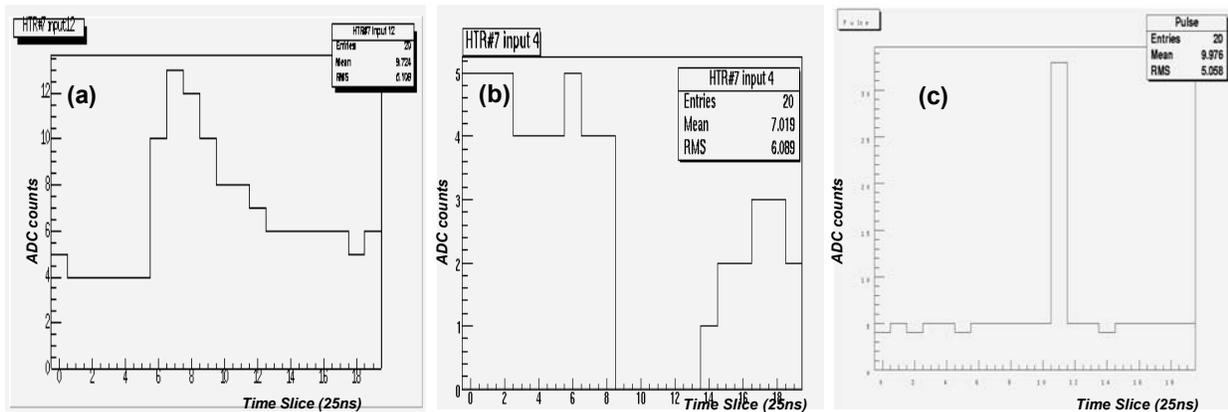
Figure 5: QIE beam event pathologies: (a) pulse in the signal input before the splitter, (b) pulse in reference input before the splitter, (c) pulse in signal capacitor after the splitter.

integrated on a single capacitor of a range, which is then reset. Figure 5 shows the pathology of events seen in the tails of the QIE pedestal distribution.

The charge spectrum of events is shown in Fig 6. Because the pulses typically spanned ~10 time slices but were coming randomly in the time window (a feature of a non-triggered system), a sum of all 20 pedestal subtracted time slices was used to represent the total charge in the event. The majority of events were minimum ionizing (MIP) protons passing through the silicon. The highest energy events seen were 250-500 fC. An extensive study [15] of HPDs (200 μm thick) in a 200 MeV proton beam revealed that minimum ionizing events deposit ~48k electrons (~8 fC), while high energy events from nuclear interactions in the silicon can extend to ~1pC. The contribution from these inelastic nuclear reactions is small (~1%). In the case of the interactions in the HPD, the silicon thickness and pixel area are precisely known. In the QIE, however, it is difficult to estimate and predict the expected charge deposition because there is a large uncertainty in knowing the active volume that would be involved. A rough estimate of the rate of high energy events from the test beam data indicates an expected rate of ~20 events/QIE/year. So although the measurements are not extremely precise, it is safe to conclude that the rate of these events should be less than that expected from the HPDs. The impact on physics from the interactions in the QIE is negligible, since they can be easily identified by looking for charge deposition in a single channel not correlated to other sub-detectors, and by examining the time profile of these events, which have a much slower time constant than events from the detector.
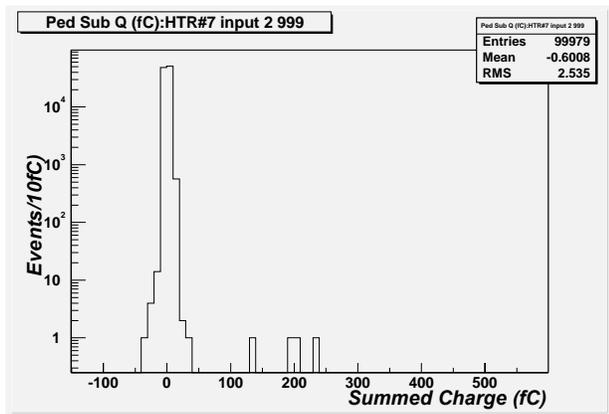

Figure 6: Charge spectrum (fC) of events with the QIE in a 200 MeV proton beam. Entries are pedestal subtracted sums of 20 time slices. The plot represents a fluence of 1E12 p/cm^2.

In order to study "true" SEU, several runs were taken with the QIEs in "forced range" mode; forced range selection allows the QIE to be put into a less sensitive range. Consequently, proton interactions that resulted in the non-Gaussian tails in the pedestal distribution seen in Fig 4(b), have too small a charge deposition to cause the pedestal to deviate on the more coarse upper ranges. The data taken from these special runs were analysed for events +/- 3ct from the mean. No SEU events were seen over a fluence of 5.8E13 protons/cm^2, giving a limit on the cross-section of 1.7E-14 cm^2 for the QIE. After taking into account the data acquisition triggering rate relative to that expected in the experiment, a cross-section limit of 1.7E-12cm^2 was determined, corresponding to an expected SEU rate in the experiment (over ~1650 front-end boards) of less than 21.8 SEU/yr or 0.8 SEU every 2 weeks. Our previous studies using shift registers from the AMS process yielded a cross-section of (0.24-0.49)E-14 cm^2 for SEU tolerant cell designs and (0.6-1.2)E-13 cm^2 for cells of nominal size. But the number of cells in the QIE is quite small (~15 cells of nominal transistor size and one critical cell that was made SEU tolerant [16] because it involved the QIE ring-counter). The CCA is not expected to contribute any upsets because all registers were designed with SEU tolerant flip-flops. Thus the number of expected upsets due to the QIE from test register studies is 15-30 SEU/yr or ~1 SEU/2-weeks for the system, which is consistent with the limit set with the front-end boards.

V. SEU AND SEL STUDIES OF THE CCM

Preliminary studies of beam induced SEU in the A54SX72A Actel FPGAs that are used on the CCM modules have been conducted at the IUCF [17]. These FPGAs are used to download information via the slow data path. Two different configurations have been tested, one having FPGAs set up as a 2012-bit shift registers and the other having FPGAs as 670-bit shift registers implementing Triple Module Redundancy (TMR). During irradiation, data words were continuously written to and read from the FPGA registers while the devices were monitored for SEU and SEL. In the registers without TMR, SEUs were observed at an average of ~60 SEU per 2012 cells per 2E12 p/cm^2, indicating a cross-section of 1.51E-14 cm^2. Consequently, the expected rate in system with FPGAs without TMR is ~1 SEU/week for the ~130 module system. There were no SEUs seen in the eight registers with TMR over 4.7E12 p/cm^2, leading to a limit on the cross-section of 3.15E-16 cm^2 per cell and a SEU limit of less than 1 SEU/28.5yrs of operation for a system with FPGAs with TMR fully configured. In the final design, however, space limitations in the FPGA necessitate that only critical functions of the FPGA have TMR implemented.

In the case of the SEL, a study was performed in which one set of modules was exposed to 25 times the fluence (2.5E12 p/cm^2) expected for 1 board over 10yrs of operation. No SELs were observed and a SEL limit of less than 1 SEL per CCM module per 2 years of operation for the ~130 module system was achieved. Previous studies of individual components on the CCMs have set a more stringent SEL failure limit of less than 1 CCM module failure in the system expected per 4 years of operation.

Additional studies are planned for Spring 2004 using approximately 5 more CCMs to try to achieve a limit of no failures in the system over 10 years of operation.

VI. SUMMARY

All components of the HCAL front-end electronics have been proven to operate up to expected radiation levels of $4E11$ n/cm^2 and 1 kRad. Additional component studies of destructive events such as SEL have shown that chosen devices are immune to SEL during a 4 year operating period. A limit on SEU rates of less than 0.8 SEU every 2 weeks has been set for the ~1650 6-channel front-end board system, which is consistent with the rate predicted from previous test-register studies. A limit on SEL failures in the 6-channel board system of less than one failure per 10 years of operation has been demonstrated. In the CCM, SEU rates will depend on the final configuration of the FPGA and is highly dependent on TMR implementation. Without TMR, the maximum expected SEU rate is ~1 SEU/week for the ~130 module system. A CCM module system test using a single module achieved a limit of less than 1 SEL per CCM per 2 years of operation for the ~130 module system. Further SEU/SEL studies using production CCMs will be conducted in Spring 2004, with a goal of achieving a limit of less than 1 SEL per CCM module per 10 years of operation for the system and of measuring the SEU rate in the final FPGA configuration.

VII. ACKNOWLEDGEMENTS

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