

The OTIS TDC Chip for LHCb Outer Tracker Readout

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Abstract

OTIS¹ is a 32 channel TDC² chip developed at the University of Heidelberg. It will be used for the readout of the Outer Tracker detector in the LHCb Experiment. It features radiation hard layout techniques and is implemented in commercial 0.25 μm technology. The first full-scale prototype OTIS 1.0 has been submitted for manufacturing in April 2002.

The TDC itself is based on a clock driven architecture and uses a DLL³ as time reference. Each channel's drift time data is written to a ring buffer to cover the trigger latency, after which the data is either transferred to the derandomiser FiFo or overwritten. The buffer management as well as the trigger handling, data formatting and transmission to the subsequent DAQ stages is accomplished by a control circuit.

Within the scope of this paper, measurement results and modifications leading to OTIS 1.1, the next version of the chip, are presented.

I. LHCb OUTER TRACKER FRONT END ELECTRONICS

The outer tracker detector of the LHCb experiment consists of $\approx 50\,000$ straw tubes, whose anode wires are read out with ASDblr[1] chips. Being amplified and discriminated by 4 ASD chips, the signals of 32 channels connect to one OTIS chip for drift time measurement. The OTIS chip stores the drift times of all 32 channels relative to the 40 MHz LHC clock in an intermediate memory to cover the L0 trigger latency. Upon a trigger, the corresponding data is retrieved from the memory, formatted and transmitted to the next DAQ stage. Operating synchronous to the 40 MHz LHC clock, the 8 bit parallel ports of 4 OTIS chips can connect to the 32 bit wide input of the subsequent GOL[2] chip. The latter serialises the data and

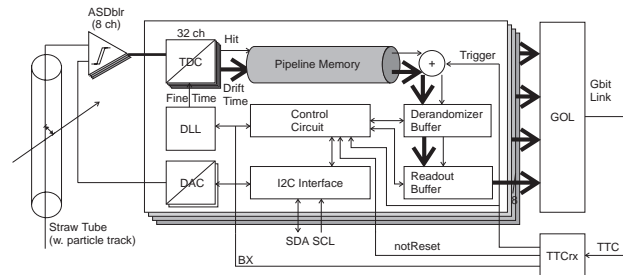


Figure 1: Schematic representation of the frontend electronics in the LHCb outer tracker.

drives it off the detector via an optical transmitter. The schema of the LHCb outer tracker DAQ is shown in fig. 1.

II. CHIP ARCHITECTURE

The OTIS chip consists of three main components:

- The TDC core with pre-pipeline register
- The pipeline memory with derandomiser buffer
- The control algorithm and slow control circuit

A general overview, which shows the relation of the different building blocks of the OTIS chip is given in fig. 2.

A. The TDC core

The TDC core comprises of a 64stage DLL used as a time reference, the hit register and the decoder circuit. The 40 MHz LHC bunch crossing clock is delayed by the DLL's chain of 64 starved inverters and subsequently compared to the original clock signal by a phase decoder. The latter steers a charge pump, which in turn adjusts the delay of the DLL to exactly 1 clock cycle. This determines the TDC's intrinsic resolution of $\frac{25\text{ns}}{64} = 390\text{ps}$. The 64 fine time signals tapped from the DLL are used to clock the hit register, thus forming the clock driven architecture of the TDC. The subsequent decoder converts the hit position to a binary representation. It is split into two halves which are used

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¹Outer Tracker Time Information System

²Time to Digital Converter

³Delay locked Loop

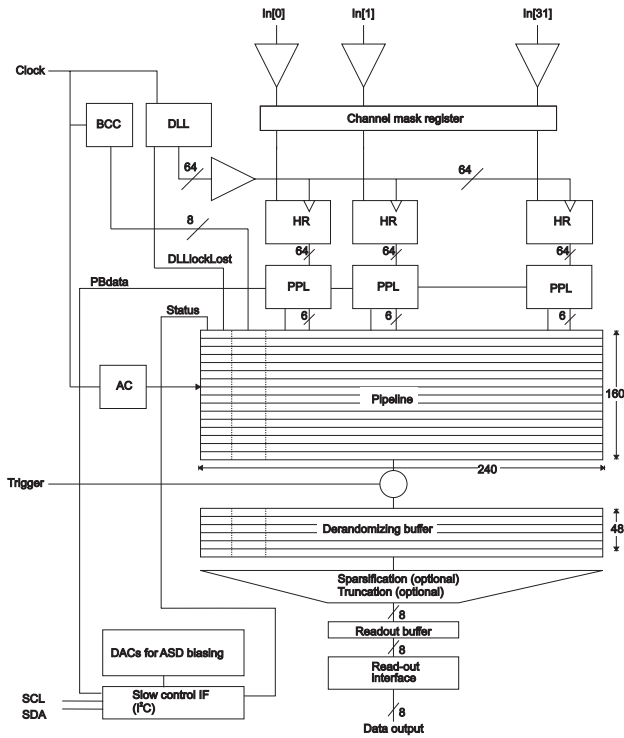


Figure 2: Block schematic showing the relation of the OTIS chip's basic building blocks.

interleavedly to maintain the dead-time free operation required by LHCb. It consists of a diode matrix, since an implementation with standard cells would require ≈ 64000 gates and considerably increase the chip size. Besides a 5 bit drift time information, each decoder half also provides a *hit bit*, indicating the recognition of a hit in the corresponding half of the decoder. The output signals of the first half are latched during the second half of a bunch crossing clock cycle, preserving this information for final processing in the first half of the next clock cycle. The outputs of the second decoder half are stable during the first half of the next clock cycle and thus are not latched, except for the *hit bit*. The so called *priority encoder* uses the *hit bits* of the two decoder halves together with the original hit input. This encoder determines the half, that contained the first hit, or selects the second half, if no hit was found. The actual selection is performed by a multiplexer, which propagates the corresponding decoder half's fine time and *hit bit* information together with an artificially generated MSB to the pre-pipeline register for storage. The complete schema of the TDC is depicted in fig. 3.

The pre-pipeline register is the interface to the following pipeline memory. In addition to the fine time, it also stores some status informations. It is further needed to feed the subsequent stages with programmable test data and also provides the test patterns for the self-test of the pipeline memory.

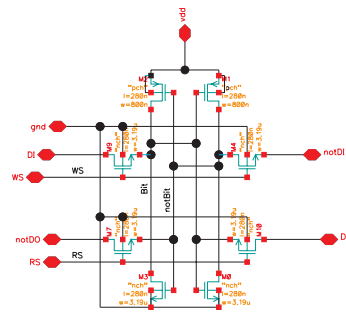


Figure 4: Schematic of an SRAM memory cell used in the OTIS' pipeline memory and derandomiser buffer.

B. Pipeline memory and derandomiser buffer

The pipeline memory is a 164×240 bit dual ported SRAM used as a ring buffer. Synchronous to the bunch crossing clock the data of the pre-pipeline register is written to the memory. A trigger initiates the clock synchronous transfer of 1, 2 or 3 words to the derandomiser buffer, selecting data that has been written to the memory up to 160 clock cycles (i.e. $4 \mu\text{s}$) ago. The derandomiser compensates trigger rate fluctuations and uses the same SRAM architecture as the pipeline memory. The size of it is 48×240 bit. Thus it is large enough to hold the data of 16 triggers ($\hat{=} 3$ words), which is an LHCb requirement. A cell of the SRAM memory is shown in fig. 4.

C. The control algorithm

The control algorithm performs the memory access required for trigger handling and data retrieval for readout. In addition it provides the 50 ns and 75 ns measurement ranges by combining data from up to 3 consecutive bunch crossings. Furthermore it implements the two different formats of the readout data stream:

- **Encoded Hitmask:** This data format is shown in tab. 1. The 4 byte header information (containing e.g. BX counter and status information) is followed 32 bytes representing the drift times of the 32 channels according to table 2. While the lower 6 bits are the measured fine time within the clock cycle, the first two indicate the bunch crossing of the hit, starting with 00 for the first one and leaving 11 to indicate the absence of a hit signal. Obviously only the first hit per trigger and channel is read out, allowing for a 100% channel occupancy. The fixed 900 ns readout time required by LHCb is intrinsic to this mode.
- **Plain Hitmask:** In this readout mode the 4 header bytes are followed by 1, 2 or 3 32 bit hit

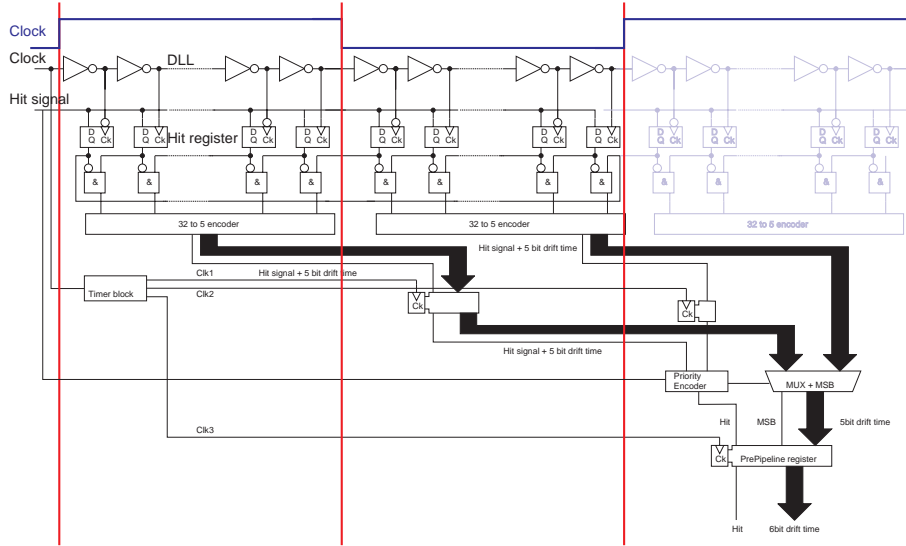


Figure 3: Schematic of the TDC core. The clock waveform on top together with the order of the different components is intended to visualize the timings of the different parts.

Table 2: 8 bit drift time encoding of the OTIS chip in *Encoded Hitmask mode*.

First Hit Position	Data
1 st BX	00xxxxxxxx
2 nd BX	01xxxxxxxx
3 rd BX	10xxxxxxxx
No Hit	11xxxxxxxx

masks and a number of 6 bit drift times according to the total number of "1"s in the hit masks. In this case the data frame has to be cut after 900ns or filled with "0"s to meet the LHCb specifications. Depending on the number of hit masks, only a limited occupancy per trigger and bunch crossing can be transmitted using the selectable truncation: 1 BX = 100%, 2 BX = 50%, 3 BX = 26%. The structure of the data frames is shown in tab. 3.

The transmission of a data frame on the OTIS' 8 bit parallel output port is indicated by a *Data Valid* signal. Further parts of the OTIS chip include a standard I²C interface used for setup, monitoring and slow control purposes. It is e.g. used to mask input channels, adjust the trigger latency or write playback data to the chip and select the playback mode. Furthermore it can be used for slow event readout and to set the threshold levels of the ASD chips via on-chip 8 bit DACs.

III. THE OTIS 1.0 CHIP

OTIS 1.0 is the first full scale prototype chip. On a die size of $5.4 \times 6.0\text{mm}^2$ it implemented all key features, but

- no Plain Hitmask readout mode
- no Data Valid Signal
- no event readout via I²C bus
- unbuffered DAC outputs
- LVDS (instead of differential CMOS) data outputs.

Measurements performed with the OTIS 1.0 chip during the last 14 month lead to a thorough understanding of the chip's features: The control algorithm performed as expected from simulations, i.e. the readout of a data frame takes exactly 900 ns, and while in playback mode, the read data is exactly as programmed. Also the trigger handling shows the predicted behavior, e.g. a *FiFo full* signal after 16 triggers in 3-BX mode. Furthermore a random trigger test performed at 40 MHz clock speed with some 10^7 triggers did not reveal any problems. However, depending on temperature and clock speed the chip's memory self test function failed after a certain time. Operation in playback mode, which is identical to the memory self test regarding pre-pipeline register and memory, did not yield any data corruption. Thus this failure was attributed to a timing problem in the error checker circuit, which is part of the control algorithm.

Tests of the TDC exhibited missing codes in the 2nd half of a clock cycle, including also losses of the hit bit. These effects are strongly channel-dependent as fig. 5 shows. The strong channel dependency, together with the vanishing of the effect in case a double hit (i.e. a hit signals with same relative timing in two consecutive clock cycles) was applied gave a strong hint

Table 1: Data format of the OTIS chip in *Encoded Hitmask* mode.

Bit	0...31	32...39	...	280...287
Data	Header	Drift time (CH0)	...	Drift time (CH31)

Table 3: Data format of the OTIS chip in *Plain Hitmask* mode for 1, 2 and 3 BX (top to bottom) readout.

Bit	0...31	32...63	64...69	...	$58 + (6n) \dots 63 + (6n)$
Data	Header	Hitmask (1 BX)	Drift time [1]	...	Drift Time [n]
Bit	0...31	32...95	96...101	...	$90 + (6n) \dots 95 + (6n)$
Data	Header	Hitmasks (2 BX)	Drift time [1]	...	Drift Time [n]
Bit	0...31	32...127	128...133	...	$122 + (6n) \dots 127 + (6n)$
Data	Header	Hitmasks (3 BX)	Drift time [1]	...	Drift Time [n]

on a timing problem with either *Clk2* or *Clk3* in fig. 3. At this point it should be denoted, that a parasitic simulation of the complete TDC circuit was not possible: A Simulation on the extracted netlist, which has a flat topology, failed due to insufficient computer resources⁴. A Simulation with backannotated capacitances is also impossible due to multiple instantiations of the same cell, which prevents the backannotation of the individual capacitances of each instantiation. An FIB⁵ patch on one chip, providing an external clock input to the timer block in fig. 3 proved ineffective. In turn a second patch, establishing an external *Clk3* inputs on channels 28, 29 and 30 was applied. Delaying this *Clk3* input by about 4 ns resulted in the nicely linear delay scan shown in fig. 6, which proves that the OTIS' TDC concept is working. Further measurements on this chip resulted in a differential nonlinearity of 0.54 ns (or 1.4 LSB), when no correction for the DLL's intrinsic asymmetry and the mismatch of the first and last time bin is (which is due to different routing and parasitics) is applied. Correcting for these systematic effects, the DNL is reduced to 0.25 ns (or 0.64 LSB), which is comparable to the results from the first DLL prototype (DNL = 0.51 LSB), which did not have this features.

IV. THE OTIS 1.1 CHIP

The crucial point causing the timing problems of the OTIS 1.0 TDC is the use of two clock domains within this circuit (c.f. fig 3): The clock signals delayed by the timer block made of unregulated inverter chains is used to latch signals locked to the well regulated timing of the DLL. Thus it was decided to eliminate the second clock domain inside the TDC by simply deriving all clock signals from the DLL. This is shown in fig. 7. Provided a good estimation of parasitics and a sufficient safety margin for process parameter variations,

⁴on a SUN Fire280r w. 8GByte RAM and 36GByte swap

⁵Focused Ion Beam

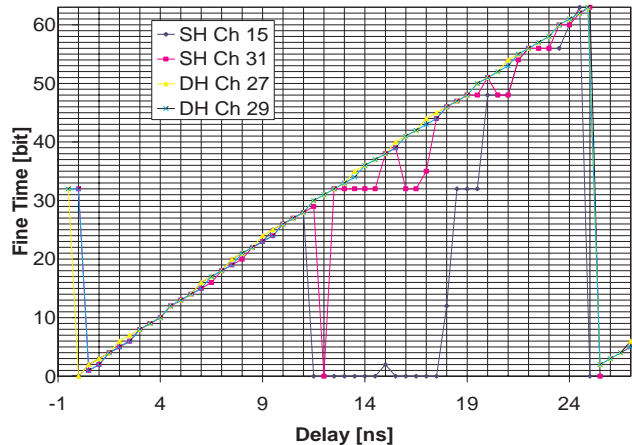


Figure 5: Delay scan of the OTIS 1.0 TDC. The figure shows channel-dependent missing codes in the 2nd half of a clock cycle, which disappear if signals with identical relative timing are applied in two consecutive clock cycles (DH = double hit).

this approach is immune against timing problems. Also the linearity of the DLL is improved by a better matching of the first and last delay elements to the center part of the DLL. Finally OTIS 1.1 will implement all missing features of OTIS 1.0, e.g:

- Plain Hitmask readout mode
- Data Valid signal for the subsequent GOL chip
- DAC outputs suitable to provide threshold levels to ASDblr or ASDq discriminator chips
- Differential CMOS outputs
- 5 V compatible I²C pads
- Event readout via the I²C bus
- Revised reset schema
- other minor changes

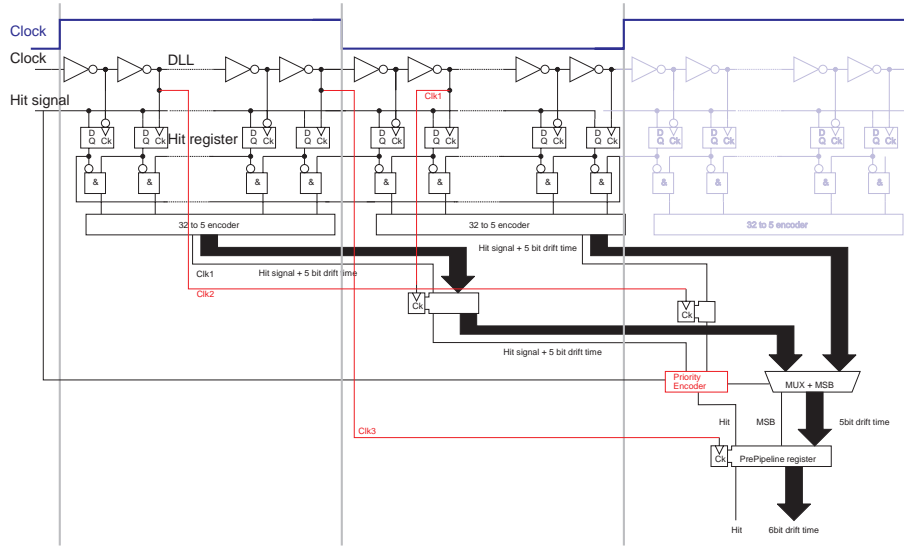


Figure 7: Schematic of the OTIS 1.1 TDC core. The clock waveform on top together with the ordering of the different components is intended to visualize the timings of the different parts. All clocks are now tapped from the DLL.

V. CONCLUSIONS

The first full scale prototype chip OTIS 1.0 fulfills all LHCb key requirements regarding timing and control signals, but needs some external components like level converters to fit into the LHCb outer tracker readout chain. Its TDC showed missing codes in the 2nd half of a bunch crossing and had to be patched to become fully functional. This patch led to a thorough understanding of the TDC and proved that the OTIS' TDC concept is working. The OTIS 1.1 will be submitted for production by the end of October 2003. It incorporates improved TDC and DLL components. Furthermore it features all planned readout modes and modifications to seamlessly fit into the LHCb outer tracker readout chain. In turn it is intended for production to equip this detector.

Status reports and further test results will be available at [3].

VI. REFERENCES

- [1] ATLAS use of ASDbl: http://www.quark.lu.se/atlas/electronics/trt/chip_asdbl.html
Measurements for LHCb: <http://www.nikhef.nl/user/toms/lhcb/otfe/afe/deadtime/index.html>
- [2] A 1.25 Gbit/s Serializer for LHC Data and Trigger Optical Links, Paola Moreira et al., Proceedings of the 5th workshop on electronics for LHC experiments, September 20-24, 2000, CERN-LHC-2000/041
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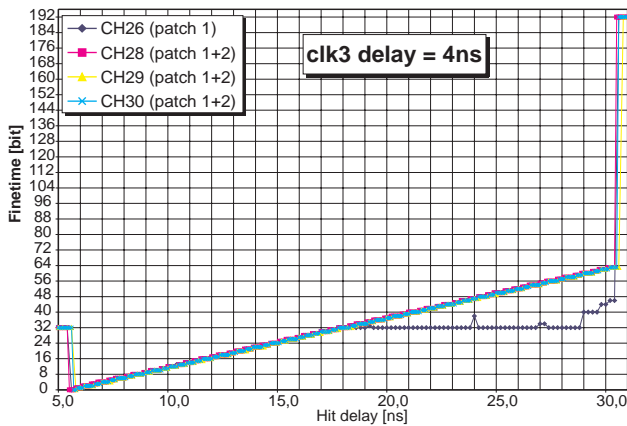


Figure 6: Delay scan of the patched OTIS 1.0 TDC. The missing codes on channels 28, 29 and 30 (ext. *Clk3* input) have disappeared, while channel 26, which is missing the 2nd patch still shows this problem. The drift time of 32 on the left margin is caused by the hit signal of the previous bunch crossing while the 192 at the right margin are the correct encoding of an empty event (c.f. tabs. 1 and 2).