Performance of the ALICE TPC Front End Card

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Abstract

This paper addresses the performance of the Front End Card (FEC) for the ALICE Time Projection Chamber (TPC) on measured data. The ALICE TPC Front End Electronics consists of 557568 channels. A single readout channel is made of two basic units: (a) an analogue ASIC (PASA) that incorporates the shaping/amplifier circuits for 16 channels; (b) a mixed-signal ASIC (ALTRO) that integrates 16 channels, each consisting of a 10-bit 25-MSPS ADC, the baseline subtraction, tail cancellation filter, zero suppression and multi-event buffer. The complete readout chain is contained in FECs, with 128 channels each, connected to the detector by means of kapton cables. A fraction of the final electronics (1024 channels) has been characterized in a test that incorporates a prototype of the ALICE TPC as well as many other components of the final set-up. The tests show that the system meets all design requirements.

I. Introduction

The ALICE Time Projection Chamber [1] (TPC) is a large gas cylinder (about 88 m^3) divided in two drift regions by an electrode located at its axial centre. A field cage creates a uniform electric field along each half of the chamber. Charged particles traversing the TPC volume ionise the gas along their path, liberating electrons that drift towards the detector end plates where multi-wire proportional chambers, with cathode pad readout, provide the necessary signal amplification. Each of the two readout planes is azimuthally segmented in 18 trapezoidal sectors.

As detailed in [1], the front-end electronics has to read out the charge detected by 557568 pads located on the readout chambers at the TPC end-caps. These chambers deliver on their pads a current signal with a fast rise time (less than 1ns), and a long tail due to the motion of the positive ions. The amplitude has a typical value of 7μA. The signal is delivered on the detector impedance that, to a very good approximation, is a pure capacitance of the order of few pF.

II. General Requirements

The main requirements for the readout electronics are listed in Table 1.

Table 1: Front-end electronics requirements

PARAMETER	VALUE
Nr. of channels	557 568
Signal-to-noise ratio (MIP)	30:1
Dynamic range	900:1
Noise (ENC)	< 1000 e^-
Conversion gain	6 ADC counts / fC
Cross-talk	< 0.3 %
Shaping time (FWHM)	190 ns
Sampling rate	5 – 12 MHz
Tail suppression after 1μs	1‰
Power consumption	< 100 mW / channel

One of the tightest requirements is defined by the extremely high pulse rate with which the ALICE TPC FEE has to cope. Indeed, the detector innermost chamber will be exposed to signal occupancy up to 50%. On the other hand, the extremely

large data volume (~ 700MByte / event) requires performing the zero suppression in the FEE. Therefore, in order to preserve the full resolution on the signal features (amplitude and time), a very accurate cancellation of the signal tail and correction of the baseline have to be performed before the zero suppression.

The radiation load on the TPC is low (1krad ⊕ 10^{11}neutrons/cm^2 over 10 years). Thus standard radiation-soft technologies are suitable for the implementation of this electronics. However, some special care should be taken to protect the system against potential damages caused by Single Event Effects.

The front-end electronics system has to satisfy many other constraints while meeting the required performance specifications. Mainly, the read-out electronics needs to fit into the overall detector structure; in particular into the available space, which has important consequences for the requirements on reliability, power, and cooling.

III. SYSTEM OVERVIEW

A single readout channel is comprised of three basic functional units (fig. 1): a charge sensitive amplifier/shaper (PASA); a 10-bit 25-MSPS low power ADC; a digital circuit that contains a shortening filter for the tail cancellation, the baseline subtraction and zero suppression circuits, and a multiple-event buffer.

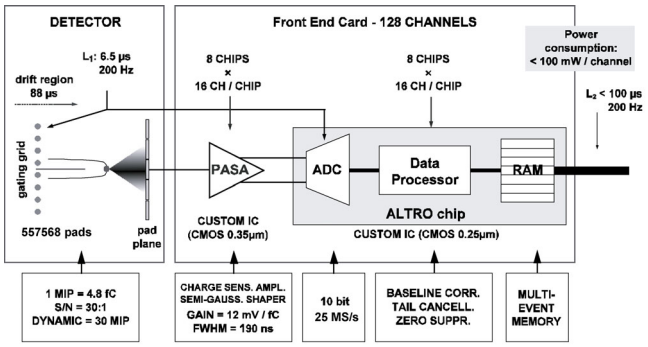

Figure 1: Front-end electronics basic components

The charge collected on the TPC pads is amplified and integrated by a low input impedance amplifier. It is based on a charge sensitive amplifier (CSA) followed by a semi-Gaussian pulse shaper of the 4th order. These analogue functions are realised by a custom integrated circuit, implemented in a CMOS technology 0.35µm, which contains 16 channels with a power consumption of 11mW/channel. The circuit has a conversion gain of 12mV/fC and an output dynamic range of 2V with a differential non-linearity of 0.2%. It produces a pulse (fig.2) with a rise time of 120ns with a shaping time (FWHM) of 190ns. The single channel has a noise value below 570e$^-$ (r.m.s.) and a channel-to-channel cross–talk below -60dB.

Immediately after the PASA, a 10-bit pipelined ADC (one per channel) samples the signal at a rate of 5-12 MHz. The digitised signal is then processed by a set of circuits that perform the baseline subtraction, tail cancellation, zero-suppression, formatting and buffering. The ADC and the digital circuits are contained in a single chip named ALTRO [2,3]. ALTRO (see figure 3) integrates 16 channels, each of them consisting of a 10-bit, 25-MSPS ADC, a pipelined Digital Processor and a multi-acquisition Data Memory.

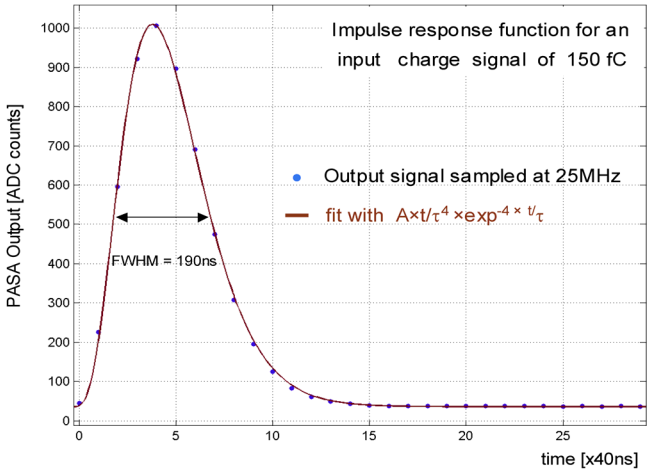

Figure 2: PASA response function

When a Level-1 trigger is received a predefined number of samples (acquisition) is temporarily stored in a data memory. Upon Level-2 trigger arrival the latest acquisition is frozen, otherwise it will be overwritten by the next acquisition. The Digital Processor, running at the sampling frequency, implements several algorithms that are used to condition and shape the signal. After digitisation, the Baseline Correction Unit I is able to perform channel-to-channel gain equalisation and to correct for possible non-linearity and baseline drift of the input signal. It is also able to adjust DC levels and to remove systematic spurious signals by subtracting a pattern stored in a dedicated memory. The next processing block is an 18-bit, fixed-point arithmetic, 3rd order Tail Cancellation Filter. The latter is able to suppress the signal tail, within 1µs after the pulse peak, with the accuracy of 1LSB. Since the coefficients of this filter are fully programmable, the circuit is able to cancel a wide range of signal tail shapes. Moreover, these coefficients can be set independently for each channel and are re-configurable. This feature allows a constant quality of the output signal regardless of ageing effects on the detector and/or channel-to-channel fluctuations. The subsequent processing block, Baseline Correction Unit II, applies a baseline correction scheme based on a moving average filter. This scheme removes non-systematic perturbations of the baseline that are superimposed to the signal. At the output of this block, the signal baseline is constant with an accuracy of 1LSB. Such accuracy allows an efficient Zero-Suppression procedure, which discards all data below a programmable threshold, except for a specified number of pre- and post- samples around each pulse. This produces a certain number of non-zero data packets, thus reducing the overall data volume. Each data packet is formatted with its time stamp and size information in a way

that reconstruction is possible afterwards. The output of the Data Processor is sent to a Data Memory of 5-Kbyte, able to store up to 8 full acquisitions. The data can be read out from the chip at a maximum speed of 60MHz through a 40-bit wide bus, yielding a total bandwidth of 300-Mbyte/s. Moreover, the readout speed and the ADC sampling frequency are independent. Therefore, the readout frequency does not depend on the bandwidth of the input signal being acquired. The ALTRO chip is implemented in the ST 0.25µm HCMOS-7 process.

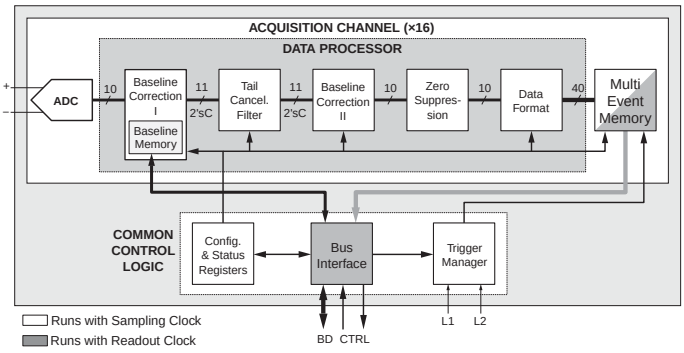

Figure3: The ALTRO chip block diagram.

The complete readout chain is contained in the Front End Cards (FEC) [4], which are plugged in crates attached to the detector mechanical structure. Each FEC, better described in the next section, contains 128 channels and is connected to the cathode plane by means of 6 flexible cables. A number of FECs (up to 25) are controlled by a Readout Control Unit (RCU)[5]. As sketched in figure 4, the RCU interfaces the FECs to the DAQ, the Trigger, and the Detector Control System. The RCU broadcasts the trigger information to the individual FEC modules and controls the readout procedure. Both functions are implemented via a custom bus, based on low-voltage signalling technology (GTL), the ALTRO bus. The interfacing of the RCU modules to the Trigger and to the DAQ follows the standard data acquisition architecture of the experiment.

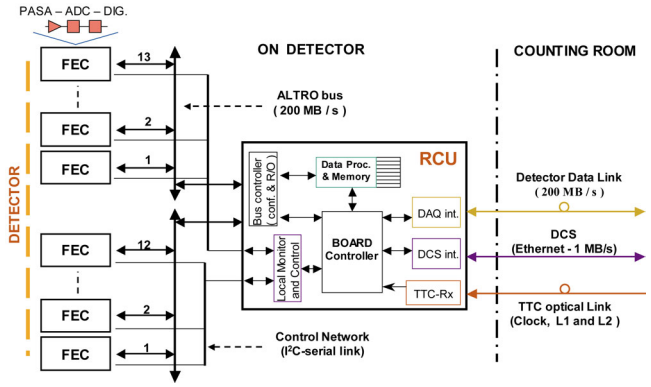

Figure 4: Block diagram of the TPC readout partition. The overall TPC readout consists of 216 readout partitions.

In summary, for each of the 36 TPC sectors, the front-end electronics consists of 121 FECs, 6RCUs, and 6 detector data links.

IV. THE FRONT END CARD

The Front-End Card contains the complete read-out chain for amplifying, shaping, digitising, processing and buffering the TPC signals; it must handle the signal dynamic range of about 10 bits with minimal degradation of precision and store the signals during the Level-2 trigger latency.

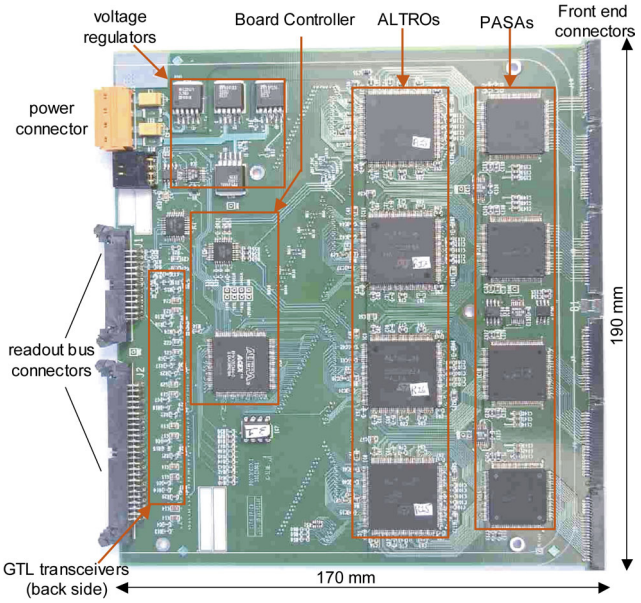

Figure 5: FEC layout. The components are mounted on both sides of the board. The figure shows the board topside with 4PASAs, 4 ALTROs, 1 FPGA, the voltage regulators and other auxiliary components. On the board bottom side are symmetrically mounted other 4 PASAs and 4 ALTROs and, close to the readout bus connectors, the GTL transceivers.

With reference to figure 5, we describe hereafter the FEC layout following the signals flow. The FEC receives 128 analogue signals through 6 flexible kapton cables and the corresponding connectors. The input signals are very fast, with a rise time of less than 1ns. Therefore, to minimise the channel-to-channel crosstalk, the 8 PASA circuits have to be very close to the input connectors. The analogue to digital conversion and the digital processing are done by the ALTROs, which are connected to the corresponding PASAs with differential signals. It should be noticed that the PASA and ALTRO can also be interconnected in a single-ended mode. However the noise increases by a factor two with respect to the differential-mode interconnection adopted in the FEC.

The FEC channels are multiplexed, at the board level, via a LVCMOS bus. It features an asynchronous VME-like protocol, which is enhanced by a clocked block-transfer that provides a bandwidth of up to 300Mbytes/s. The FEC is interfaced to the RCU through a bus based on the GTL technology, named ALTRO bus [6]. At the board output the bus signals are translated from LVCMOS level to GTL level by bi-directional transceivers. The configuration, readout and test of the board are done via the GTL bus. Moreover, the FEC contains a circuit implemented in a FPGA, named Board

Controller (BC), which provides the RCU with an independent access to the FEC via an I^2C link. This secondary access is normally used to control the state of the voltage regulators and monitor the board activity, power supplies and temperature.

The board offers a number of test facilities. As an example a data pattern can be written in the ALTRO chip and readout back exercising the complete readout chain. The Board Controller allows verifying the bus activities, the presence of the clock and the number of triggers received.

The ALTRO chips and the BC work synchronously under the master clock with a frequency up to 60 MHz. The ALTRO circuits usually perform the same operations concurrently, under the control of the RCU. However, the latter can also control a single channel at a time. This is performed in the configuration phase and for test purposes. The RCU broadcasts the trigger information to the individual FEC modules and controls the readout procedure. Both functions are implemented via the GTL bus.

In order to match the position of the connectors on the back of the chamber pad plane, the FEC has to have a width of 190mm. Moreover, in order to fit into the available space its height and thickness are of 170mm and 14mm respectively.

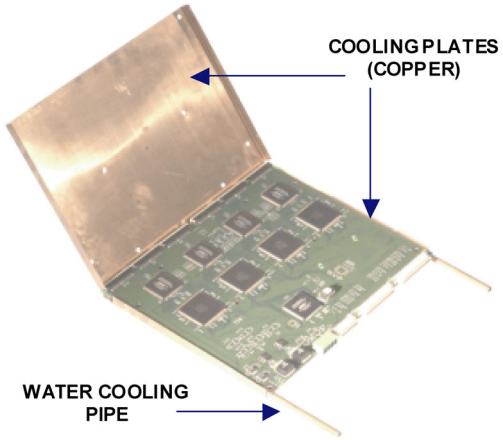

Figure 6: Cooper cooling plates and FEC assembly.

The FEC printed circuit board (PCB) contains 4 signal layers and 4 power layers (2 supply layers with the corresponding ground layers). The power layers have essentially the same geometry. The duplication of the power and ground layers, provides the following advantages: 1) it eases the implementation of the controlled-impedance lines; 2) it reduces the voltage drop over the power layers; 3) it reduces the noise produced by the ground bouncing. From the power supply point of view the board is divided in three main sections: the PASA section, the ALTRO/ADC section and the digital section. Therefore each power layer consists of three different power planes. The ALTRO/ADC and the digital planes are supplied with the same input voltage (+2.5V), and are closed together at the input of the voltage regulators. The PASA plane is supplied at +3.3V. The three ground planes (PASA ground, ALTRO/ADC ground and digital ground) are closed together with a pad, which is located upstream the voltage regulators.

The FEC has a maximum power consumption of about 6W. In order to minimize the heat transfer to the detector sensitive volume, the FECs are embedded in two copper plates cooled by water (see figure 6).

V. INTEGRATION WITH THE DETECTOR

A fraction of the final electronics (1024 channels) has been characterized in a test that incorporates a prototype of the ALICE TPC as well as many other components of the final set-up (e.g. detector data link, cooling system and low-voltage power supply).

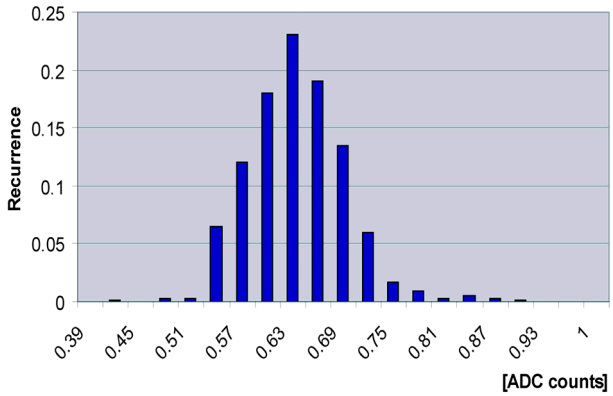

Figure 7: Histogram of the r.m.s. noise for 1024 FEC channels connected to the detector.

As ionization sources the ^{83}Kr decay and Cosmic rays have been considered. The tests show that the system meets all design requirements. It exhibits a noise (r.m.s.) of 0.65 ADC counts (fig. 7), which corresponds to an equivalent noise charge of 730 e^-, and a spread in the output DC level of 3% of the dynamic range.

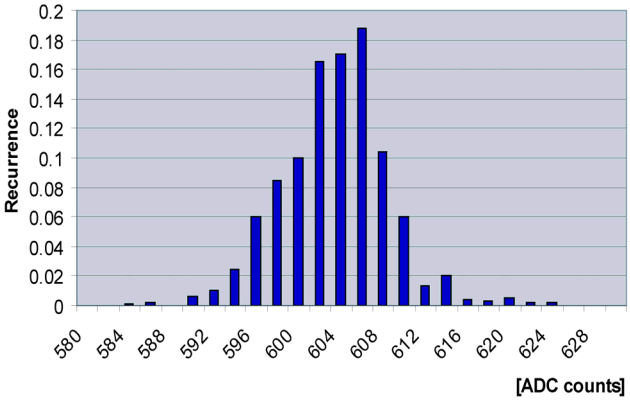

Figure 8: FEE Conversion Gain dispersion measured pulsing the detector cathode wires.

The dispersion of the conversion gain has been measured pulsing the detector chamber cathode wires. The resulting pulse height distribution shows a dispersion in the overall signal conversion gain in the order of 8 ADC counts (r.m.s.) (fig. 8).

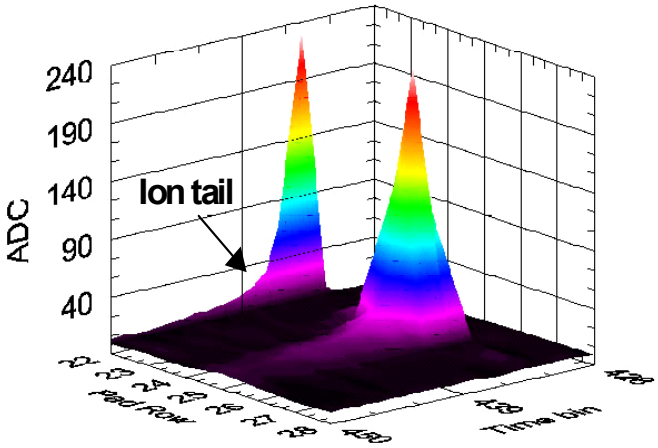

Figure 9: Single ionization cluster produced by the decay of ^{83}Kr.

Particular emphasis was given to the detailed characterization of the detector signal and the study of the performance of the digital processing algorithms. The study of single ionization clusters (figure 9), produced by the decay of the ^{83}Kr, allowed a full characterization of the signal ion tail and the calculation of the coefficients of the tail cancellation filter.

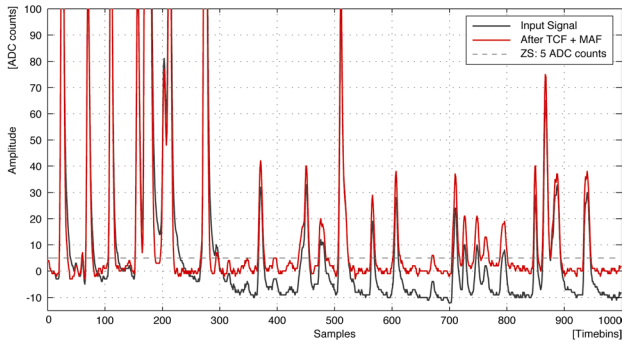

Figure 10: Processing of a high occupancy cosmic ray event. In black the signal at the input of the ALTRO chip processing chain. In red the combined effects of the ALTRO's Tail Cancellation filter. (TCF) and Moving Average filter (MAF). The dotted line represents the zero suppression threshold. The application of the TCF and MAF allows retrieving signals that otherwise would be discarded by the zero suppression algorithm.

The detection of events produced by large showers of cosmic rays allowed testing the performance of the tail cancellation and baseline correction circuits. Indeed, a few events were characterized by the same signal occupancy (about 50%) predicted for the relativistic collisions of heavy ions in ALICE (figure 10).

These measurements show that the ALTRO chip performs a good cancellation of the signal tail (0.1% of the signal amplitude within 1μs) and the restoration of the baseline (within 1 ADC count), even for very high signal occupancy.

VI. Conclusions

An innovative electronic system with on-detector signal processing has been developed for the ALICE TPC FEE. A fraction of the final electronics has been benchmarked by realistic measurements with a prototype of the ALICE TPC.

Test show that the system fulfils all design requirements. In particular, despite of the high level of integration of digital circuits close to the analogue front-end, the system shows a noise figure of 730e$^-$ (r.m.s.). Moreover, the tests have shown that the system is able to process high multiplicity events with a baseline restoration at 1 ‰ of the dynamic range within 1μs. The average power consumption of the final system is about 40mW/channel.

VII. References

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