

The ALICE Pixel Detector Readout Chip Test System.

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Abstract

The ALICE experiment will require some 1200 Readout Chips for the construction of the Silicon Pixel Detector [1] and it has been estimated that approximately 3000 units will require testing.

This paper describes the system that was developed for this task.

I. INTRODUCTION

The Pixel Readout chip [2] is a mixed signal device containing both analogue and digital circuits. It is made up as a matrix of 32 columns by 256 rows of Pixel cells. Each cell comprises of a pre-amplifier, pulse shaper, discriminator, two digital delay units and a 4 event de-randomising buffer. These cells are connected as 32 parallel shift registers each of 256 bits read out sequentially at 10MHz. Each cell contains five configuration bits, three for the threshold fine control and two to enable testing and masking of the cell.

The test system used for testing the prototype version of the readout chip was made up of several modules each performing a specific function, but were invariably of different formats and often requiring adaptation between them. The computer used to control the system was not flexible enough to be able to be programmed to give a rapid online indication of the quality of the device under test or to present the results of the completed measurement in a graphic manner. With so many devices to be characterised and tested the opportunity was taken to develop a simple yet flexible test system incorporating the required functionality which could be used at all stages of the testing and qualifying of the Readout chips and sub assemblies.

The test system should be capable of supplying the necessary signals to ensure the correct functionality of the

internal circuitry of the device as well as finding use in other areas of the qualification process.

II. THE TEST PROCEDURE

Initially, several devices were tested on an Integrated Circuit (IC) tester capable of performing simple low level tests. These tests ensured that the various sections within the devices functioned correctly and could be accessed for more complete tests¹. Once the design had been proved to function correctly on the IC tester they were transferred to the Test System for higher level tests.

Using the test system each device was fully characterised for its dc operating conditions, power consumption and the functioning of the various internal sections, including dynamic testing of the sensitivity and spread of thresholds, noise, calibration of the internal configuration digital to analogue converters.

At each step the system is capable of displaying the progress of the measurement and once finished the results are displayed in a graphical form. Data is stored into a database for reference at a future date.

The same hardware was used for beam tests and tests of radiation tolerance.

III. THE SYSTEM DESIGN

The test system was designed taking the following requirements into account:

- *Hardware Requirements*
 - To supply the necessary supply voltage and biases as required by the device,

¹ We shall not discuss these tests in detail as they are beyond the scope of this paper.

- provide an interface between the DAQ environment and the Pixel Chip environment,
- be flexible enough to perform a variety of DAQ functions such as Wafer Probe testing, testing subassemblies of the Pixel Detector, radiation and beam tests,
- be simple, compact and easy to reproduce,
- use off-the-shelf and industry-standard components whenever possible,

- *Software Requirements*

- Have powerful graphic capabilities,
- be flexible and adaptable when choosing hardware,
- a comprehensive Graphical User Interface (GUI) should be developed,
- full monitoring facilities should be available,
- generation and maintenance of a database,
- be adaptable to different test scenarios.

The test system has been designed around a PC connected to a VME crate, as shown in Figure 1. The connection is made by a National Instruments MXI connection.

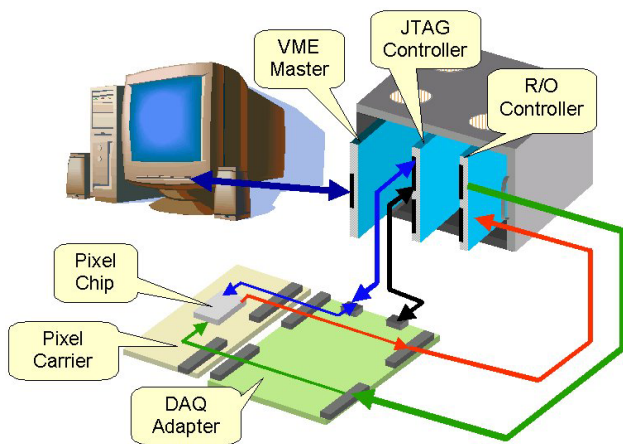


Figure 1: The layout of the basic test system

A Readout Controller (PILOT Module) [3] has been developed in the VME standard to control the readout of the Pixel Readout Chip. As the Pixel Readout Chip is configured and controlled by JTAG [4] so JTAG is also used control a DAQ Adapter board that is situated close to the Pixel readout chip under test. There are various choices of JTAG controller: models which use a PC parallel port, models which may be installed in the PC, or as in our case a module installed in the VME crate. Differential connections between the modules installed in the VME crate and the DAQ Adapter board allow the use of long interconnecting cables making the system suitable for use where the readout/test system must be sited away from the actual Pixel Readout chip.

- *The PC*

As the functioning of the system relies heavily on software and that large amounts of data need to be manipulated, a fast PC with a large amount of memory and storage is preferable.

- *MXI Controller*

The MXI Controller [5] provides the connection between the PCI bus of the PC and the DAQ VME crate.

- *Readout Controller*

The readout controller (Figure 2) is a VME module that, on receipt of commands from either the VME bus or an external source of trigger signals, generates all signals necessary for the readout of the Pixel Chip. Zero skipping and hit encoding are performed to reduce the amount of data to be stored. A test path has been included to allow testing the system with known data.

- *JTAG Controller*

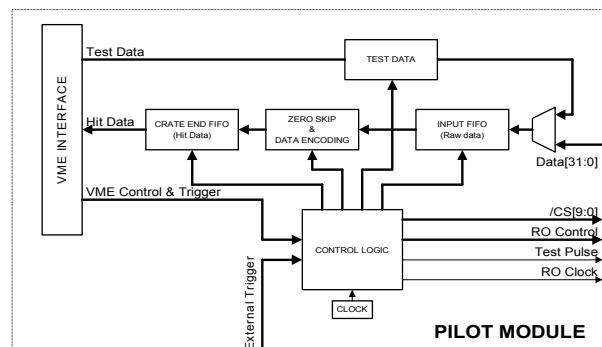


Figure 2: The block diagram of the Readout Controller.

The JTAG controller requires two channels, one for controlling and configuring the Pixel Readout Chip, the other to control the DAQ Adapter Board. Using two channels reduces the risk of a faulty Pixel Readout Chip impeding the correct functioning of the DAQ Adapter Board.

- *DAQ Adapter Board*

The DAQ Adapter Board is situated between the Pilot Module and Pixel Chip under test and serves as an interface between the two environments. It houses the line drivers and receivers necessary for the DAQ connection and Gunning transceiver Logic (GTL) drivers necessary for the Pixel Chip bus connection.

It also houses the circuitry to derive the necessary power and bias supplies. Monitoring of both applied voltage and consumed current are possible.

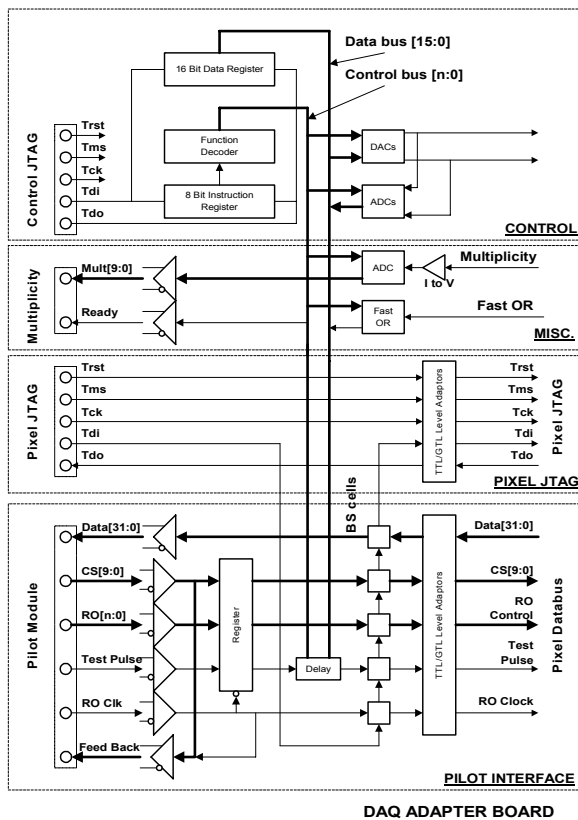


Figure 3: The block diagram of the DAQ Adapter Board.

Additional circuitry has been included to allow a multiplicity measurement to make a rapid evaluation of the total number of hit Pixels within the chip.

The control of the Adapter Board is by means of a simple JTAG protocol consisting of an 8 bit IR Scan to address a device and a 16 bit DR Scan to write or read a data value.

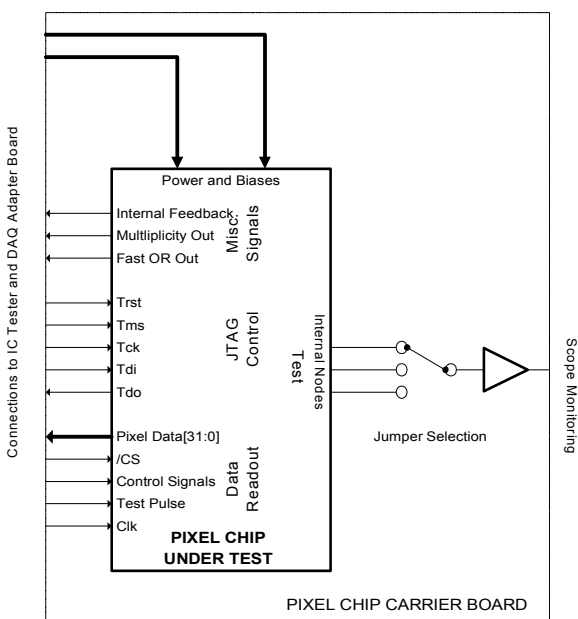


Figure 4: The block diagram of the Pixel Carrier Board.

- Pixel Readout Chip Carrier Board

The individual Pixel Readout chips are wire bonded to the carrier board (Figure 4), which may be connected to either the IC tester, or the DAQ Adapter board. Test points have been included on all bus signals. Facilities have been provided to allow observation of various internal nodes of the device.

Variations of the carrier board have lent themselves for both wafer probing tests and evaluation of the prototype bus structure currently under design for use in the Pixel Detector.

IV. TEST SYSTEM SOFTWARE

The final testing and production of the Alice Pixel detector will take place in several laboratories. For practical reasons the number of operating systems and software environments must be kept to a minimum.

The test software architecture reflects the flexibility of the hardware. Its modularity guaranties that the system can be used with different hardware

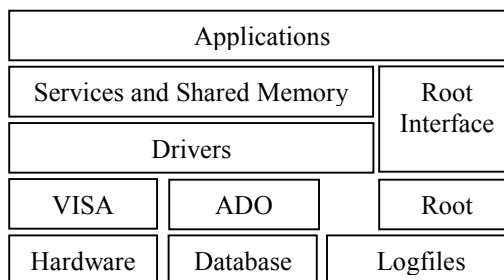


Figure 5: The PTS software architecture

configurations without the need of rewriting the software core.

Windows 9x/NT/2K and National Instrument's LabView were chosen as the main software environments. In addition, CERN's package ROOT [6] is used for offline analysis. The system has taken advantage of several industrial standards, such as VISA [7] or ADO [8] to simplify hardware and database access.

To enhance the flexibility, software modules are logically grouped into three basic layers: the drivers, services and applications to form the full Pixel Test System (PTS). The relationship between architectural layers is shown in Figure 5.

The driver layer handles the communication between the software system and hardware components. Its main role is configuration of connected devices and basic I/O operations (e.g. JTAG data scan). Drivers communicate with the service layer by means of a fixed protocol, which simplifies system adaptation to hardware modifications. A hardware modification requires only a minimum set of software modules to be changed.

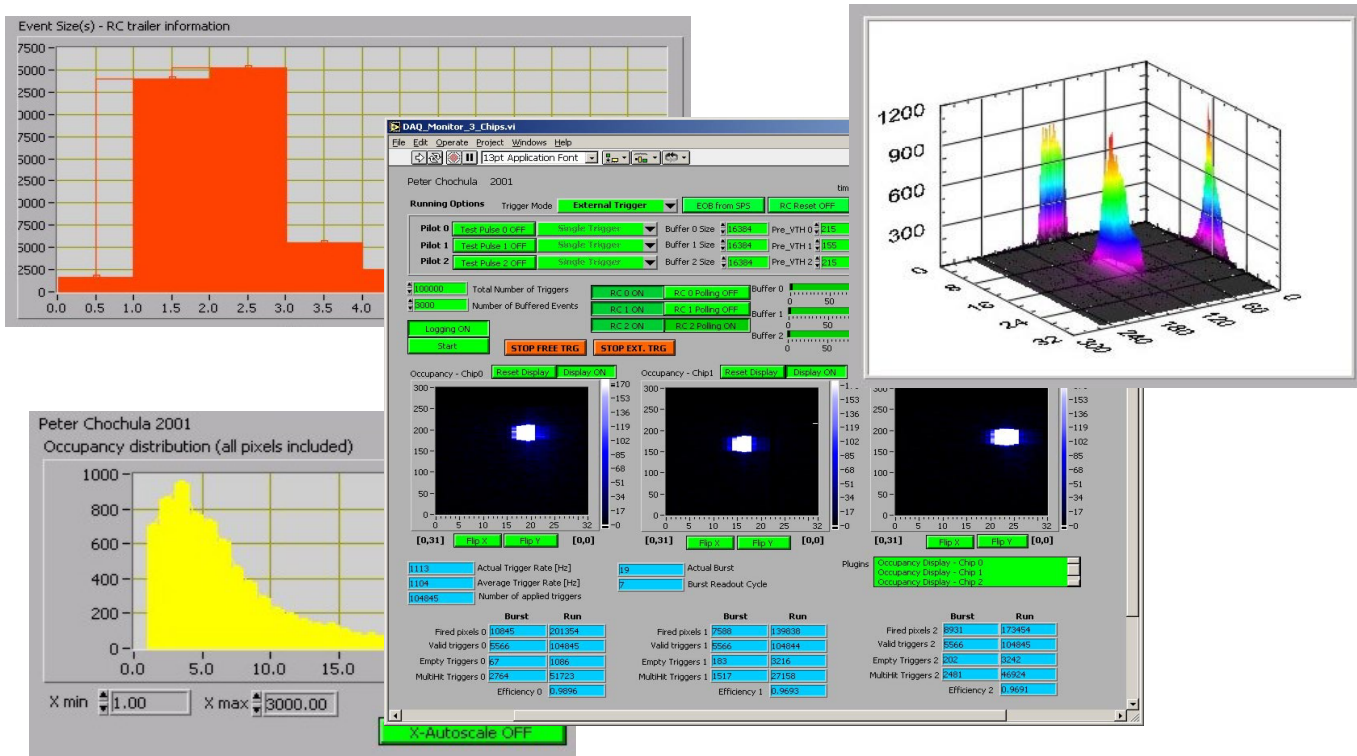


Figure 6: A snapshot of DAQ Monitor display with an example of plugins

On the lowest level, the drivers rely on Virtual Software Architecture (VISA). This industrial standard provides a unified interface to different busses (e.g. VME, VXI, GPIB, RS-232 or Ethernet). For non-VISA compliant devices Windows compatible DLL libraries are used.

The service layer acts mainly on the data level. Its role is data formatting and integrity checking. For example, pixel data are checked for consistency at this level. Corrupted frames, buffer overflows or missing triggers can be immediately signalled to the applications, which can then take the proper action. Another important role of the service layer is data flow control. For example, two applications are not allowed to access the same hardware at the same time. Device execution timeouts are also handled at this level so that an accidental hardware failure will not lock the software system. Inter-module communication is simplified by using shared memory also provided by this layer.

Programs belonging to the highest layer are divided into two basic categories: the Control Panels and the Applications. Each hardware component of the system has its own associated Control Panel, which enables low level register access, device reconfiguration and macro command execution. Programs belonging to this category are mainly used for debugging or low-level device commissioning. On the other hand, the Applications perform the most complicated tasks including JTAG integrity checks, DAC calibrations and threshold scans.

V. THE TESTBEAM SOFTWARE SYSTEMS

The Test beam DAQ and monitoring program is also a part of the highest PTS layer. It is the most powerful part of PTS so far. A single application (called DAQ Monitor) enables the acquisition of data in a variety of conditions ranging from free running modes with either software or external triggering up to the synchronous operation with an external triggering system. The DAQ Monitor can service a variable number of connected detectors.

In order to keep the testbeam control system at the level of a single application, a concept of plugins has been introduced. These plugins are software modules used to perform specialized tasks, such as checking of trigger efficiencies, monitoring of system performance and calculation of cluster size distributions. The online system loads the plugins on demand. For example they are completely omitted if the highest system speed is required. The offline analysis can re-use the same plugins for data reconstruction. An example of the DAQ displays is shown in Figure 6.

The DAQ software is capable of operating at a sustained trigger rate of 65 kHz, which is adequate for testbeam purposes requiring a trigger rate of ~10 kHz.

The detector control system monitors voltages and temperatures in the different parts of the system. A LabView controlled multiplexer connects input channels to an external GPIB based multimeter. The position of the

irradiated chips can be changed by using a remotely controlled x-y table.

VI. OFFLINE ANALYSIS AND DATABASE ACCESS

Despite its flexibility, the physics community does not commonly use LabView for data analysis. Instead, the Root system is usually employed to perform the offline processing. The PTS includes an interface that allows for this task. By using Root, the PTS can take advantage of the variety of its classes for efficient analysis. The choice of Root was motivated also by economical factors, since it is a free system and does not require the purchase of expensive compilers. A non-negligible fact is also the portability of code to different operating system platforms. However our mainstream system remains Windows.

To perform the characterization of the full production of about 3000 chips, several Terabytes of data must be processed. The production data and measured optimal settings for each chip must be preserved in an accessible way for the actual PTS as well as for future final DAQ and Control systems. Our choice has been the MySQL [9] database running under the Linux operating system. To interface the database to LabView we use Microsoft's Active Data Objects (ADO). This technology, based on ActiveX [10], provides a unique way of accessing different data sources either locally or over a network. One of the main advantages of ADO is that being an industrial-standard our system will be compatible with any common database which we might choose in the future. In a manner similar to the hardware drivers, it is only necessary to change a software driver (data provider) to make the PTS compatible with any other data sources.

VII. CONCLUSIONS

The test system described has proved to be flexible enough to satisfy all the requirements ranging from wafer probing, readout chip testing, radiation and beam testing.

The software has greatly reduced the time necessary to characterize the devices. The PTS has proved invaluable not only to rapidly assess the device under test is functioning but also to assist with the debugging of the overall system

VIII. REFERENCES

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