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The Front-End Electronics for LHCb calorimeters[1]

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1. ABSTRACT

The electronics for the electromagnetic and hadronic calorimeters of LHCb is under design. The 32 channel-9U front-end board offers the complete front-end and readout electronics for every channel including original shaping, 12bit-40MHz ADC, digital filtering and latency for level 0 and level 1 triggers. The clipped PM input signal is integrated during 25ns, but also delayed then subtracted to itself 25ns later which allows performant pile up independence. This board also includes the first processing levels of the L0 calorimeter trigger.

A 16 channel-6U prototype board has been designed and used at CERN in test beam in 1999.

2. INTRODUCTION

The electromagnetic and hadronic calorimeters currently designed for LHCb are lead-scintillator and iron scintillator sandwiches read by light shifting fibers. The output of the plastic fibers is equipped with phototubes. The readout system will have about 6000 channels for the Ecal and 1500 for the Hcal.

3. REQUIREMENTS

The main requirement for LHCb electronics is the pile-up rejection. Indeed, to ensure a satisfactory independance of successive sampling, the residue of a signal 25 nsec after the sampling time is required to be less than 1%. This implies to shape the PM signal. Shaped data has to be sampled at 40MHz on 12 bits then to undergo digital filtering for rejecting LF noise and to be transcoded within LUTs into energy over 8 bits for trigger data and 12 bits for readout data. The latter has to be buffered during the L0 latency, (4 μsec)[1] to be derandomized and then rebuffered for the level 1 latency. After the level 1 trigger, an extended zero suppression has to be performed before sending the formatted event to the DAQ.

There are also trigger elements sitting in the front-end crate. The first stages concern the search for local maxima inside groups of 512 channels, with a validation by the Preshower and Pad Chamber data.

4. FRONT-END OVERVIEW

Fig 1 describes the Front-End crate and its main interconnections. The PM signals are connected to the Front-End board through 10 meters of coaxial cables. There are 16 FEBs in the crate, each receiving 32 signals. The output of these boards are connected to the custom backplane, sending signals using LVDS levels to the Event Filter. This board is in charge of performing the advanced zero suppression and the event formatting after level 1. Data is then sent to the DAQ through optical links. The Crate Controller is in charge of driving the serial link which is used for loading the hardware and of distributing the TTC signals. These two boards may eventually become a single board.

From its 32 signals, and using also neighboring cells, each FEB computes, in pipeline mode, the maximum of the 32 sums over every 2x2 cell area. This maximum is sent to the Trigger Validation Board, which validates the candidate with the Preshower and the Pad Chamber (ECAL) or adds the ECAL information [3] (HCAL), and then sends the result to the final Selection Crate over long distance links, for the final Level 0 decision

[1] This is an update and supersedes the note 99-053. It includes more recent measurements and corrections and classifications of some results.

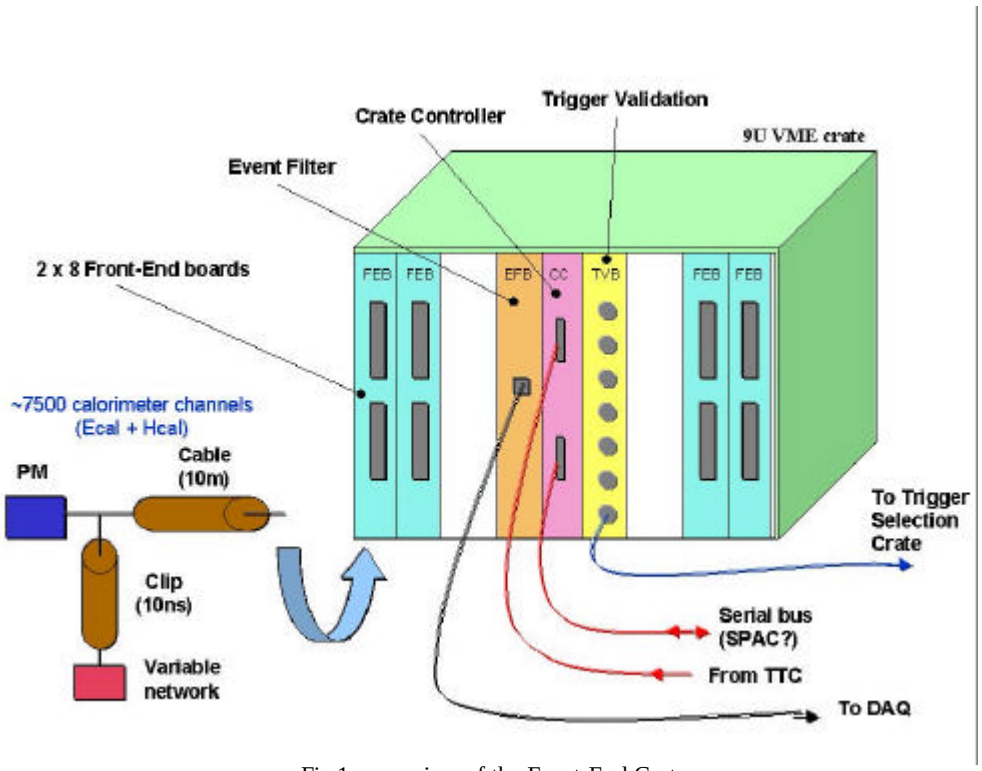

Fig 1 : overview of the Front-End Crate

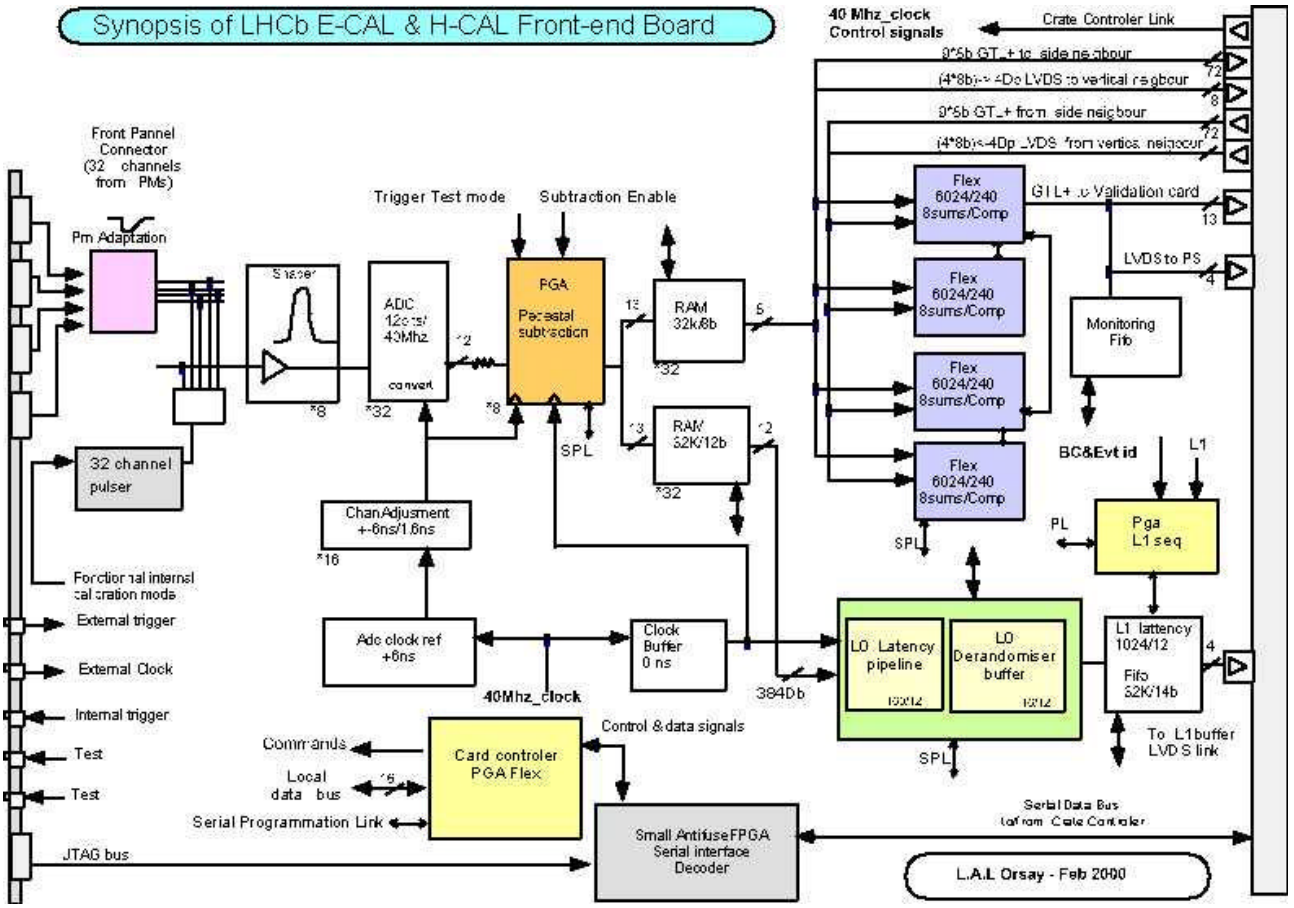

Fig 2 : block diagram of the Front-End board

5. THE FRONT-END BOARD

Fig 2 shows the block diagram of the 32 channel Front-End board. This is a 9U board using VME mechanics but without the VME bus. The access to the board ,for initialisation and monitoring ,will be only trough a serial bus which has still to be defined.

The main data path inside the board starts with the four 8-channel coaxial input connectors. The signals goes into the cable compensation, a pole zero network compensating for a 10%-20nsec signal tail, before entering the analog chip. After a 12bit ADC conversion, data undergoes a subtraction of the smallest of the two previous samples. This subtraction is intended to reduce the high bandwidth noise of the integrator, and the two samples are used to decrease the probability that a signal is present in the sample which is subtracted. Then data is converted into energy within two LUTs, one for the trigger which outputs 8 bit words, the other for the readout data which outputs 12 bit words in a pseudo floating format. The latter data is then sent to the L0 latency pipeline, L0 derandomizer and L1 latency buffer. After L1 trigger, it is sent across the backplane using LVDS levels towards the Event Formatter.

At the right top of the board, trigger data is first added in squares of 4 cells while preserving the original granularity, then compared looking for the local maximum on the board. The latter is sent with its address (total of 13 bits) using LVDS levels towards the Trigger Validation Board.[3]

Beside those data paths, some utility functions have been implemented. To correct for variable time delay in PM, one can adjust the sampling time of every ADC on the board thanks to programmable delay chips with a precision of 1 ns. A functional analog calibration has also been implemented to allow checking of the complete readout chain. This has already been useful during the test beam operations.

6. THE FRONT-END ELEMENTS

The purpose of those elements is to shape the PM pulses in less than 25ns to avoid electronics pile-up. The characteristics aimed for are the following :

- At the input : the PM maximum current is 20mA over 25 ohms.
- At the output : the ADC input dynamic range is 1V under 250 ohms.
- The residue after 25ns should be smaller than 1%.
- The sampling area should cover +- 2nsec with a 1% precision.
- The RMS noise should be < 1 ADC count (250uV).
- Because of the shaping and limited integration time, the fluctuation on the useful number of photoelectrons is increased compared to the case of a full integration. This increase should remain smaller than a factor $\sqrt{2}$.

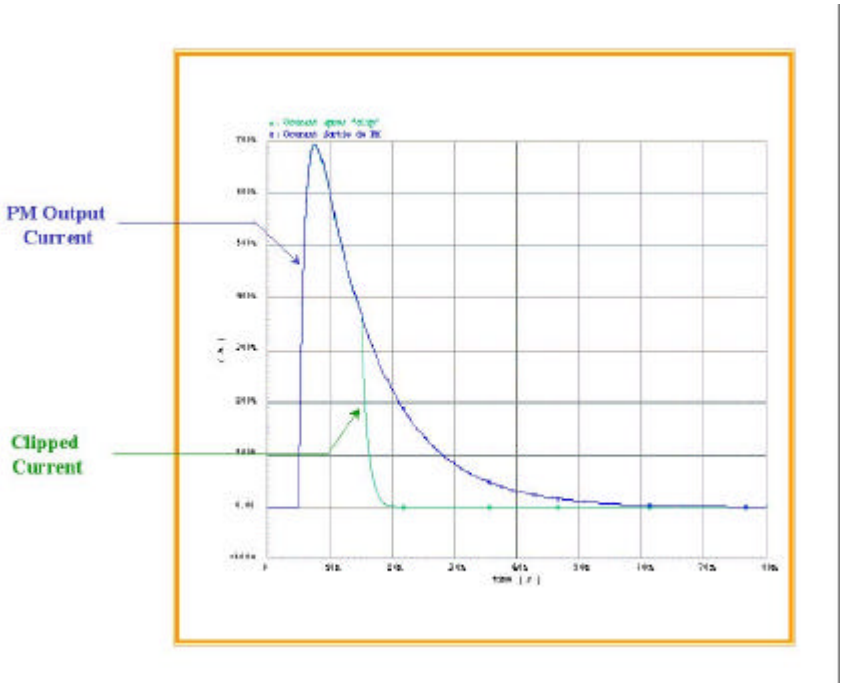

Fig 3 : PM output pulse

To fulfil the above requirements, two problems have to be solved. The first one concerns the PM signal. If one looks at Fig 3, which shows an idealized PM signal, the PM output current has a fast rise time but a slow decay that goes over at least the two consecutive samples at 40 MHz. It thus needs to be pulled to zero after 10ns to ensure the zero pile-up requirement. The remaining area is on the order of 60% of the original one.

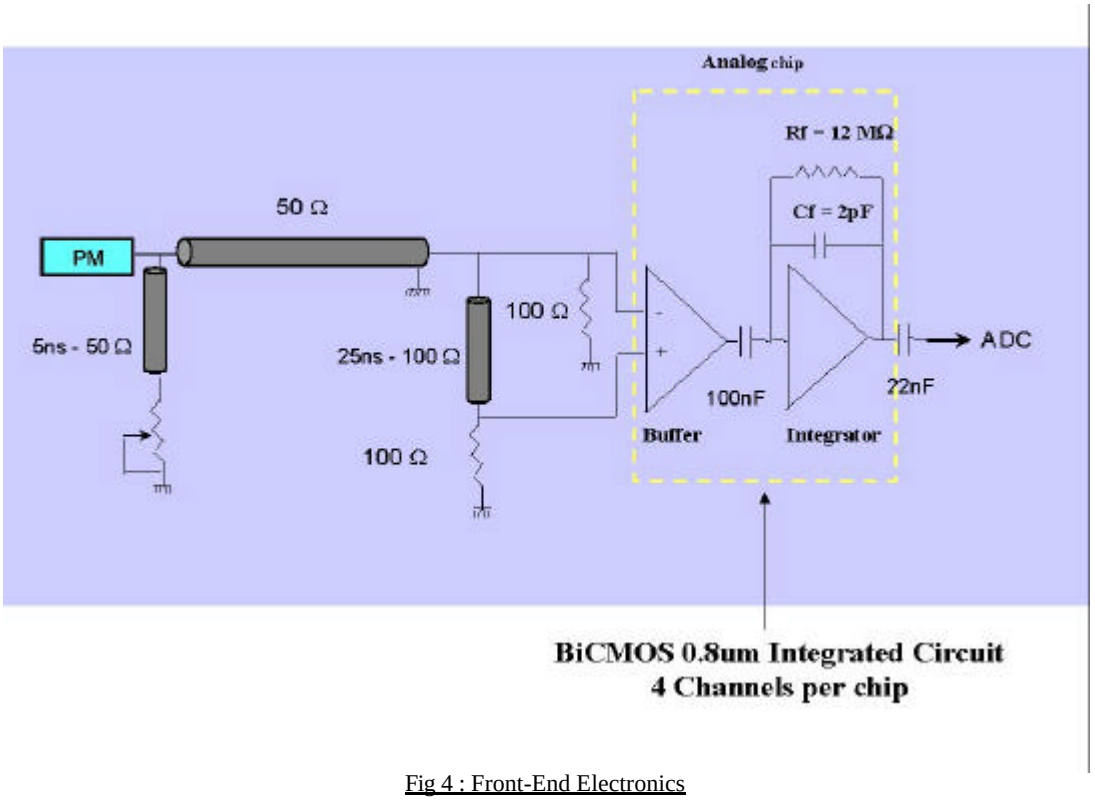

Fig 4 : Front-End Electronics

To realize this cut on the signal, the clipping circuit on the left of Fig 4 will be used. It consists in a short 5 nsec cable located at the output of the PM base. It sends part of the signal towards a variable network which will send back a inverted part of the signal. As both the source and reflected signals are, on average, negative exponentials, their superposition gives an almost zero signal, as shown on fig 3.

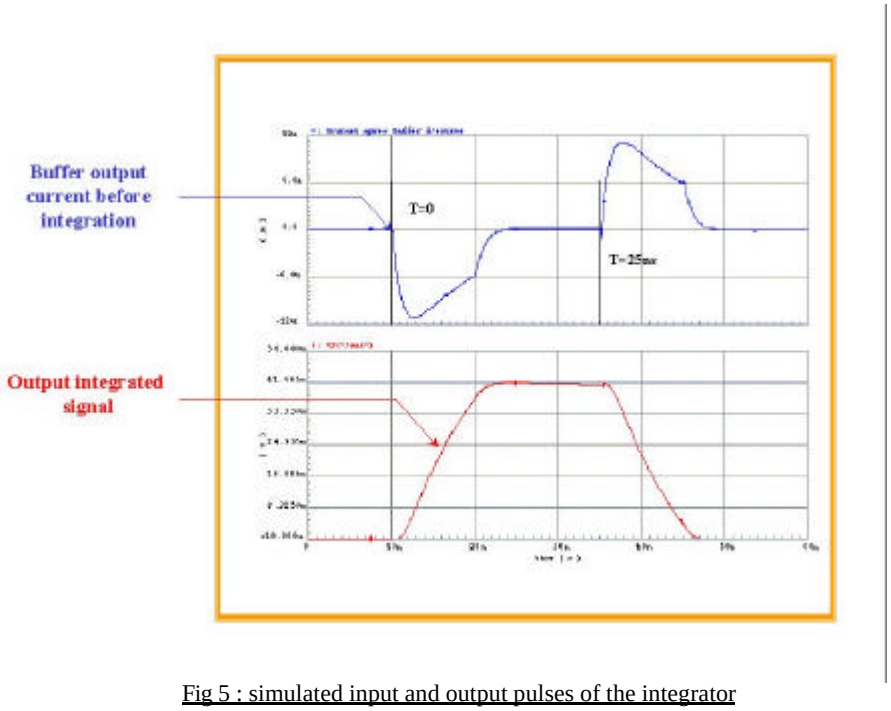

Fig 5 : simulated input and output pulses of the integrator

Now that the input signal has been shaped, we have to measure the energy deposited in the calorimeter. The corresponding information is the area of the PM signal. The best way to measure it without deteriorating too much the statistic fluctuation is to integrate this signal in a capacitor (Cf). The difficulty then becomes to empty this capacitor. Two ways are possible :

- Use a switch mounted in parallel but this system induces a dead time when the capacitor is being emptied, what implies the use of two integrators in parallel and a multiplexor. But due to the inevitable injection of charge from the switches, pedestals are generated which can be the sources of drifts at the 0.1% level.
- Subtract in a linear way the signal to itself thanks to a specific configuration.

The latter is the chosen solution. The configuration appears in the middle of Fig 4. The input signal of the analog chip is diverted, delayed by 25ns, then subtracted to itself thanks to the differential buffer. The latter has also in charge the division of the input current to adapt it to the small value of Cf. This solution is the one already proposed in the technical proposal [2].

Between the buffer and the integrator, there is an external AC coupling that allows to separate the DC levels. The integrator has a fast risetime and offers a satisfactory plateau at the top of the signal (see bottom plot of Fig 5).

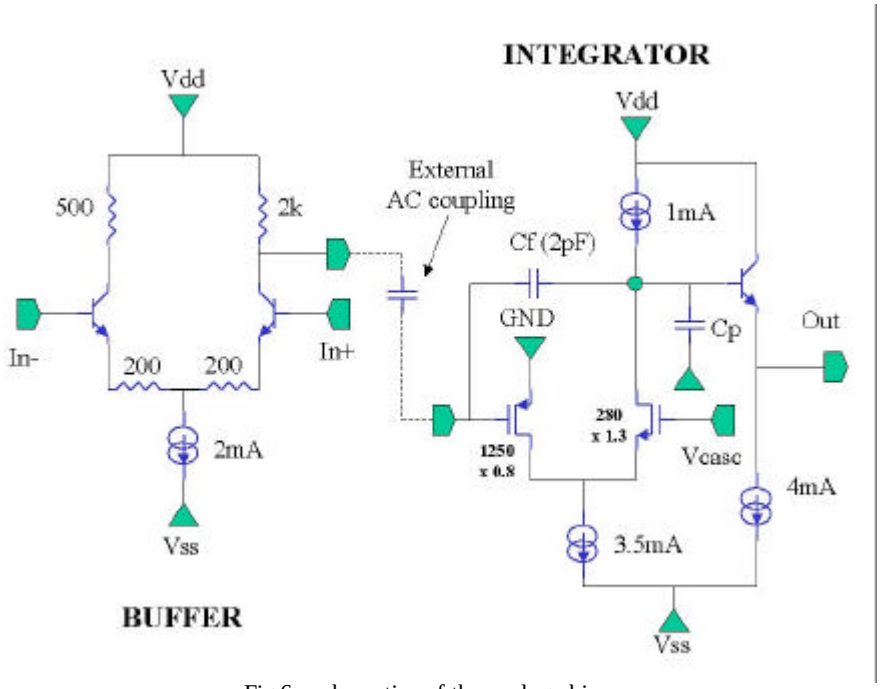

Fig 6 : schematics of the analog chip,
(a version with Cf = 4pF is foreseen)

Fig 6 shows the schematics of the analog chip. The 2K resistor at the output of the buffer is used for replacing a 1mA current source that would never match exactly the half of the emitter source current and produce more noise with the same power supplies than the resistor. Obviously, the buffer provides essentially a current output as the input impedance of the integrator is small (200 ohms) compared to the 2K of the resistor.

The integrator schematics is based on a cascode amplifier. Its open loop gain is high (60dB), it's fast as there is no Miller effect on the input PMOS, and it produces very low noise. On the other hand, there is a need for an emitter follower at the output not to degrade the gain by the charge impedance. In our case, as the charge is only 350 ohms, another follower has been mounted on the board using discrete elements. The decay time of the integrator is linked to the 2K resistor which leads to a nominal value of 4us.

The 350 ohm charge is composed of 250 ohms which is the ADC input impedance and a serial 100 ohm resistor. The latter prevents the ADC saturation at 1V from affecting the integrator. The resulting effect is a division of the signal by a factor 1.4.

Fig 7 shows the layout of the current version of the analog chip. Up to now, three versions have been submitted. The main difficulty that appeared was a resistor in the gate access to the input PMOS of the integrator. This was due to a bad polysilicon design and introduced noise and instability in the chip response. This problem was fixed and the chips received in the summer of 1999 were fully operational. When mounted on test bench at LAL, the chip offered the results shown in Fig 8.

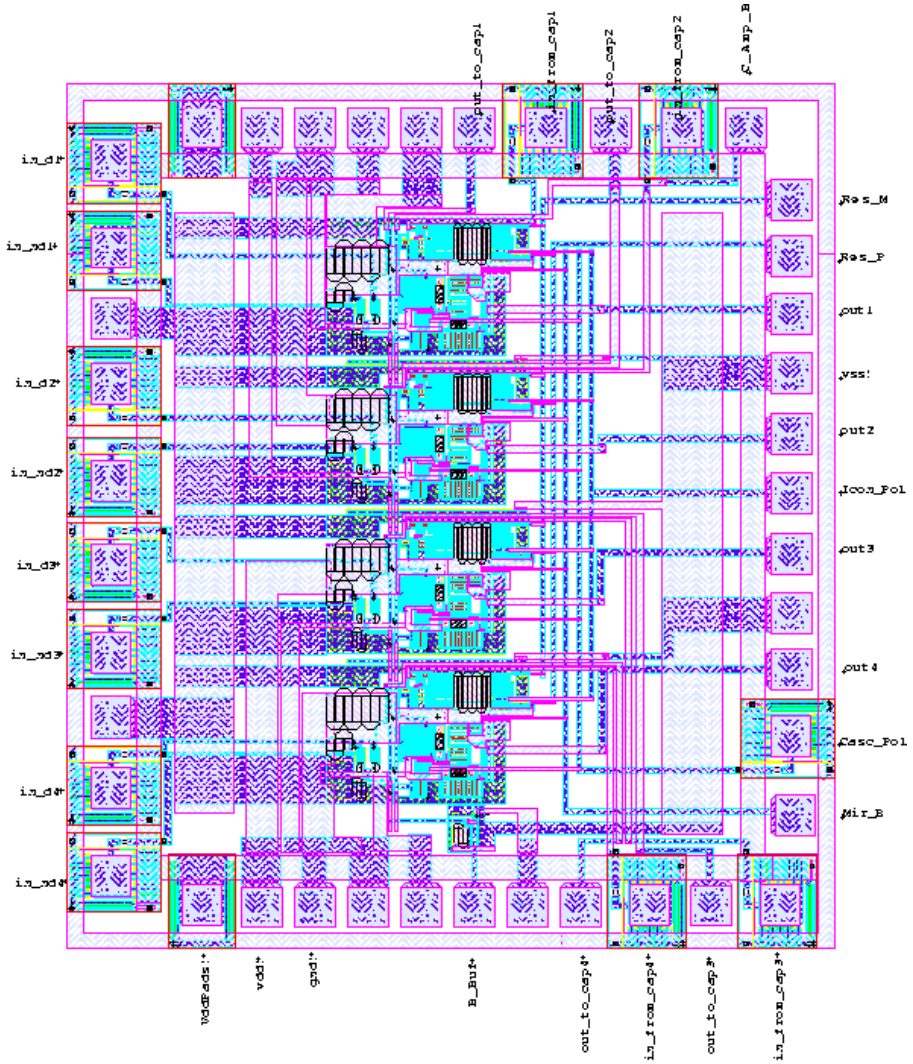

Fig 7 : layout of the analog chip

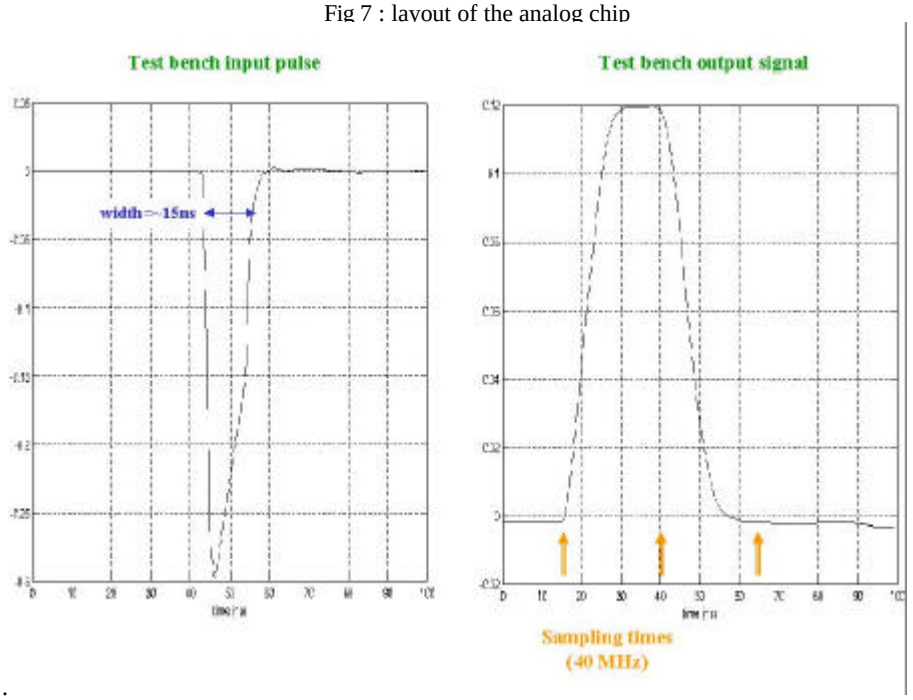

Fig 8 : real signals on test bench

On this plot (Fig 8), the input pulse derives from a generator and is clipped as the real PM signal. The output signal shows a nice flat top in concordance with the simulations. The global preliminary results from this test bench are given in Fig 9.

Simulation Results :		**Current Test Bench Results :**
Dynamic Range : 1.4V	⇔	> 1.4V
Non Linearity : 0.5%	⇔	< 1% over the whole dynamic range
Residue after 25 ns : < 0.5%	⇔	< 1% (undershoot ~ 3%)
RMS Noise after 1 ADC Channel	⇔	1.2 ADC Channels
Subtraction (ie 250uV)		(ie 300uV)
Power Consumption : 40mW/Channel	⇔	(38mW/Channel
Open-Loop Gain : ~ 60 dB	⇔	~ 60 dB
gm (Input PMOS) = 34mA/V		gm (Input PMOS) = 18mA/V
Fall Time : 3 us	⇔	2 us
Rise Time : 2.5 ns	⇔	5 ns
		With a 8pF parasitic capacitance at the integrator input
Input Impedance : 190Ω	⇔	270Ω
Deterioration of statistic fluctuation < 1.4	⇔	< 1.2

Fig 9 : first results from the test bench

These results show a good adequation between simulation and real circuit, except for the gm of the input transistor. This is due to simulation models and also explains the mismatches in the rise time and the input impedance of the integrator.

7. THE PROTOTYPE FRONT-END BOARD

The prototype FEB shown on Fig 10 is a 16 channel board which has been designed for the test beam of 1999. It comprises the same readout chain excepting the L1 buffer. Moreover, some extra functionalities as the spying of the raw data at the output of the ADCs have been implemented. This allows to crosscheck offline the subtracted data with their source.

Another interesting purpose of this board is the configuration state machine implemented in the VME interface Altera. It allows to configure all the other FPGAs on the board in an interactive way, permitting to debug the board easily (even far from home through ftp) and also to modify the functionality of the FPGAs for test purposes.

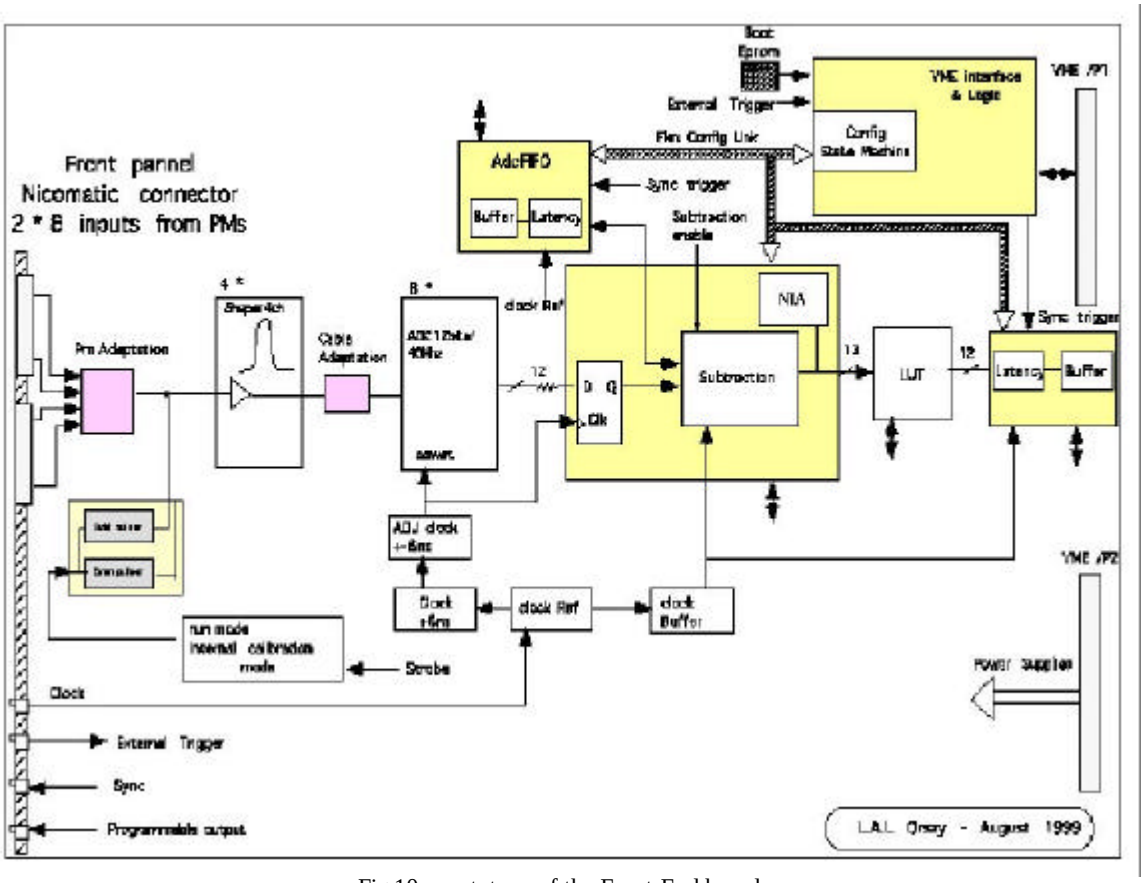

Fig 10 : prototype of the Front-End board

Fig 11 offers a picture of the board. On the left side, one can see the 2 x 8 channel input connectors, followed by the PM and cable compensation networks and the delay lines. The four 4 channel analog chips are followed by half the ADCs and the LUTs. All the big FPGAs (10K50 and 6K16) are on the other side of the board, together with the other half of the ADCs.

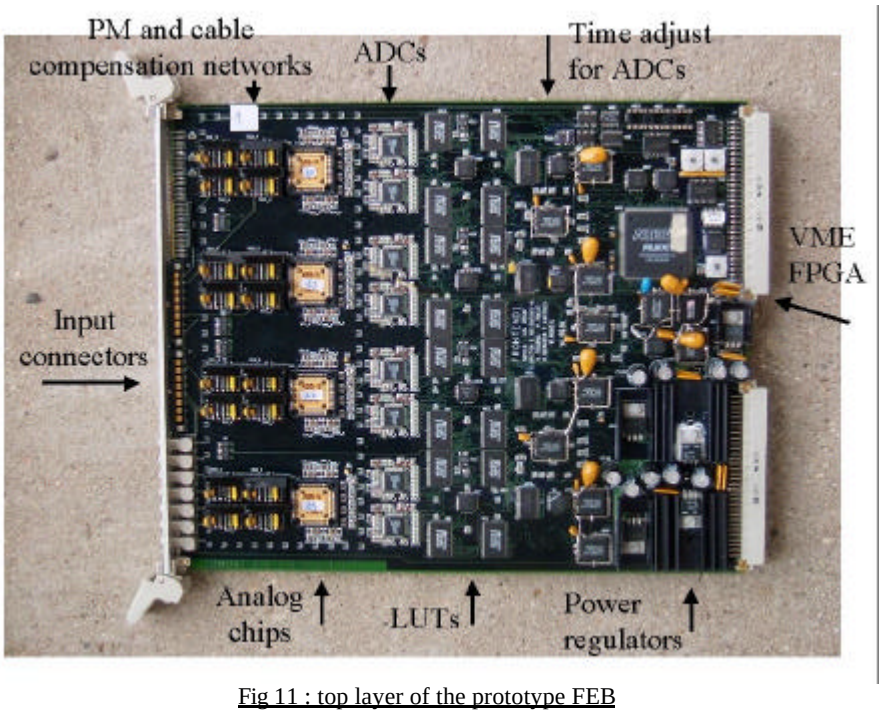

Fig 11 : top layer of the prototype FEB

8. THE TEST BEAM ENVIRONMENT

This board was installed on test beam in the setup shown in Fig 12.

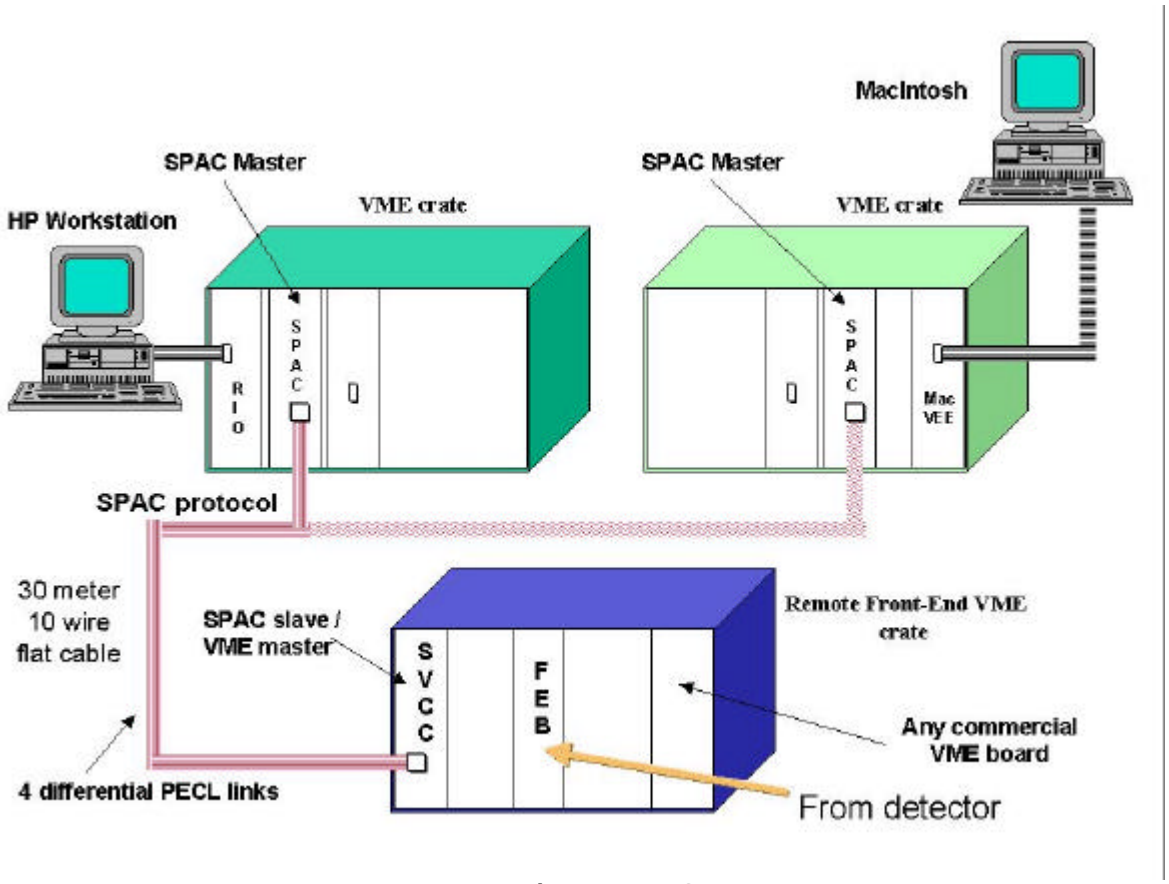

Fig 12 : test beam setup at CERN

One can remark here that two VME master crates can alternatively be connected to the remote electronics. This is intended for debugging and monitoring purposes. Indeed, when electronics is installed at CERN for test beam, local DAQ still needs to be debugged. The MacIntosh interactive test software, which also provides data acquisition, and the possibilities of live insertion of the SPAC bus[4] thus allow to start the debugging phase of the hardware while permitting crosscheck of the readout data with the one read by the standard DAQ.

9. TEST BEAM RESULTS

The first measurements made on test beam were related to the signal coming from the PMs. It is plotted on top of Fig 13.

One can remark that the width of the signal is larger than on test bench. This was due to an underestimate of the risetime of the PM and of the light output from the scintillator and the wavelenghtshifting fiber in the test bench simulation. Nevertheless, the shape at the output of the integrator (bottom plot) looks adequate with a flat top within 1% for +-2nsec.

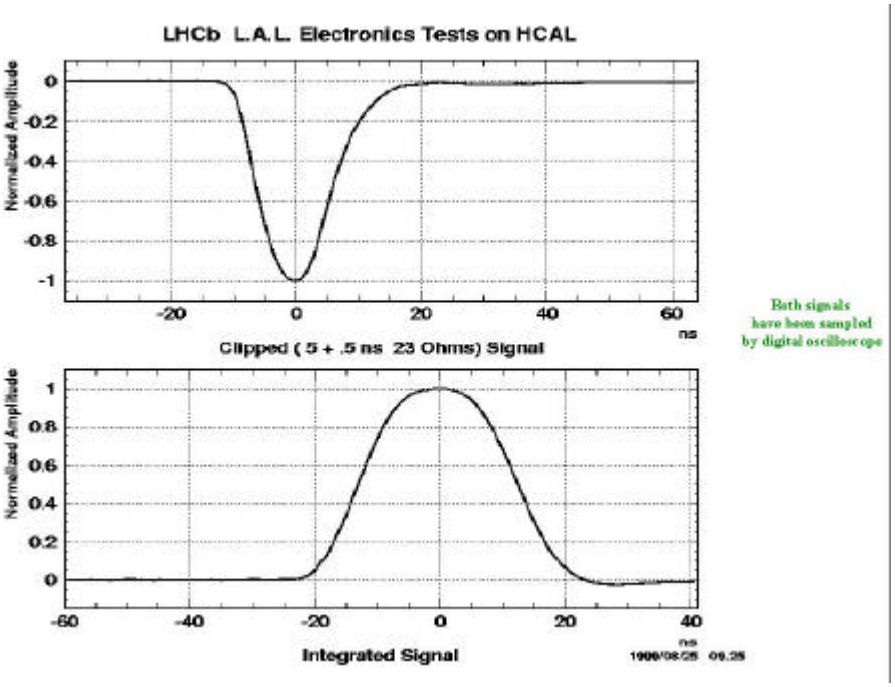

Fig 13 : real signals on test beam

The following step was to compare the new 40MHz electronics with the CAMAC LeCroy one. Data was thus taken on the same channel through the two different paths. The comparison is plotted on Fig 14.

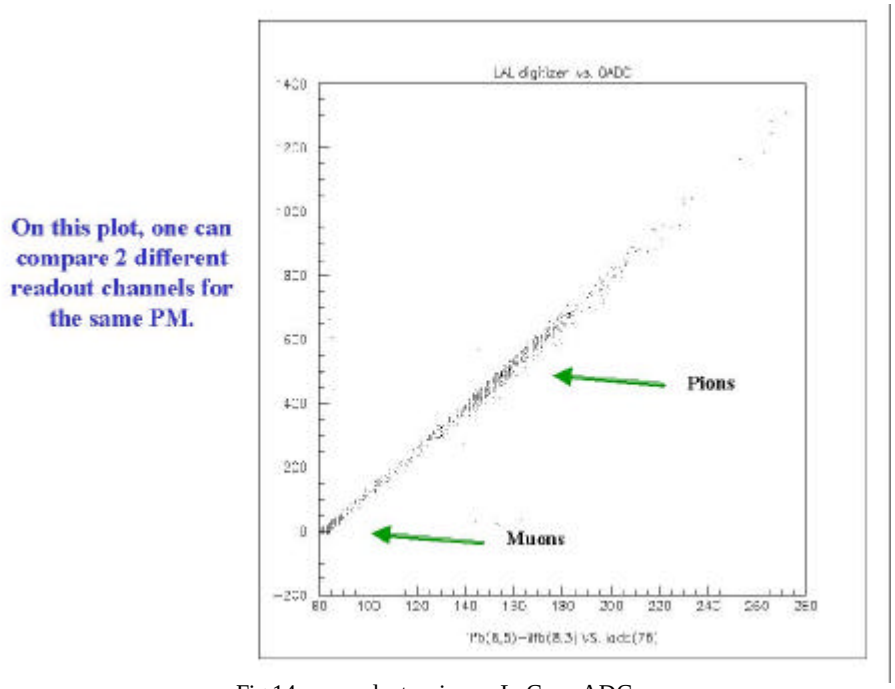

Fig 14 : new electronics vs LeCroy ADCs

Fluctuations from a strict correlation are caused by noise of the 40MHZ and Lecroy ADC and by the deterioration of statistical fluctuation from the fast electronics (see Fig 9).

Fig 15 presents the results of an ECal run. 6 samples are plotted successively. The signal is centered on the sample 5 (third one). On the sample 3, one can observe the noise distribution. This corresponds to a RMS of 1.86 ADC count.

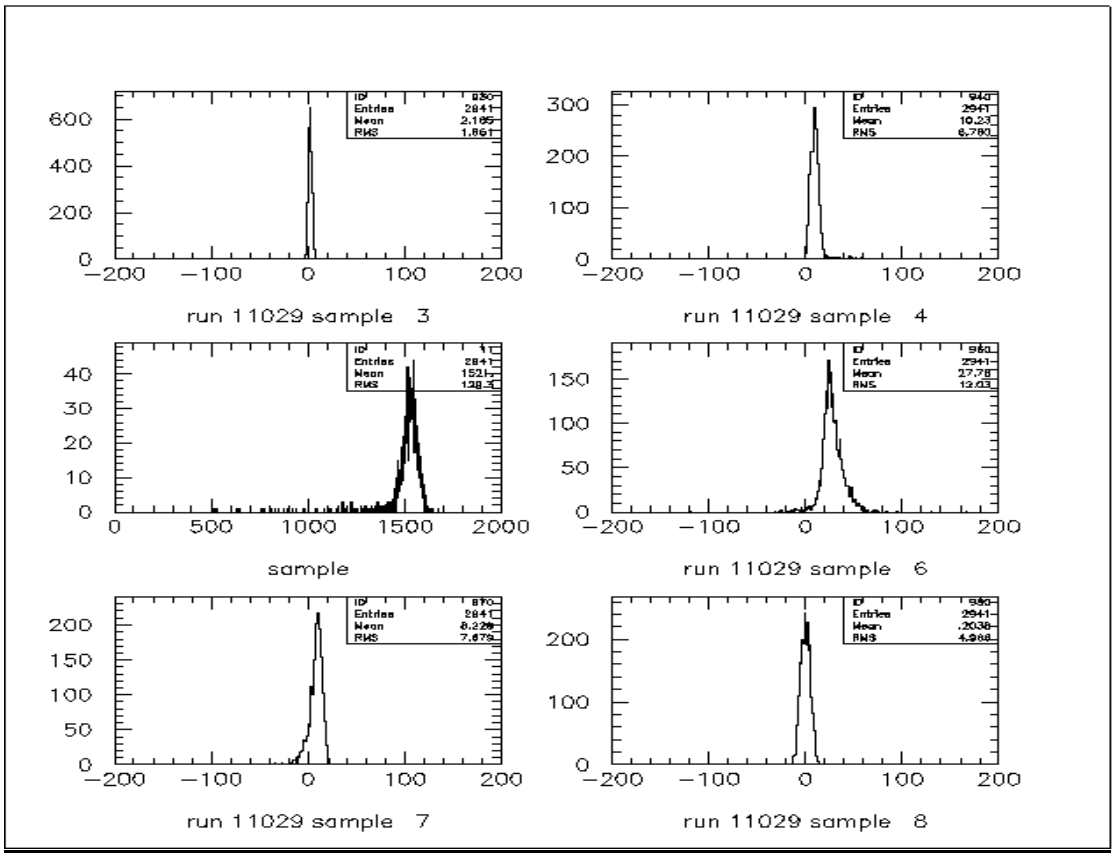

Fig 15 : 6 samples from an Ecal run

On the samples 6 and 7 appears the result from the subtraction of the smallest of the two previous samples. On sample 8, we're back to the baseline. The effects on samplings other than the main one are typically at or below the 1-2% level.

10. NOISE AND CROSS TAL, FURTHER TESTS

a) Noise

The noise levels were measured on the card after the test beam period and after improvments obtained by better decoupling of the amplifier Vdd and Vss and by inserting current limiting resistor at the digital ADC output to reduce the feedback of the ditigital commutation. From the observation of the noise pulses values x_{ij} - $\bar{x}$ on n channels and m events on can calculate

$$S_1 = \sum_j^m \left(\sum_i^n x_{ij} - \bar{x} \right)^2 = m(n^2 \sigma_{coh}^2 + n \sigma_{incoh}^2)$$

$$S_2 = \sum_j^m \sum_i^n (x_{ij} - \bar{x})^2 = m\ n(\sigma_{coh}^2 + \sigma_{incoh}^2)$$

From these values the coherent and incoherent noise are extracted.

It is useful to study the noise contribution as function of integration time. In order to do this, the substraction of a preceding sample is done by software and one substracts the value measured 25, 50...250 nsec before, thus varying the effective integration time.

The result of such a procedure is presented on fig. 16 for the incoherent noise and fig. 17 for the coherent noise. As expected (for the noise produced before the integrator) the incoherent noise grows as the square root of the integration time t with however a residual at t = 0 of about 0.5 ADC count (obtained by extrapolation). This last number represents the contribution of noise internal to the integrator or generated after the integrator (at the ADC input).

The measurement can be fitted by

$\sigma_{incoh}^2 = (0.5)^2 + (0.27)^2$ x t nsec

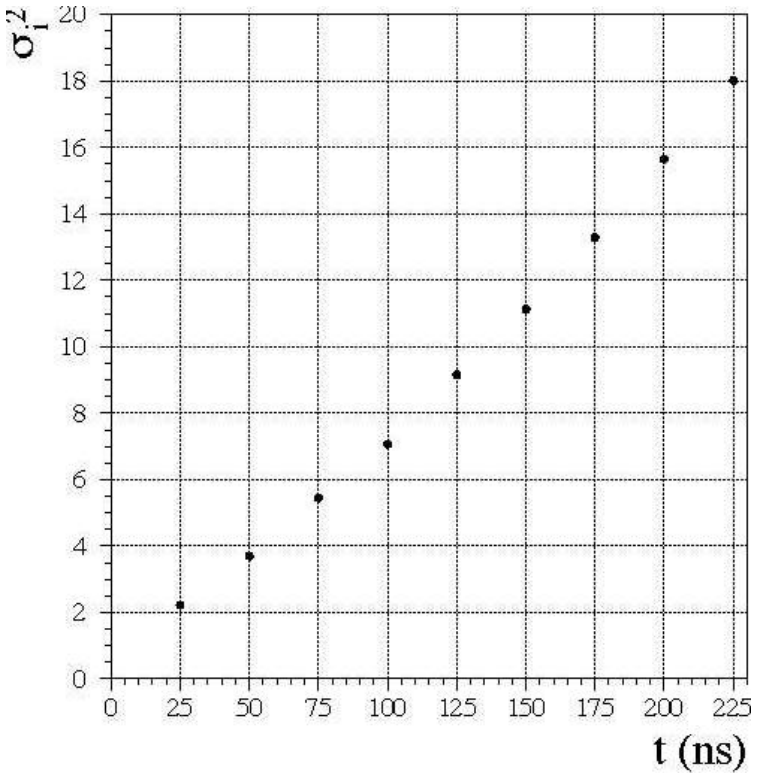

Fig 16 : incoherent noise as function of effective integration time

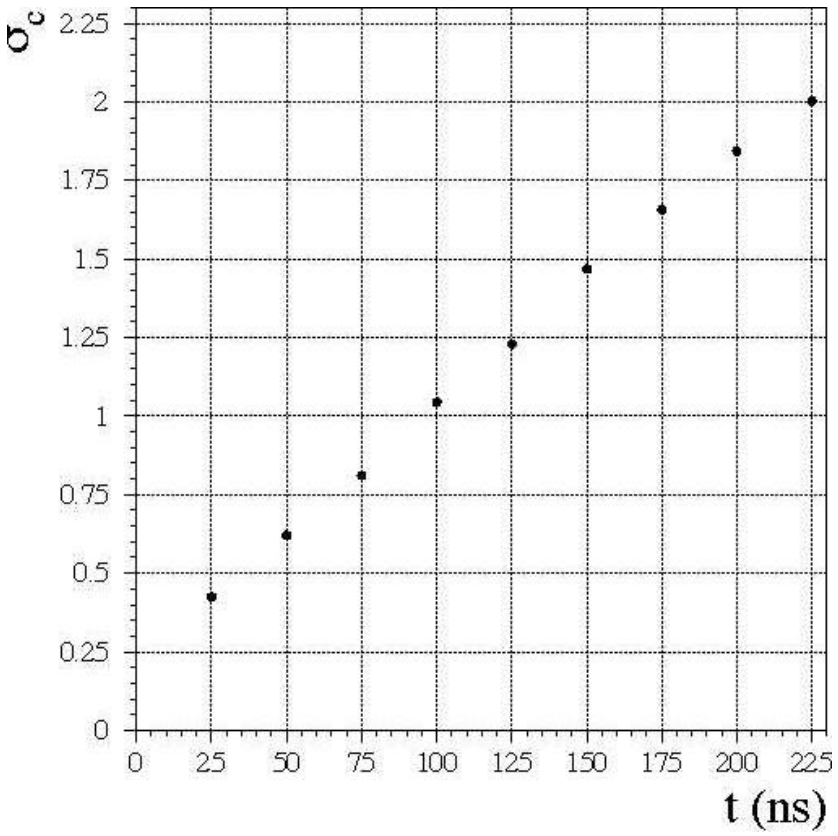

Fig 17 : coherent noise as function of effective integration time

A similar analysis on the coherent noise (fig. 17) shows that it varies linearly with integration time as expected if its source is from frequencies much lower than 40 MHZ

$\sigma_{coh} = 0.22 + 0.008$ t nsec

In the foreseen mode of operation, in which the smallest of the two preceding samples is substracted is the card, the numbers above result in a coherent noise of 0.52 ADC counts and an incoherent noise of 1.6 ADC count. This last number is in

agreement, within 12 % with the noise value measured with the single chip test bench (fig. 9). It is hoped that in a next version of the chip with a 4 picofarad integrating capacitor the incoherent noise can be reduced to 1 ADC count.

b) Crosstalk

The crosstalk between the 4 channels of a ship were found to be typically < 0.5 %. However in one combination (channel 4 to 3) a 1.5 % crosstalk has been found. This has been traced to a 30 femtofarad stray capacitance in the chip layout between the output of channel 4 and the input of channel 3. Corrective measures are being studied.

11. NEXT STEPS OF THE DEVELOPMENT

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The next steps of the developments for this electronics are the following :

- Concerning the Front-End Board :
  - A new version of the analog chip aiming at a reduced noise
  - Implementation of the trigger part of the board
  - Study of the L1 buffering hardware
  - Extension to a 9U/32 channel board
- Study of the fast backplane using LVDS signals
- Study of the Event Filter (which provides advanced zero suppression and event formatting)
- Study of the Crate Controller (which includes serial access bus and TTC)
- Study of the Trigger Validation Board (which prepares the candidates for the L0 trigger Main Selection Crate)

12. ACKNOWLEDGMENT

The idea of using a double signal with a 25 nsec delay line was proposed by our IHEP collaborators. We wish to acknowledge the essential contribution of A. Schopper of Cern, A. Konoplianikov, R. Djeliadine of IHEP, A. Golutvin, V. Rusinov, E. Tarkowski of ITEP to the test beam measurements.

13. REFERENCES

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[3] C.Beigbeder et al., “A Joint Proposal for the Level 0 Calorimetric Triggers”, LHCb 99-017, June 7th 1999
[4] D.Breton et al., “SPAC : Serial Protocol for the Atlas Calorimeter “, www.lal.in2p3.fr/technique/se/spac