The Front-end Electronics for the Calorimeter Triggers

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INTRODUCTION

This document describes the first stage of the L0 calorimeter trigger, implemented on the front-end boards. The evolution of the L0 calorimeter trigger since the Technical Proposal [1] can be followed through several LHCb notes:

1. 'The LHCb Calorimeter Trigger and its implementation with the 3D-Flow system' [2]. This proposal is based on a multi-layer processor approach, using custom ASIC, and has not been retained by the collaboration.

2. 'An alternative high PT electron and hadron trigger for LHCb' [3]. A synchronous L0 trigger is proposed that is based on the search of local maxima of transverse energy E_T. The algorithm requires that the sum of a group of 2x2 cells be the highest in a large area of 8x8 cells.

3. 'An Update of the 2*2 Implementation for the Level 0 Calorimeter Triggers' [4]. In this note a detailed description of the data flow and hardware implementation of the trigger proposed in Ref. [3] is given.

4. 'Proposal for a Level 0 calorimeter trigger system for LHCb' [5]. An alternative system for the L0 calorimeter trigger, derived from the electromagnetic pre-trigger of HERA-B is presented. The proposed system is also synchronous, but the algorithm performs a shower analysis based on a 3x3 calorimeter matrix.

5. 'A joint proposal for the level 0 calorimetric triggers' [6]. This note describes a complete system for the calorimetric L0 trigger, that is based on ideas from the two proposals [4] and [5]. The system, as described in this note, was approved by the collaboration in June 1999.

It is worth mentioning several changes that have occurred since the previous documents were released:

1. The MU1 chamber is no longer used to identify that an electromagnetic cluster is charged or neutral. Instead a new detector, the Scintillator Pad Detector (SPD) is used. The SPD consists of a plane of scintillator pads with the same shape as the PreShower and is located in front of the lead of the PreShower. Like the PreShower, the SPD is read out using PMTs. However each channel has a discriminator that produces a single bit of data per cell and this is read out into the PreShower front-end card. In total the PreShower generates two bits of information for the trigger, the one from the PreShower itself and the other from the corresponding SPD.

2. Originally, it was assumed that the whole PreShower and SPD information is sent to the ECAL Validation Card. In order to simplify the connectivity and to reduce the cost it has been decided to send from the ECAL front-end card the information that identifies the area of interest to the PreShower front-end card. This selected information (twice 4 bits) is then sent to the ECAL Validation Card. It has to be stressed that this protocol preserves the synchronous character of this stage.

3. Previously ECAL information relevant to the HCAL trigger was available in the ECAL Validation Card. For similar reasons of simplifying the connectivity, this information is now sent directly from the ECAL front-end boards to the HCAL Validation Card.

In the present document, we describe the technical details of the first stage of the L0 calorimeter trigger, namely the selection of one candidate in each front-end card. This selection is performed in an identical way for both ECAL and HCAL. The design is based on commercially available components. However, mass production of these cards will take place only in 2003 and therefore some components, mainly the FPGAs, will probably be replaced by higher performance ones.

1. Principle of operations

The L0 calorimeter trigger is performed in three steps.

1. A local maximum is searched in each front-end card, covering an area of 4x8 cells. The quantity used is the transverse energy on the sum of an area of 2 by 2 cells. In order to compute the 32 sums, each

card needs to access an extra row and an extra column of cells. This part is performed on the front-end boards, and is described in the present note.

2. Once the maximum is selected on the front-end card, it is sent to a Validation Card, where information from other detectors is used. For ECAL, the SPD and PreShower information allows to classify candidates as electron or photon, or to ignore them. For HCAL, the transverse energy is corrected by the ECAL deposited energy, one adds in fact the ECAL local maximum which is in front of the HCAL candidate, if any.

3. The third step is to select the highest of the electron, photon and hadron candidates, possibly the second highest for some of the particle types, and to send them to the L0 Decision Unit.

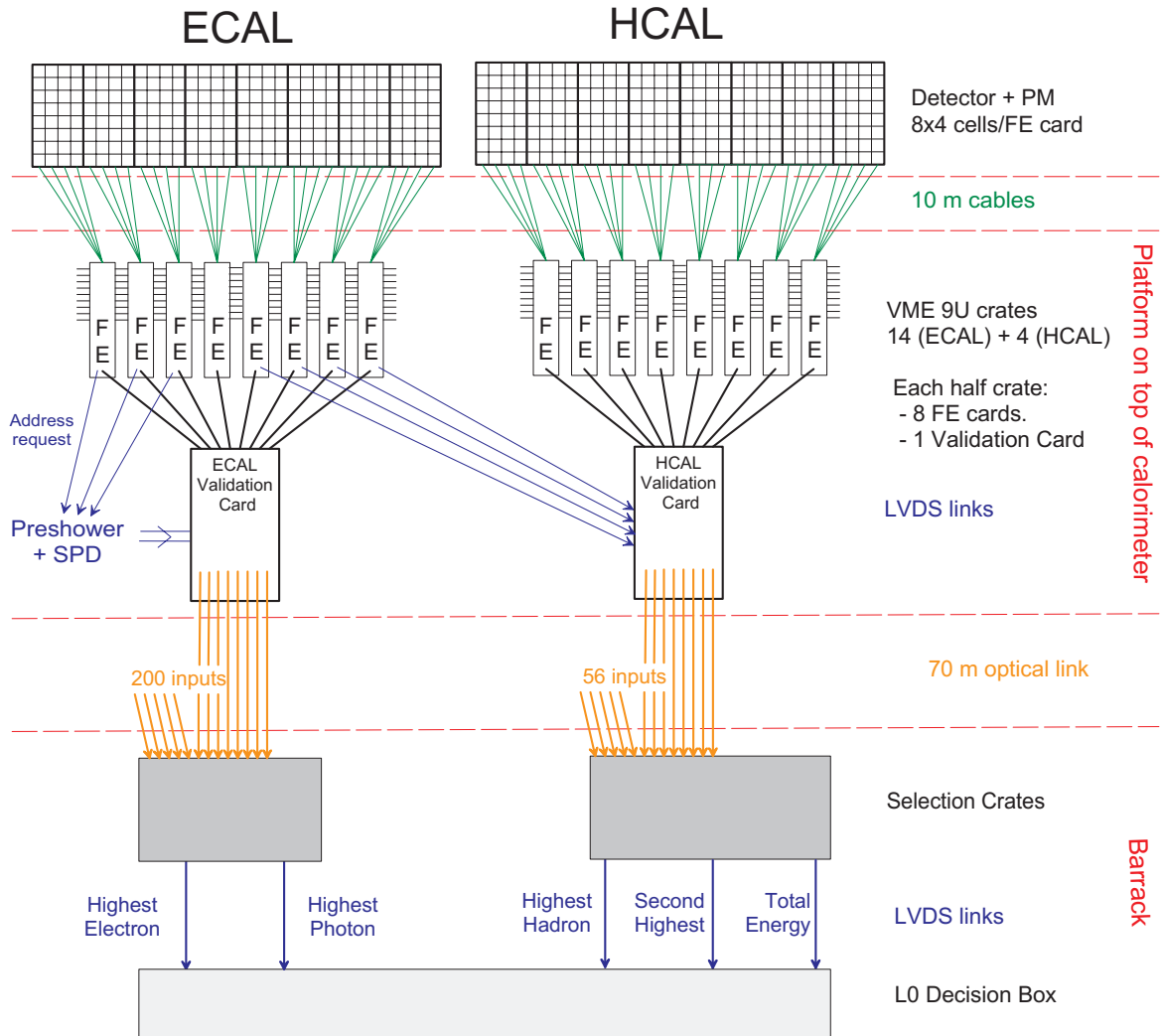The overall system is summarised in Figure 1.

Figure 1: Overall view of the L0 calorimeter trigger.

This note describes only the first step. It should be stressed that this step is identical for ECAL and HCAL: There is a single type of calorimeter front-end card, even if some connections are not used for the HCAL case. We believe it is better to have some unused features on part of the cards than to develop and maintain two similar but not identical types of cards. Nevertheless, we need to have a different card for the PreShower and the SPD, as described in Section 2.2.

2.   Overview of the front-end cards

2.1.   Calorimeter front-end card

The calorimeter front-end card has several functional blocks: Analog shaping, digitisation, pedestal correction, storage for L0 and L1 latency. And, of course, trigger processing. A global view of the card is shown in Figure 2 where the trigger part is located in the top right corner.
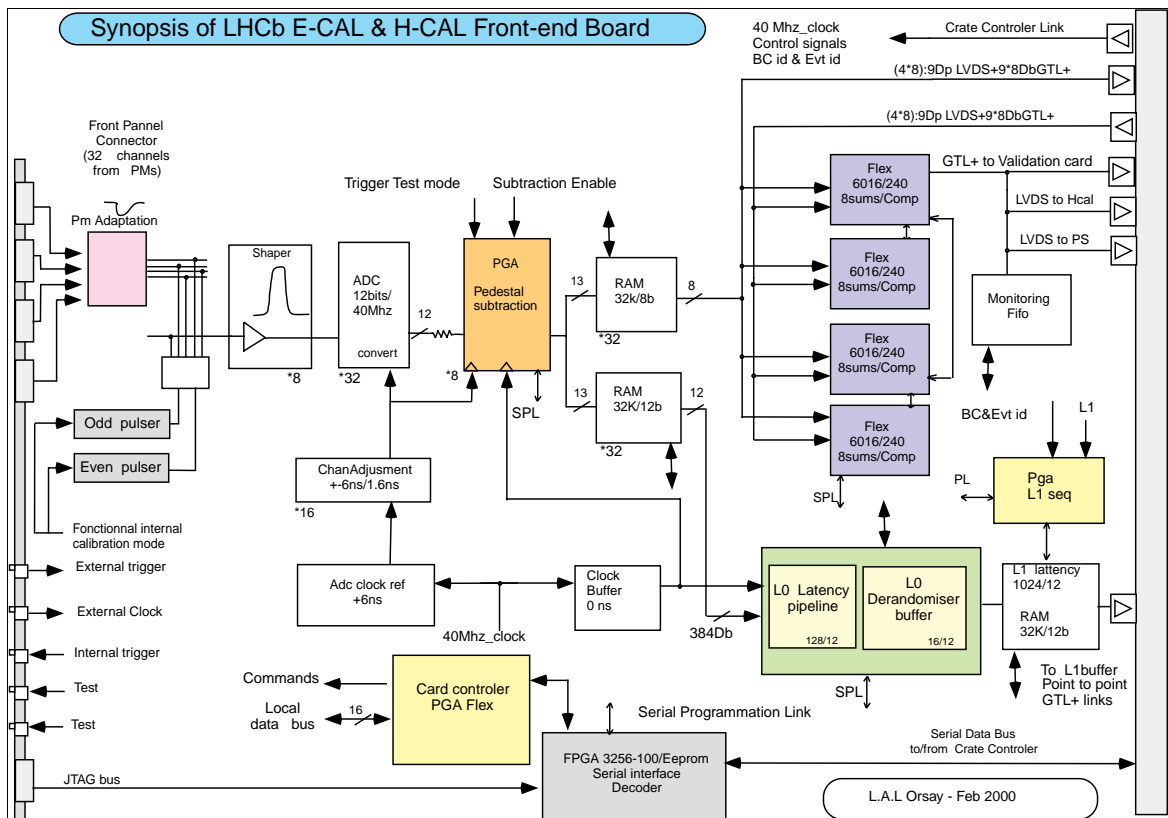

Figure 2: Synopsis of the Calorimeter front-end Card

A description of the front-end card can be found in [7]. After shaping and digitisation, a pedestal subtraction is performed in an FPGA, by subtracting the lowest of the two preceding samplings. This eliminates the low frequency noise, and gives a pedestal subtracted data. On the trigger branch, this 13-bit value is converted to 8 bit transverse energy E_T using a dedicated RAM as look-up table. Note that any type of transformation can be performed in this RAM, not only transverse energy. Several schemes have been proposed to improve the trigger, for example to take into account the magnet kick. What we call E_T in this note is the output of this RAM. This 8-bit information is summed for the 4 cells of each 2x2 area, and the highest of these 32 sums is selected as the candidate from this card. The output of this RAM should then be additive, as the E_T value for the candidate is the sum of the E_T values of its four cells.

In order to compute the 2x2 sums for 32 cells the card needs to access the information of an extra row and an extra column, which means 13 extra cells. The information is passed by the backplane for the extra column, and using point to point LVDS links for the extra row. This is described in Section 4 and represented by the top right connections in Figure 2, the arrow indicating the direction of the signals. As the transmission takes some time, a delay is introduced for the local cells before all cells can be combined.

The output of the card is essentially the address and E_T of the selected 2x2 area. This information is sent to the Validation Card. In the case of ECAL cards:

- The same information is also sent to the HCAL Validation Cards. This allows adding the energy released in ECAL by the HCAL candidate. In about half the cases, the output should be sent to two HCAL cards, and two output drivers and connectors are available for that purpose.

- The address of the candidate is sent to the PreShower front-end card, which then sends the PreShower and SPD information for the 4 cells in front of the candidate to the ECAL Validation Card.

Note that, for HCAL cards, these connections are not used.

2.2. PreShower and SPD front-end card

The PreShower front-end card has a similar structure, with a different analog part and 64 channels instead of 32. The trigger part of the card performs the following operations on the 2 bits (PreShower and SPD) available per cell:

- Collect the neighbours, similarly to the ECAL-HCAL card.

- Wait in pipe-line mode for the information from ECAL

- Extract the two groups of 4x2 bits corresponding to the addresses sent by the two ECAL cards. As a card handles 64 channels, there are two ECAL addresses received per card. One can see the physical card as handling two logical cards, each of them matching one ECAL card.

- Send these two groups of 8 bits to the ECAL Validation Card.

Note that the processing is fully synchronous, working in pipeline mode, with an address received and an answer sent at 40 MHz.
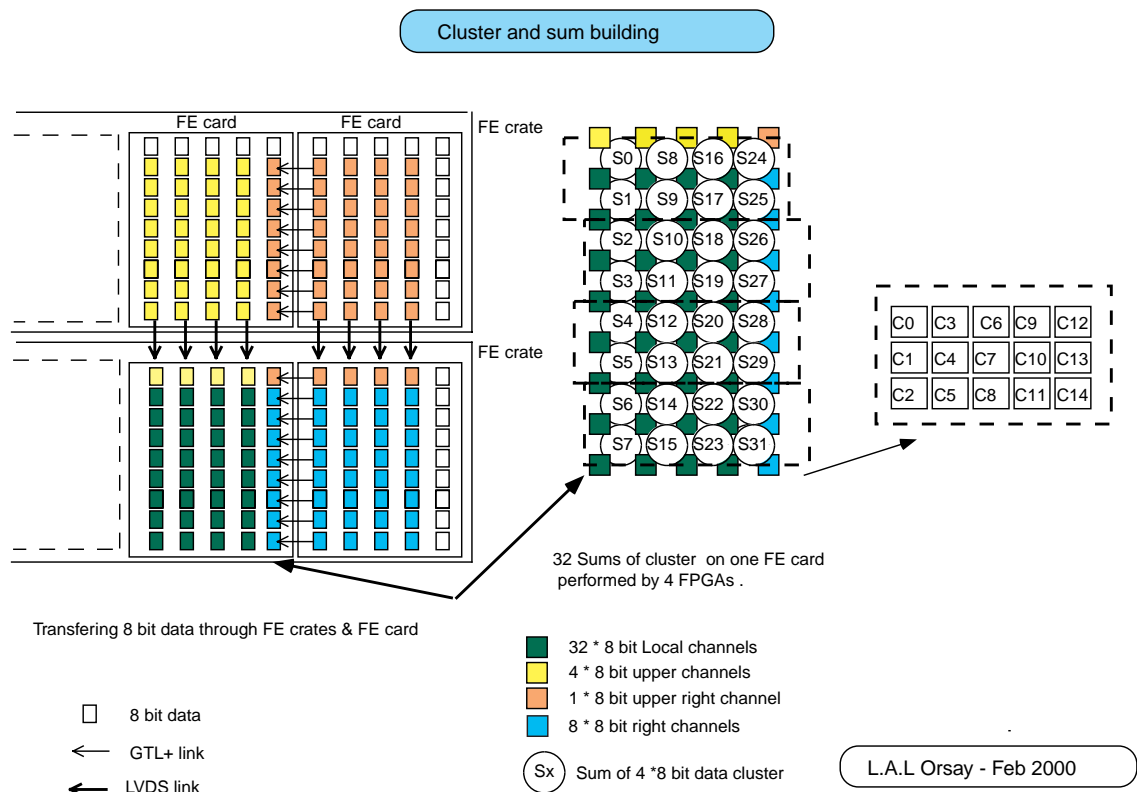
3. Sum and selection

Figure 3: Cells and sums

Figure 3 shows how the sums are performed. The left part depicts how the cells are available on four front-end cards, and how the bottom left card works. 32 cells are on board, four are coming from the upper board, 8 from the right board, and the last input comes from the upper right board via the right board, in two steps. Each step takes one clock cycle, so the 32 on-board cells have to wait two cycles, the 4+8 simple neighbours have to wait one cycle and the corner cell is used immediately. After this wait cycle, the data are all in phase, and the whole processing will proceed in a synchronous way, in pipeline mode.

The processing is performed in 4 identical FPGAs ALTERA 6024-1. They are of the same type, and have the same internal code, for easy downloading and maintenance. As shown in the right part of Figure 3, each FPGA will process 8 sums, and needs to receive 15 inputs. The bottom three FPGAs have the same timing pattern for the neighbour inputs, only the top one is different, as the cells coming from the top card are available only later. A digital level on one input pin will select which delay pattern to use. In the current design based on available FPGAs, we use 185 of the 199 pins, and 700 of the 1960 logic cells, but the input delays are not yet included. However, for the final implementation, we intend to use the Apex family with BGA type connectors, up to 984 pins. They are recent and more delicate to use, but will allow us to use a single FPGA for this sum and selection, avoiding lines on the board, and saving several clock cycles (see later). They are also cheaper, have a GTL+ bus interface included and maybe LVDS lines. Nevertheless, this note shows that we can already implement the system with available ALTERA 6024-1 circuits

The operations performed inside each FPGA, excluding the initial delays to time-adjust the inputs, are identical and displayed in Figure 4.
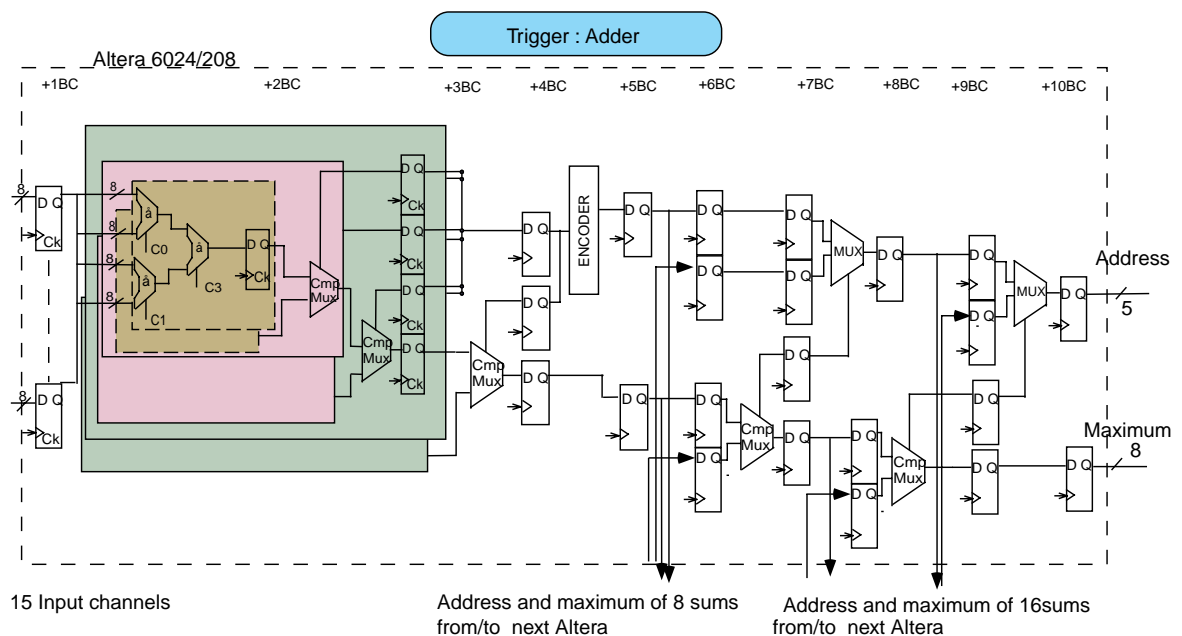
The 32 2*2 sums are compared and the highest one selected by 4 FPGAs. This is performed in 10 clock cycles, without taking into account the time. to get the neighbour information

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Figure 4: Logical diagram of one of the 4 FPGA

- First, the inputs are summed to replace the 3x5 inputs by 2x4 sums on a 2x2-cell area. This is performed in two steps taking only one clock cycle, to get the 8 sums on 8 bits. The sums are saturated, which means that if any intermediate result is greater than 255, the output is forced to be 255.

- A second step is to compare the 8 values inside the FPGA. A first comparison of 4 sums is performed in one clock cycle, between +2BC and +3BC, the comparator decision being sent to an encoder which builds the address of the highest of the four. The next comparison, to select the highest of the two

groups of four is performed in another clock cycle. The result of the comparisons gives the address and the value of the highest sum, available at +5BC.

- At this time, the data are exchanged between FPGAs, to get the highest of the candidates selected by each FPGA. This is performed in two steps, first by comparing the neighbour (only two FPGAs are active), and then by comparing the results of these two FPGAs on a single active FPGA. The FPGAs are identical, only the tracks on the boards are different so that the proper neighbours are connected. It may be possible to do these operations in all FPGAs, and compare the results, to detect possible corruption of the system.

The code for the FPGAs has been produced and tested, and can be found in [8]. As mentioned earlier, it is likely that a single, bigger one will replace these four FPGAs for the final implementation. This will spare several lines on the board, and improve the latency by up to four BC.

4. Connections and Backplane

The trigger part of the front-end board consists mainly of the four identical FPGA described in Section 3. The inputs are from the LUT and from neighbours, as indicated in Section 2. The output is sent to several places, via the backplane or via dedicated connections. Backplane connections are using GTL levels with drivers like 74GTL16612, or direct GTL+ levels provided by the next generation of FPGAs. For the other connections, we will use serial multiplexed LVDS lines on high quality cables. The use of multiplexed lines allows decreasing the number of connection points: For the vertical neighbours, we send or receive 4x8 bits to or from the same location. These 32 bits can be transported on 9 pairs, using circuits like DS90CR483-484 for multiplexing and de-multiplexing. Two types of cables are needed:

- Short (2-5 meters) shielded cables with 10 pairs for the vertical neighbours.

- Somewhat longer (5-10 meters) shielded cables with only 5 pairs for connection to the PreShower and to the HCAL crates

All the connections are on the back of the card, using the scheme shown in Figure 5.
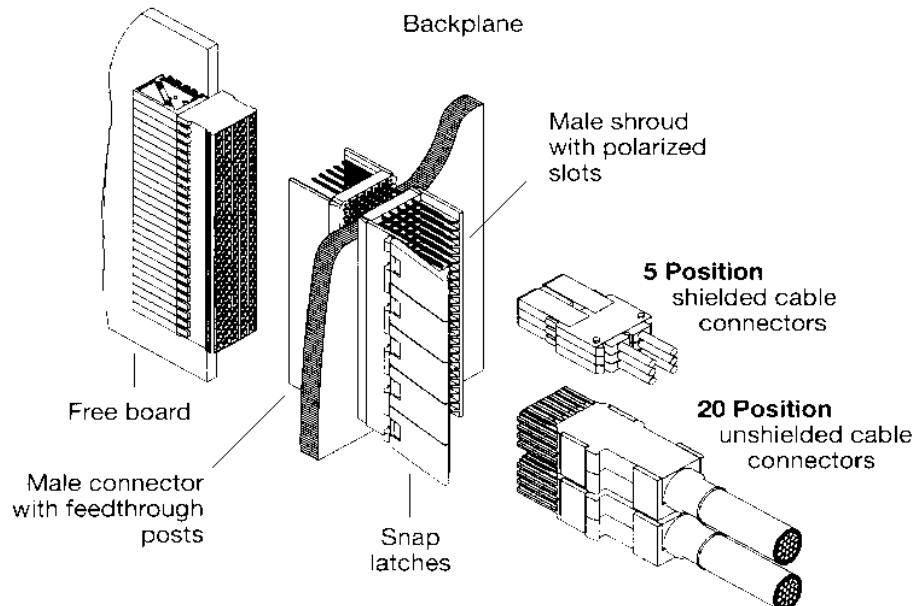

Figure 5: Principle of cable connections

We propose to use AMP Z-PACK 2mm HM connectors and cables, an example of these items is shown in Figure 6.
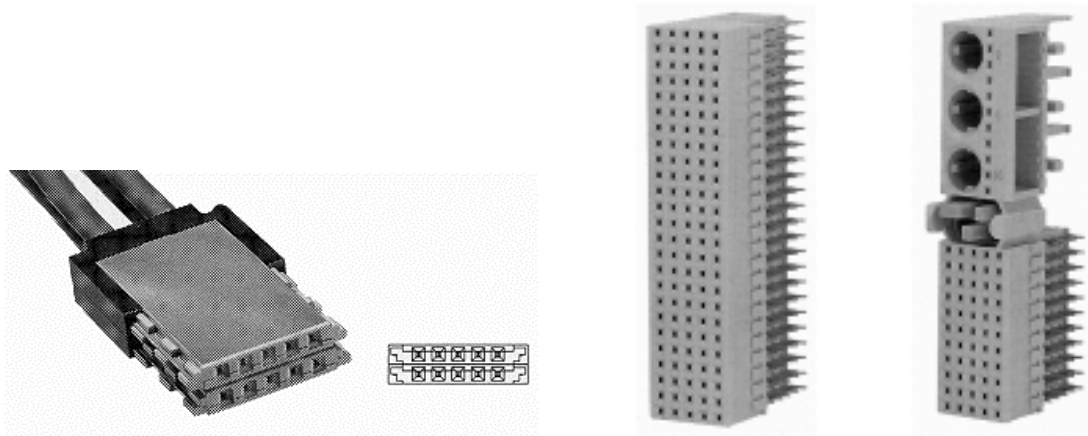
Figure 6: Examples of cable, signal and mixed signal-power connectors

Cables are shielded twisted pairs, as needed by the high bandwidth required by LVDS signals. The middle connector is soldered on the board of the front-end card. The connector on the right allows passing high current on its upper part, it will be used for power lines, with direct cable connections from the power supply to the slot.

The overall backplane design is shown in Figure 7. Each crate is equipped with a central readout card (Croc), two Validation Cards in the centre of each half, and up to 16 front-end cards. A Crate Controller card sits on the left of the crate to distribute the TTC signals, the clock (via isochronous lines), and the ECS (DCS) signals needed to download and monitor the cards. Four (or five) cables, indicated by a small box near each card, are connected to every front-end card: from and to vertical neighbours, result to HCAL (one or two cables) and address to the PreShower crate. The other connections are via GTL+ lines on the backplane: horizontal neighbours and result to one of the two Validation Cards. The ECAL Validation Cards receive also signals from the PreShower and SPD, and the HCAL Validation Cards receive data from ECAL, via LVDS cables in both cases.

The two types of cables we need have been quoted each to about 250 CHF fully equipped with connectors. The cost of cables per card is about 1100 CHF for ECAL and 500 CHF for HCAL.
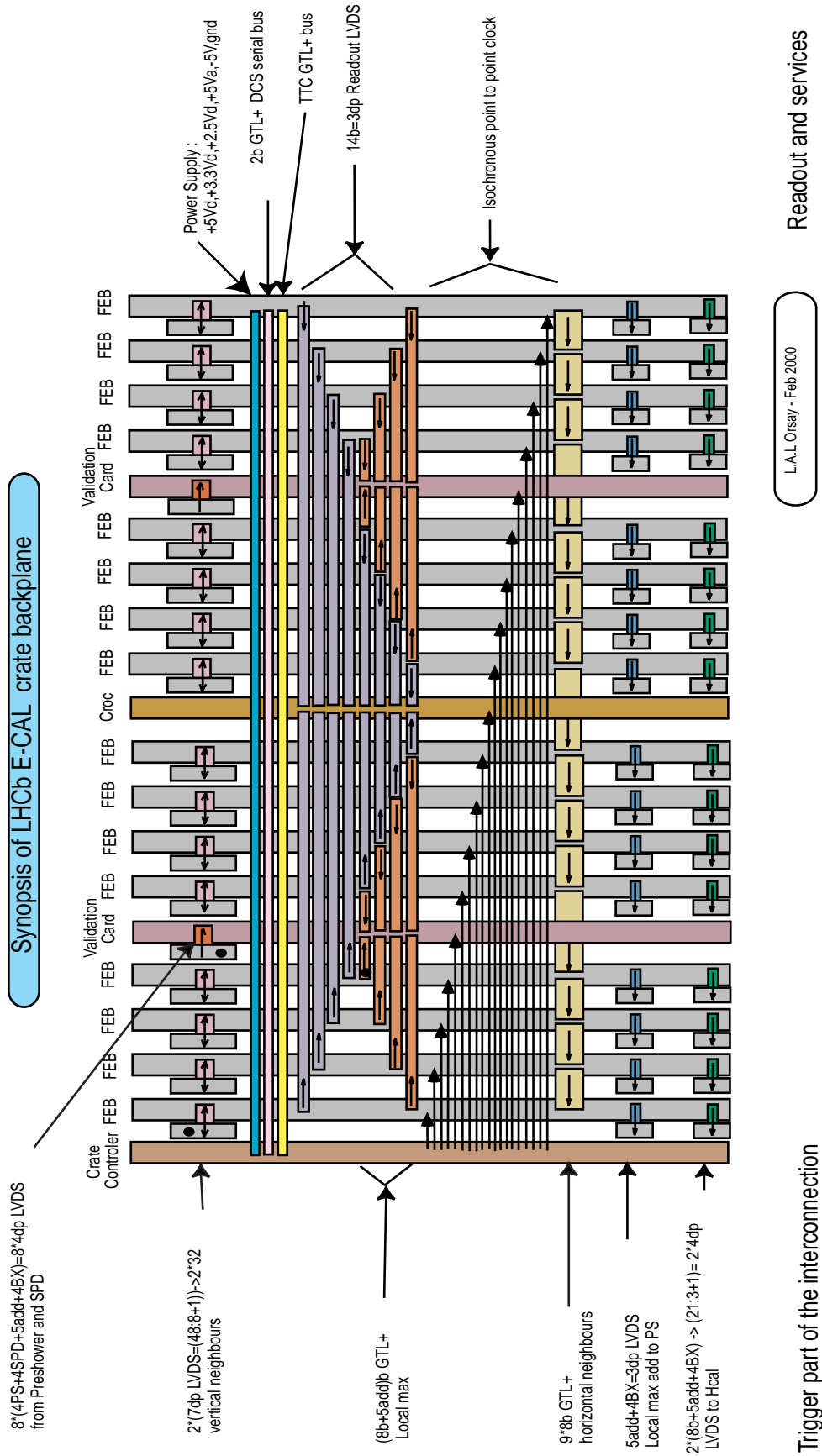
Synopsis of LHCb E-CAL crate backplane

Power Supply :
+5Vd,+3.3Vd,+2.5Vd,+5Va,-5V,gnd

2b GTL+ DCS serial bus

TTC GTL+ bus

14b=3dp Readout LVDS

Isochronous point to point clock

Readout and services

FEB FEB FEB Validation Card FEB FEB FEB FEB FEB FEB Croc FEB FEB FEB FEB Validation Card FEB FEB FEB FEB

Crate Controler FEB

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8*(4PS+4SPD+5add+4BX)=8*4dp LVDS
from Preshower and SPD

2*(7dp LVDS=(48:8+1))->2*32
vertical neighbours

(8b+5add)b GTL+
Local max

9*8b GTL+
horizontal neighbours

5add+4BX=3dp LVDS
Local max add to PS

2*(8b+5add+4BX) -> (21:3+1)= 2*4dp
LVDS to Hcal

Trigger part of the interconnection

Figure 7: Schematic layout of the backplane of the front-end crate

5. Simulation

The main components of the trigger part of the front-end board are the four FPGAs described in Section 3. They have been programmed, according to the logical diagram shown in Figure 4. This program is listed in [8]. An example output of the simulation is shown in Figure 8. The last but two lines, labelled "test.greatsum_of_all" and "test.greatest_delayed" show the simulated and computed results respectively. Note that the inputs of the simulation are random numbers, which don't try to mimic realistic calorimeter data. This explains why the output is frequently in saturation at 255.
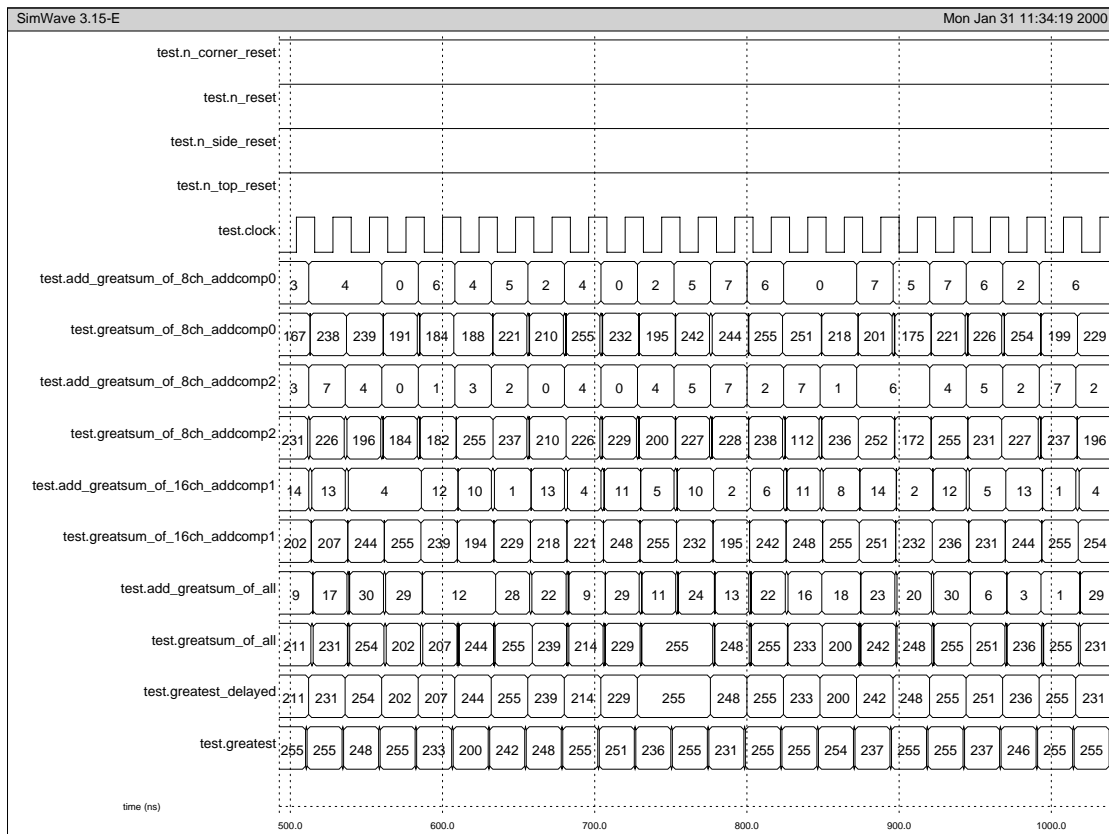

Figure 8: Example output of the FPGA simulation

6. Prototypes and future work

The issues that need testing and prototyping can be grouped as

- Internal behaviour: Test of the FPGA

- LVDS links and proper access to the neighbour's information

- Backplane connections

We intend to implement a test card, to study these various aspects. The synopsis of this card is shown in Figure 9 and includes several blocks:

- LVDS and GTL links (top right) to test the communication

- 32 input FIFO and 1 output FIFO (centre) to test the processing of the data by the ALTERA. The previously mentioned links can be used to provide the neighbours, using a second test card.

- Output to the Validation Card, to test the backplane and the Validation Card itself. Signal injection can be performed via the 32 inputs, or using the FIFO used previously for the output, so that only one

value has to be programmed per test card. In order to test the Validation Card, 8 test cards are needed, but they will not all be equipped with the 32 FIFO and the 4 ALTERA, only the single output FIFO will be needed to drive the Validation Card.
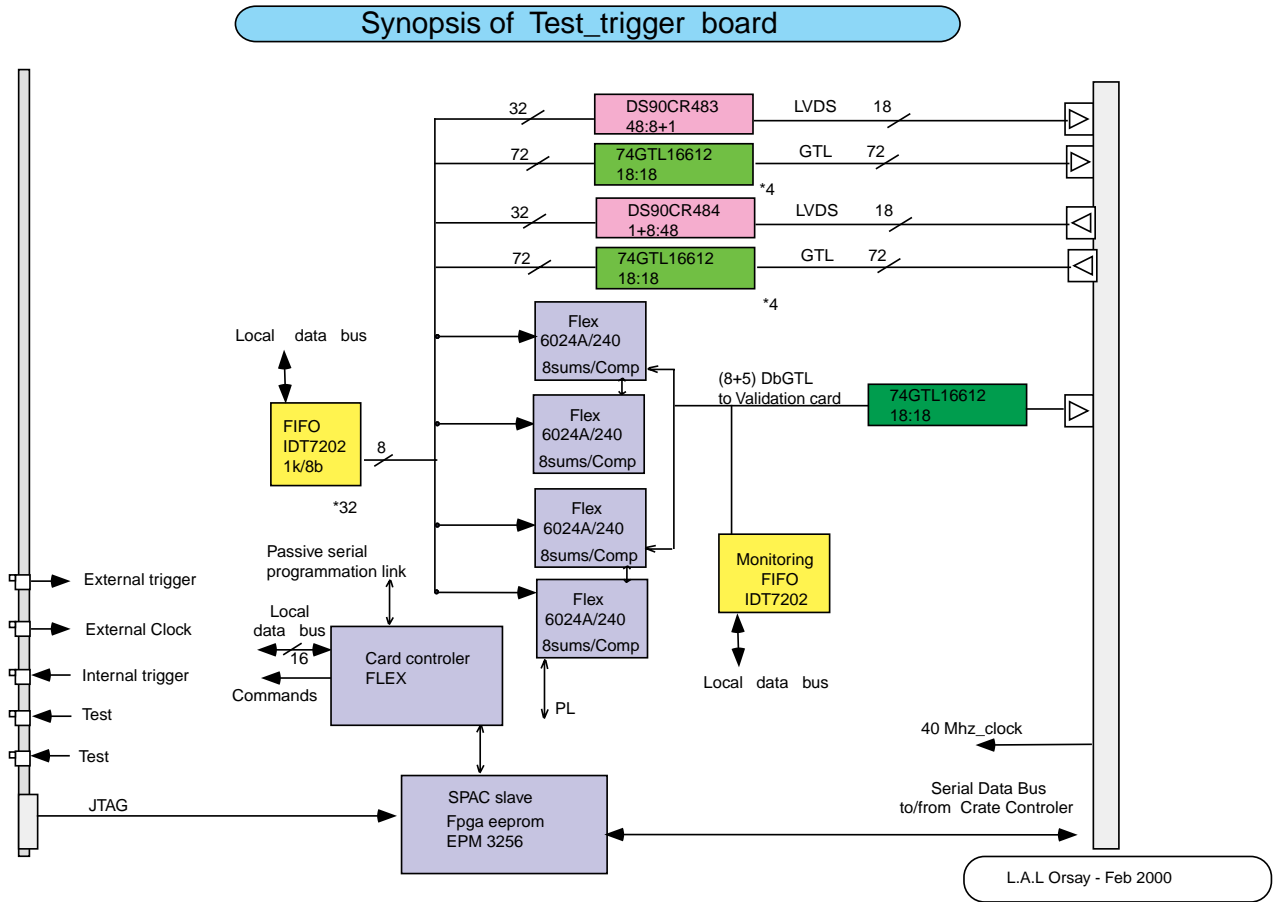

Figure 9: Synopsis of the test trigger card

This test card complements the prototype of the front-end board built and successfully tested on a test beam in 1999, as described in [7]. The latter contains the analog shaping, the ADC, pedestal correction, LUT and readout pipeline for 16 channels on a 6U VME board. These components are now validated. Building a test card with only the trigger part allows a proper testing of this last part of the front-end board for smaller cost than with a full prototype front-end board. This card will also be used to test the backplane, and as input to test the Validation Cards.

7. CONCLUSION

The front-end part of the calorimeter trigger is already defined with enough precision. We can start the prototype step and confirm with real hardware the simulation. We know how to extract the highest E_T candidate on every front-end board in less than 12 clock cycles.

REFERENCES

[1] *The LHCb Collaboration*, "Technical Proposal",
CERN/LHCC 98-4, 20 February 1998

[2] *S.Conetti and D.Crosetto,* "The LHCb Calorimeter Trigger and its implementation with the 3D-Flow system",
LHCb 98-013, 31 January 1998

[3] *The LAL LHCb group*, "An Alternative High PT Electron and Hadron Trigger for LHCb",
LHCb 98-058, 4 September 1998

[4] *C. Beigbeder at al.*, "An Update of the 2x2 Implementation of the Level 0 calorimeter Triggers",
LHCb 99-007, 29 April 1999

[5] *A.Bertin et al*, "Proposal for a Level 0 calorimeter trigger system for LHCb",
LHCb 99-013, 29 May 1999

[6] *C. Beigbeder et al.,* "A Joint Proposal for the Level 0 Calorimetric Triggers",
LHCb 99-017, 7 June 1999

[7] *C. Beigbeder et al.,* "The front-end electronics for LHCb calorimeters"
LHCb 99-053, 31 December 1999

[8] See the Web page http://lhcb.cern.ch/trigger/level0/html/altera.htm