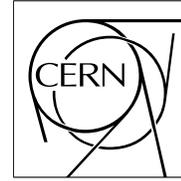**The Compact Muon Solenoid Experiment**

CMS Note

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February 7, 2003

Tests of Silicon Detector Modules
for the Tracker End Cap with the ARC System

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Abstract

During the production phase of the CMS silicon strip detector modules the ARC (APV Readout Controller) system will be used as a readout system for testing purposes. The first ten TEC (tracker end cap) modules built have been tested using the ARC system. After a description of the test environment and the test procedures the results for the so-called expressline modules are summarized.

1 Introduction

The CMS Silicon Strip Tracker (**SST**) will instrument the central region of the CMS experiment [1]. It will be composed of four parts: the Tracker Inner Barrel (**TIB**), the Tracker Outer Barrel (**TOB**) and two Tracker End Caps (**TEC**). About 16000 silicon micro strip detector modules are foreseen to equip the SST, the largest all-silicon tracker in the world. One individual silicon detector **module** consists essentially of three elements: a set of silicon sensors, a mechanical support structure and the frontend electronics (**FE Hybrid**). An example of a TEC silicon detector module is presented in figure 1.
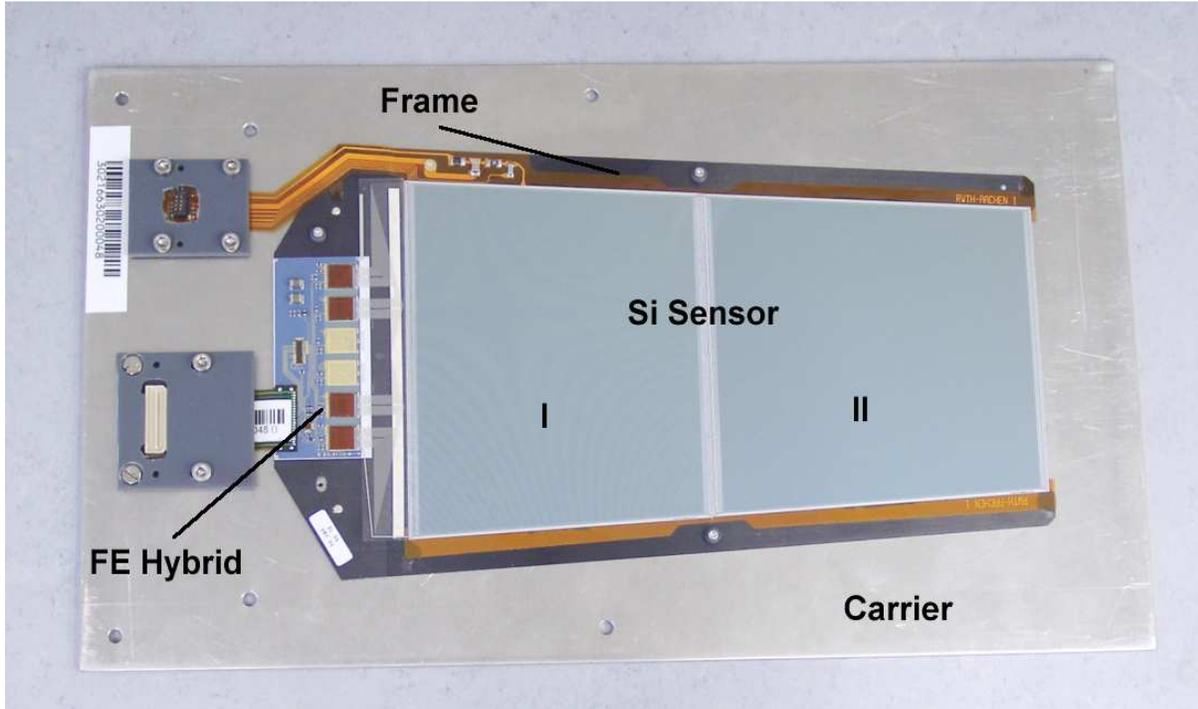

Figure 1: Photograph of one TEC module mounted on an aluminium carrier plate used for transportation. The 512 channels are counted from top to bottom.

The construction of the SST involves a large number of industrial companies and research institutes from many different countries. The large-scale production phase of the detector modules needs an appropriate testing scheme during the assembly period of more than two years.

It is essential to assure a simple and reproducible assembly and testing procedure among different testing centres. Therefore throughout the whole production a lot of different quality assurance tests have to be performed to avoid expensive production failures.

The **A**PV **R**eadout **C**ontroller system (see [2] for detailed information) is a CMS test setup intended for hybrid and module quality assurance. In total 30 ARC systems are already distributed to the SST test centres. ARC is foreseen to be used in the following production centres: hybrid manufacturers [1], APV bonding centres, gantry centres and module bonding centres.

The CMS tracker community started a preproduction of several modules for TIB, TOB and TEC utilisation. The results presented in this paper are taken from measurements done with ten TEC modules tested in Aachen with the ARC system. The preseries of ten TEC modules, the so-called **expressline modules**, is an important step at the beginning of the mass production phase: The operation of the ARC systems on site of the testing centres can be established and the centres gain experience in producing and testing silicon detector modules. [2]

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[1] In industry the ARC board will be used in the so-called **F**rontend **H**ybrid **I**ndustrial **T**ester, a simple to use setup developed by UCL Institut de physique nuclèaire in Louvain-la-Neuve [3] in collaboration with III. Physikalisches Institut B RWTH Aachen.

[2] Three of these TEC modules were taken to the PSI testbeam experiment in May 2002, while others will equip a subset (ring 6 location) of the TEC that will be used for the so-called **system test**.

From the production point of view it is important to recognize typical problems that occur during the module assembly phase (bad bondings, influence of transportation etc.). Thus special attention is paid to optimize the testing procedure, i.e. avoid tests leading to unnecessary redundant information. This includes a comparison of LED and laser measurements.

2 Test Environment

The ten TEC modules are produced in the so-called ring 6 design, i.e. these modules will equip ring 6 of the tracker end cap petals. Figure 2 shows the preseries of the ten TEC modules.
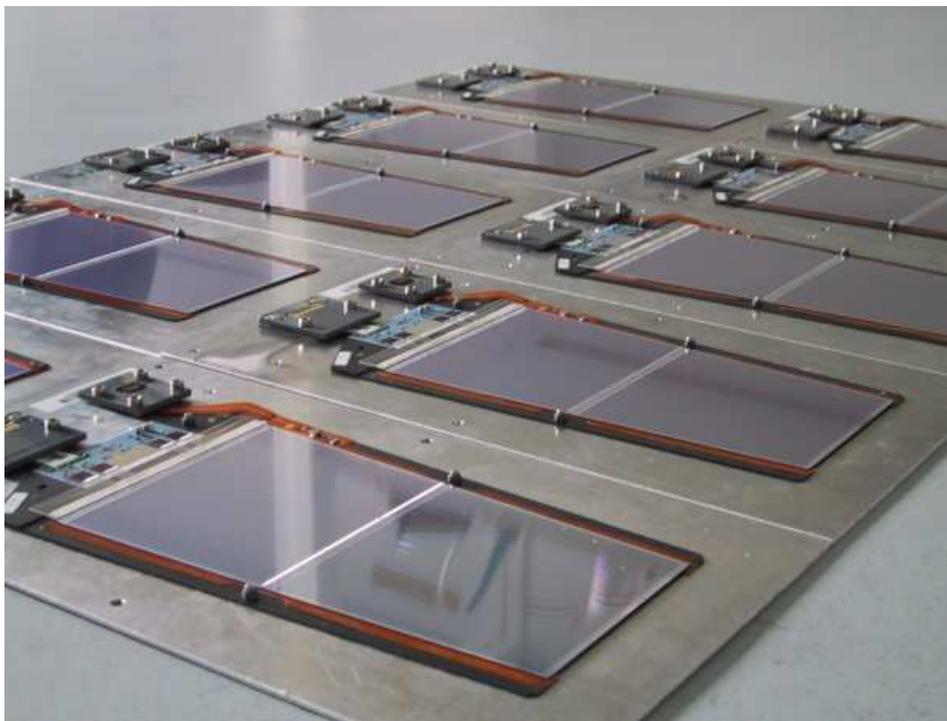

Figure 2: Photograph of TEC module preseries.

The test setup used for quality assurance consists of the standard ARC hardware (ARC board and ARC frontend adapter) extended by the LED Controller **LEP 16** allowing light tests on the depleted module (see [4]). Figure 3 gives an overview of the test environment. During the quality check the modules are located in a box (see figure 4) protecting all bondings and the electronics from external influences. In addition the box serves as LED test station and can be used outside and inside the cooling box. Detailed pictures of the LED array used are given in figures 5 and 6.

All modules are tested at ambient temperature in an airconditioned environment in the institute's clean room using **ARC S**oftware version 5.0. The APV register settings are used as described in [6], if not mentioned explicitly.

2.1 Test Procedures

The ARCS version 5.0 test procedures are divided into two different types: **fast tests** and **deep tests**. The automated fast tests are recommended at the beginning of each module test as the hybrid functionality needs to be verified (including I^2C communication and APV25, DCU2, PLL and MUX chip response). The same scenario is used during the industrial hybrid production. As the ARC board is used in the FHIT setup the ARCS C++ routines allow for communication between the laboratory PC and the ARC hardware [3]. Due to the limited manufacturing time and the large number of modules to be produced, automation and time optimized testing procedures are mandatory. The fast tests take approximately one minute.

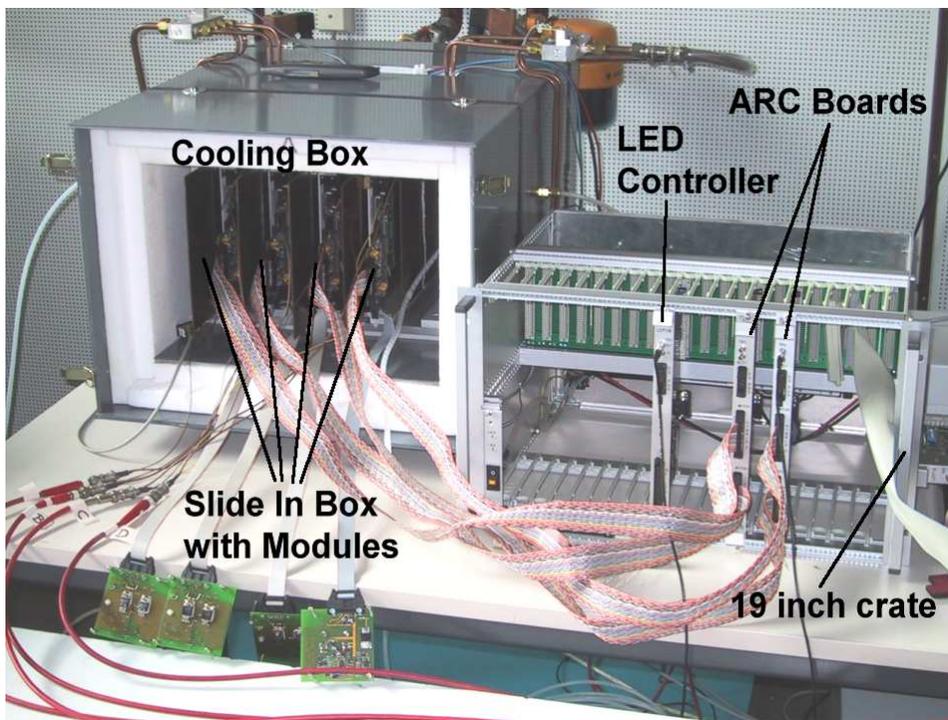[3] These tests are called **functional test** in the FHIT procedures.

Figure 3: A 19 inch crate equipped with two ARC boards (**multi board setup**, see [2]) and a LED controller. The high voltage for module depletion is supplied by a CAEN Sy 126 module. A prototype of a special HV module fitting into the ARC environment is already produced in Aachen and will be used for further module tests in the future (see [5]). The ARC boards are connected to four modules located in the cooling box.
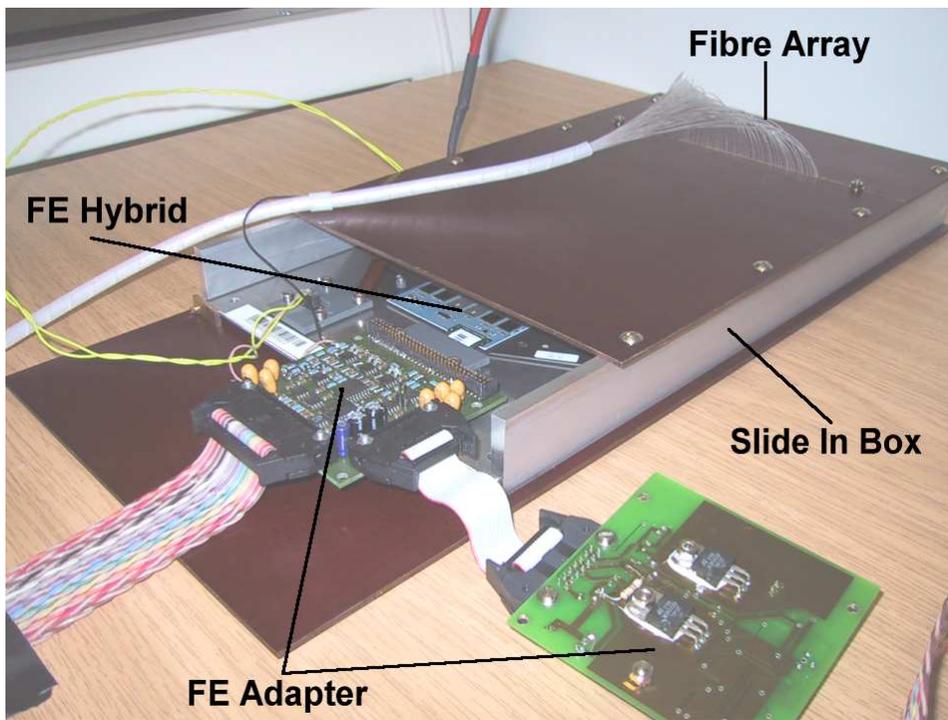

Figure 4: Module test box (**slide in box**). The module mounted on the carrier is slided into the box and connected to the ARC FE adapter. The top plate is used to hold the optical fibre array above the second silicon wafer in a few millimetres distance to the surface.
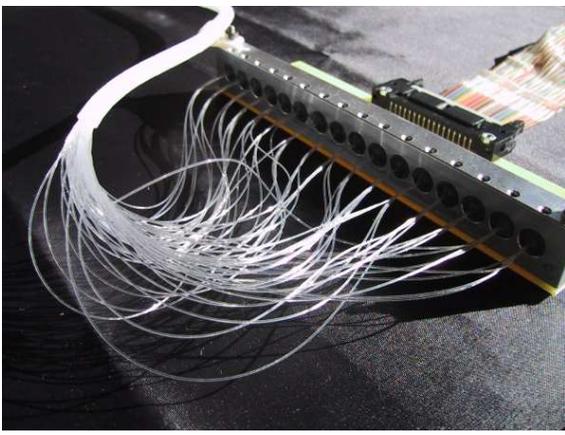
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Figure 5: LED array (λ=950 nm, infrared). The LED pulser LEP 16 (see figure 3, LED controller) is able to operate 16 LEDs. Each LED is coupled to four optical fibres to minimize the light spot on the silicon wafer leading to an optical fibre array of 64 light spots with a pitch of 1.75 mm.

Figure 6: Mechanical structure of the fibre array that is mounted on the test box. The size of one LED spot is equivalent to approximately 30 detector strips when the array is fixed 3 mm above a silicon wafer.

The deep tests include the following measurements:

- **basic** tests
  - pedestal and noise distributions
  - calibration pulse shape measurements
- **advanced** tests
  - APV pipeline check
  - pulsed LED measurements
  - laser tests

Except for the laser measurements all tests mentioned are performed at ambient temperature at a bias voltage of 150 V.

3 Results

For identification purposes during mass production each module is labeled with a module specific bar code. A bar code reader (see [7]) allows to write the identification into ARCS. The batch of ten TEC modules is characterized by the number **302166302000XX** with XX representing the individual module number. In the following module 30216630200012 is simply called "module 12".

3.1 DCU Test

Each fast test checks the response of the hybrid and its I^2C devices, e.g. APV25, DCU (see [8]). No communication problems were observed on the expressline modules. Figure 7 shows one important test in the fast test procedure: The nominal voltages on the hybrid (1.25 V and 2.5 V) can be changed slightly by the ARC FE adapter in the range of +4% and -15% (for details see [2]). Since the DCU is a pure monitoring chip –including the monitoring of the low voltages on the hybrid– a useful response check is the monitoring of the DCU output while changing the external low voltage supply.
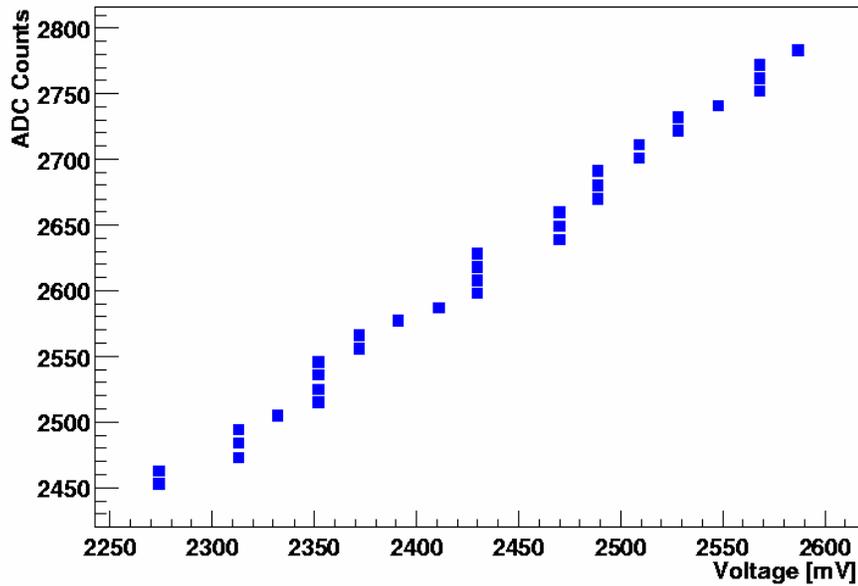
Figure 7: The external changing of the 2.5 V low voltage line which is supplied to the hybrid causes a linear response of the DCU chip. This can be used as a simple calibration of the chip.

3.2 IV Curves

All IV curves (leakage current as a function of the supplied high voltage) are measured using a commercial CAEN HV Power Supply Sy 126 at ambient temperature independent from the ARC system. The high voltage is ramped up from 0V to the breakdown voltage with 10V/sec between the points of measurement. Figure 8 shows the results. [4]
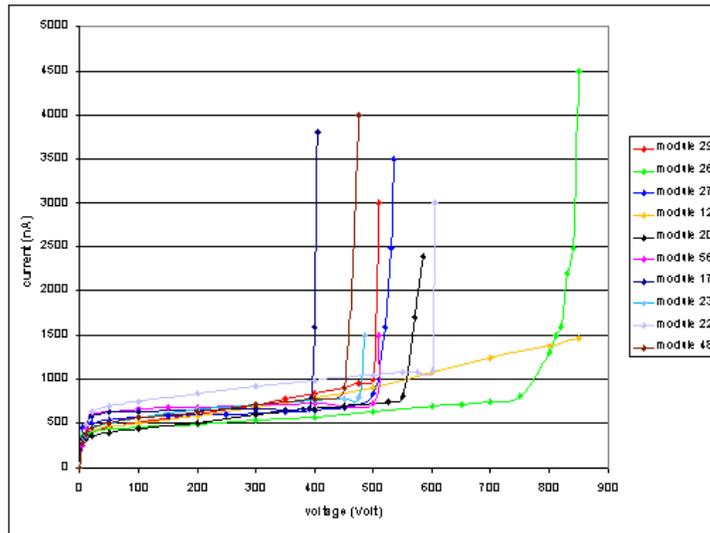

Figure 8: IV curves of the ten modules.

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[4] Note that the modules were not flushed with dry air or nitrogen and that humidity and temperature were not monitored.

3.3 Pedestal and Noise

3.3.1 Pedestal

A typical pedestal distribution of a TEC module can be seen in figure 9. The pedestals vary in a range of approximately 15 ADC counts for each APV25 chip. Since the pedestal distributions at hybrid level show large differences between the 4 chips each APV chip needs to be tuned by the APV register *VPSP* (see [10]) that allow to shift the analog data baseline.
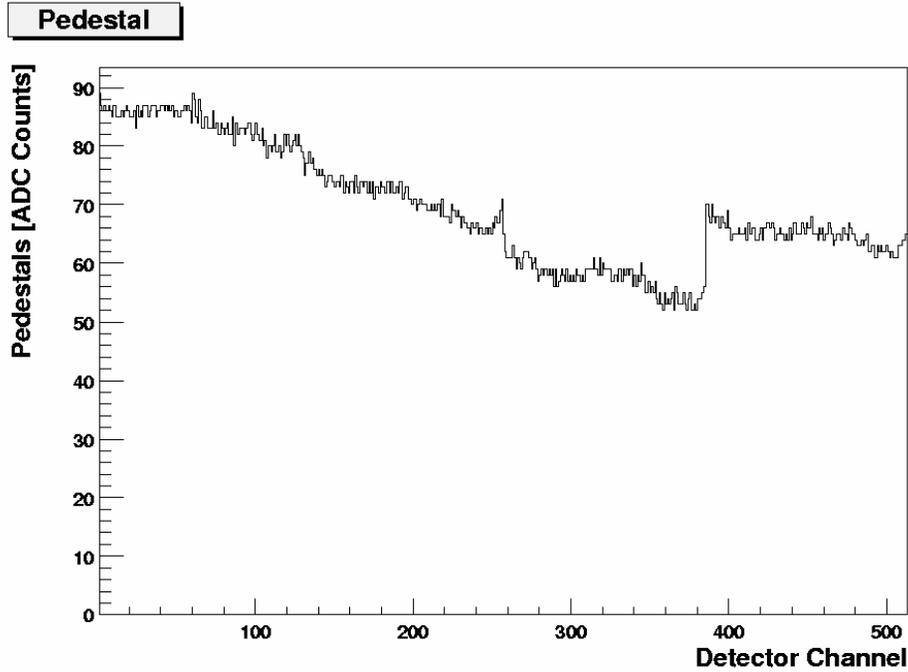

Figure 9: Pedestal distribution for all 512 channels of module 12. Four blocks of 128 channels per APV chip can be seen.

3.3.2 Noise

Two different noise calculations are considered in the data analysis tools of ARCS: **raw noise** and **common mode subtracted noise**. The common mode subtracted noise is taken as the basis to determine the list of channels showing conspicuous behavior. A short description of the flagging strategy of such **bad channels** is given here.

Pedestal and noise distributions are produced using N events. σ_{rms} is calculated by

$$\sigma_{rms} = \sqrt{\frac{\sum_i (rms_i - \overline{rms})^2}{N}}$$

with $\overline{rms}$ being the median of the rms distribution of all channels and rms_i being the rms value of channel i. A channel is masked as a **bad channel** if one of the following criteria is true:

- $n \cdot \sigma_{rms} < |rms_i - \overline{rms}|$ with n set to 5.

- $rms_i > rms_{max}$ with rms_{max} set to 3.5.

- $rms_i < rms_{min}$ with rms_{min} set to 1.

- $P_{skip} \cdot N < N_{noisy,i}$ with P_{skip} set to 0.3 and $N_{noisy,i}$ the number of events flagged by one of the following two criteria that are checked event by event:

$$|s_i| > T_{skip} \cdot rms_i \qquad \text{or} \qquad |s_i| > \frac{\sum_i |s_i| \cdot T_{skip}}{128}$$

with s_i being the common mode corrected data of channel i and T_{skip} set to 3.

For a more detailed description of the pedestal, noise and common mode calculation see [11]. In figure 10 both raw noise and common mode subtracted noise distributions are overlaid in one plot to give an impression of their differences. All found bad channels are marked by lines in the bottom part of the figure. The uppermost distribution describes the raw noise of all 512 channels of module 12 running in peak mode. A slope in the noise across each APV can be observed. This slope vanishes with a common mode correction to the raw noise data. The effect of the common mode correction is shown in the lower noise distribution: The height of the noise is reduced to 1.5 ADC counts in average. This value corresponds to 1200 electrons which is a reasonable value while running in peak mode (the noise in deconvolution mode is a factor of $\sqrt{2}$ higher, see [9]). The common mode subtracted noise distribution is flat except for the APV edges (channels 1/128, 129/256, 257/384, 385/512). The reason for this effect is still under investigation[5].

The randomly triggered **pipeline** of the APV chips (see [10]) using pedestal and noise information showed no obvious problem for the expressline modules.

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[5] These channels are not flagged as bad in other tests and therefore not included in the result summary table 1 later.
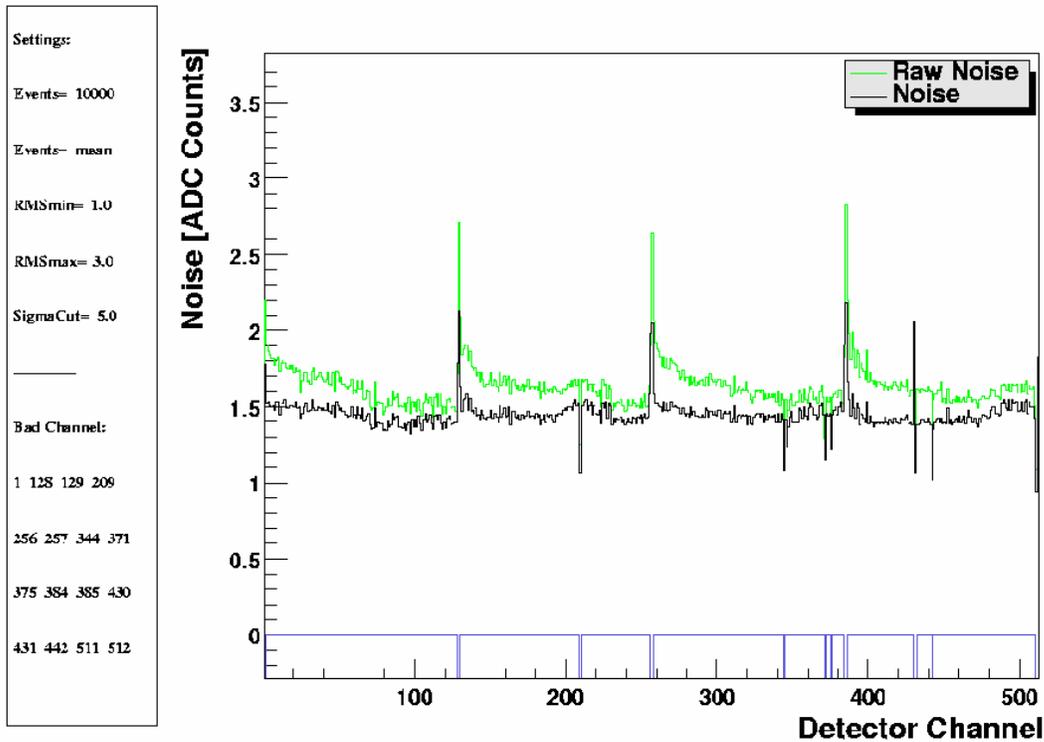

Figure 10: Two different noise distributions (raw noise and common mode subtracted noise). The bottom part shows all strips flagged as **bad channels** by ARCS 5.0.

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3.4 Calibration Pulse Shapes

The APV chip provides the generation of internal calibration pulses with a defined charge or a defined pulse height (APV register *ICAL*=29 corresponds to 25000 electrons). This information can be used to calibrate the test setup and to tag bad strips (missing or open bondings, shorts, dead channels) very efficiently. Figures 11 and 13 show three different types of pulse shapes measured with a time resolution of 3.125 ns: high, normal and low pulses. The maxima distribution of all strips allows to tag bad channels.
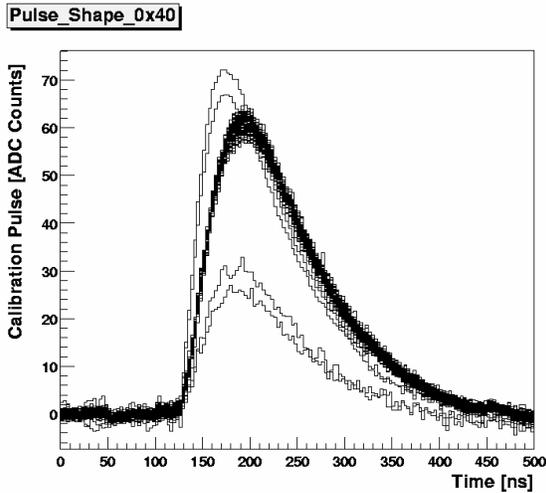

Figure 11: All 128 calibration pulse shapes of module 12 shown for one APV in **peak mode** with inverter off.
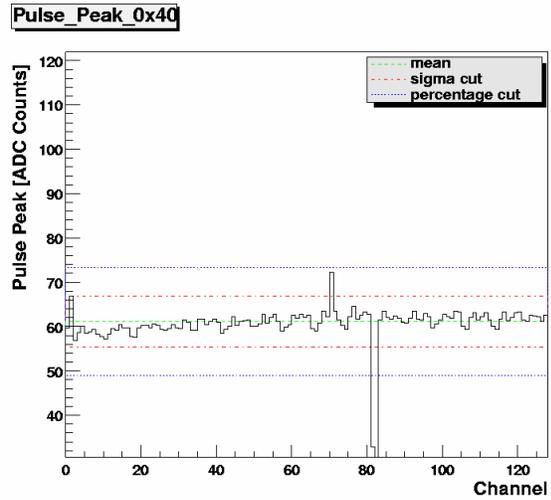
Figure 12: Distribution of the pulse maxima extracted from figure 11. Heights of about 60 ADC counts correspond to 50000 electrons leading to 1 ADC count per 800 electrons in peak mode. Strips exceeding the given thresholds are flagged as bad channels.
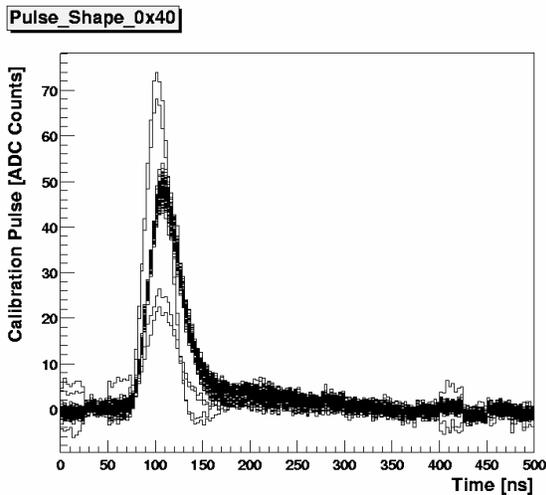

Figure 13: All 128 calibration pulse shapes of module 12 shown for one APV in **deconvolution mode** with inverter off.
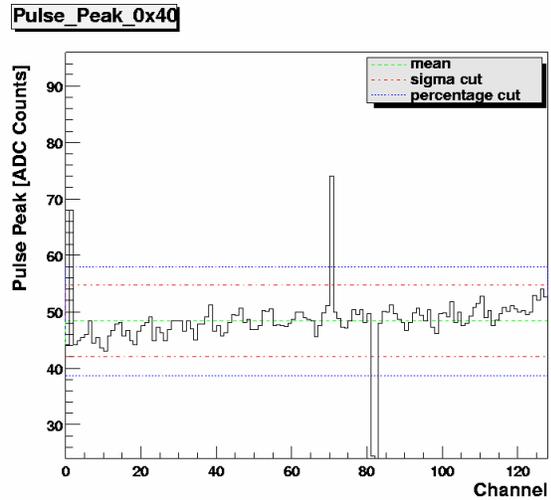
Figure 14: Distribution of the pulse maxima extracted from figure 13. Bad channels are more pronounced in deconvolution mode compared to peak mode.

Two examples of different cuts are shown in figures 12 and 14: A percentage cut (20%, dotted line) and a 3 σ cut (dashed-dotted line) with respect to the mean value (dashed line). Open or missing bondings are characterized by high pulse shapes. Low pulse shapes always occur in pairs of neighbouring strips and are explained by shorts between the two corresponding strips.

3.5   LED and Laser Measurements

Special attention is paid to the comparison of LED and laser measurements[6]. The tools used for light tests with infrared LEDs are described in section 2. ARCS 5.0 provide an automated light scan across the silicon wafer. The induced signal is used to determine bad channels. The cuts applied to the distribution are described in section 3.4. Figure 15 shows the response of one APV to a LED pulse. The intensity profile of the incoming light is reflected by the measured wave structure with an amplitude of approximately ± 7 ADC counts. Channel 35 of the displayed APV data is flagged as bad channel.

A comparison between LED and laser tests is given in figures 16 and 17 where in both cases the same strips are flagged as bad channels. Compared to LED tests laser measurements provide the possibility of studying single strips due to the focussed light spot. LED tests have the advantage of inducing a large current across the whole module giving results on pinholes (see [12]) instantaneously. In the mass production phase LED tests are easier and faster to perform.
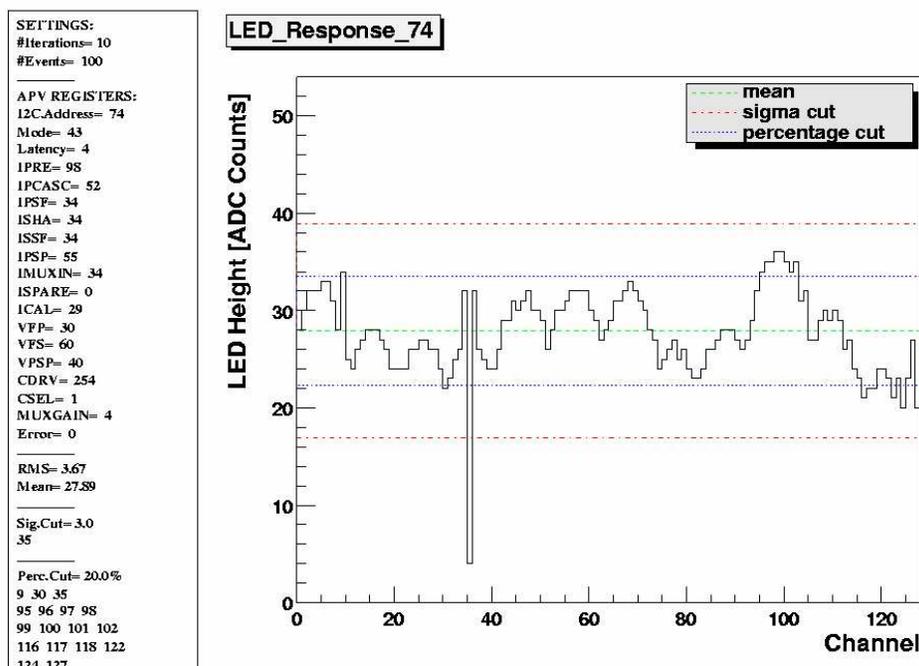

Figure 15: Response of module 27 to LED light. To show the intensity distribution of the LED light only one APV is shown.

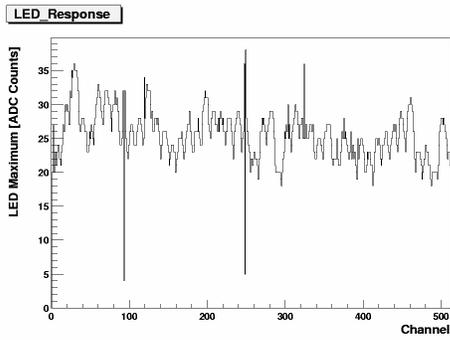[6] The laser tests were done by J. Olzem (I. Physikalisches Institut B, RTWH Aachen).

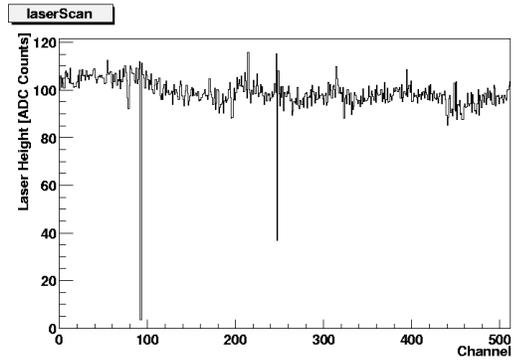Figure 16: Channel response of module 27 to the LED source.

Figure 17: Channel response of module 27 to the laser source.

4 Summary and Conclusions

Table 1 gives an overview of the test results at ambient temperature for all ten TEC modules.

In total 16 strips were identified as bad channels using tests provided by the ARC system. All modules passed the qualification criteria defined in [6] not taking into account the APV edge effect described in section 3.3.2.

The shorts observed between channels 92/93 and 442/443 on module 17 cannot be detected using the LED test, since the whole area around the shorted strips is illuminated. Here the laser test gives consistent results with the RMS noise and calibration pulse measurements.

The fact of not detecting the pinhole (channel 209 on module 12) with laser tests can be explained by the environmental conditions (different high voltage settings leading to different leakage currents, humidity) being different for the LED and laser test stations.

The test results of the first ten TEC ring 6 modules show that the developed ARC system is adequate for testing hybrids and single modules during the CMS module mass production phase.

Defect Location		Defects found in different tests						
Module	Strip	RMS Noise	Break-down	Pulse-Shape	LED	Laser	Visual Inspection	Comments
12	511	×	> 850 V	×	×	×	missing bond	
	442	×		×	×	×	open bond	
	431	×		×	×	×	○	
	430	×		×	×	×	○	
	209	×		○	×	○	○	pinhole
17	443	×	≈ 400 V	×	○	×	○	short
	442	×		×	○	×	○	
	93	×		×	○	×	○	short
	92	×		×	○	×	○	
20			≈ 560 V				no visible errors	
22	318	×	≈ 610 V	×	×	×	missing bond	unbonded pinhole
23			≈ 480 V				no visible errors	
26	480	×	≈ 800 V	×	×	×	missing bond	missing bond
27	248	×	≈ 530 V	×	×	×	missing bond	pinhole
	93	×		×	×	×	○	pinhole
29	189	×	≈ 500 V	×	×	×	open bond	
	7	×		×	×	×	○	
48	9	×	≈ 450 V	×	×	×	missing bond	unbonded pinhole
56			≈ 500 V				no visible errors	

Legend:

×   defect found during the test

○   defect not found during the test

Table 1: Summary table of the test results.

References

[1] CMS Collaboration *"Addendum to the CMS Tracker TDR by the CMS Collaboration"*, CERN/LHCC 2000-016.

[2] M.Axer et al. *"A Test Setup for Quality Assurance of Frontend Hybrids"*, CMS Note 2001/046, Oktober 15, 2001.

[3] X.Rouby et al. *"FHIT - Quick reference guide"*, May 28th, 2002.

[4] LEP 16
http://www.physik.rwth-aachen.de/group/IIIphys/CMS/tracker/en/silicon/ledpulser.html.

[5] High Voltage Board DEPP
http://www.physik.rwth-aachen.de/group/IIIphys/CMS/tracker/en/silicon/hvboard.html.

[6] L.Demaria et al. *"Procedures for Module Test"*, Draft2, March 4th, 2002.

[7] EIA Force *"User Manual"*, V 2.1, S/N 824965.

[8] Magazzu et al. *"DCU2 User Guide"*, Version 2.12, October 10th 2001.

[9] M.Friedl *"The CMS Silicon Strip Tracker and its Electronic Readout"*, Institute of High Energy Physics, Austrian Academy of Sciences, May 2001.

[10] J.Jones, *"APV25-S1 User Guide"*, Version 2.2, September 2th, 2001.

[11] M.Axer et al. *"ARCS APV Readout Controller Software, A graphical User Intreface for Hybrid and Module Testing"*, Version 5.0, July 2002.

[12] I.Tomalin *"Problems due to HIPs & Pinholes"*,
http://cmsdoc.cern.ch/Tracker/managment/Agenda_GTM/Gm_02_01/Ian_HIPS.pdf, 25th January 2002.