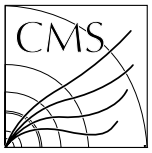

The Compact Muon Solenoid Experiment

CMS Note

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Pion Induced Single Event Upset in the CMS Pixel Detector Readout

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Abstract

Single event upset probabilities for 200 MeV pions are compared for SRAM devices implemented in two different radiation hard SOI technologies.

1 Introduction

Single Event Upset (SEU) is a phenomenon induced by radiation in electronic chips and has first been mentioned by J.T.Wallman and S.M.Marcus in 1962 [1]. Single event upsets are caused by heavily ionizing fragments and recoils, which are produced in a chip by hadronic interactions and which deposit enough charge in a sensitive node of an electronic circuit to induce for example the state of a memory cell to flip. This has always been a major concern for space borne missions with exposure to cosmic radiation over long time periods. With the advent of the new Large Hadron Collider (LHC) at CERN with greatly increased radiation levels as compared to present accelerators, it could also become an issue for particle physics experiments. In particular the front end electronic chips of the vertex detectors, close to the interaction regions, sit in a very hostile radiation environment, which, through SEU, could cause problems ranging from the intermittent loss of some channels to the temporary breakdown of detector control. Depending on the anticipated frequency of SEU, appropriate reset mechanisms must be foreseen already in the design of the readout electronics.

The charge released by ionisation, or part of it, can very efficiently be collected by drift in the high electric field at the drain of a transistor in its OFF state, and the resulting transient current might generate a SEU. Charge can also reach sensitive nodes by diffusion, although at a reduced level due to recombination and over an extended period of time. The amount of charge collected is governed by the volume from which it has the possibility to reach the node. This sensitive volume depends on the particular chip process. Chips manufactured in a bulk process have potentially a larger sensitive volume than SOI chips. Differing transistor implementations in the various technologies imply different sensitive volumes. Therefore SEU probabilities may strongly vary in the technologies considered for the frontend electronics.

At LHC single event upsets will occur mainly from pions, protons and neutrons which produce specific spectra of heavily ionizing nuclear fragments. Such particles and their energy loss have been simulated by Huhtinen and Faccio [2]. Given a characteristic shape and size of the sensitive volume V_s, and a critical value of deposited ionisation energy in V_s which must be exceeded to trigger a SEU, it is in principle possible to estimate SEU probabilities for a particular chip technology. Sensitive volume and critical energy must be obtained from dedicated heavy-ion irradiation of the circuits.

A more straightforward way to obtain SEU probabilities at LHC is to directly expose typical electronic cells, realized in the technology foreseen for the frontend chips, to a beam simulating closely the anticipated LHC environment. In the CMS experiment at LHC the readout chips of the pixel detectors will be exposed to hadron flux densities of $5 \times 10^7 cm^{-2}s^{-1}$ at a radius r=4.3 cm and five times less at r=12 cm for peak luminosity [3]. This flux consists mainly of charged pions. Due to the possibility of pion absorption, which amounts to about one third of the total cross section and where the pion rest mass is converted into kinetic energy of heavily ionizing fragments, SEU effects may be particularly strong for pions [4]. We therefore have exposed simple SRAM structures, realized in both radiation hard silicon-on-insulator DMILL (Temic) and Honeywell RIC-MOS IV technologies (minimal feature $0.8\mu m$ for both processes), to a high intensity pion beam at PSI.

In section 2 the SEU measurements are described and SEU probabilities are presented. Consequences and conclusions for the chip design are drawn in section 3.

2 Measurements and results

Shift register cells located on precursor CMS pixel readout chips [3] in DMILL and Honeywell technology were exposed to a beam of $2\times10^9\pi^+cm^{-2}s^{-1}$, in order to get a relative comparison of SEU probabilities in the two considered processes. The energy of the beam was 200 MeV, where the total hadronic cross section has a maximum due to the 3-3 resonance. At small rapidities, the pion spectrum predicted for the LHC peaks in the range of a few hundreds MeV ([3]

appendix A). A monoenergetic beam of 200 MeV as used in this experiment will simulate LHC conditions rather closely, however overestimating SEU by about 30% (all pions in this experiment have maximal cross sections). Since Si is a symmetric nucleus, no difference is expected between π^+ and π^- [4]. The pion fluence was determined by activation of Al foils: $^{27}Al(\pi^+, xN)^{24}Na$ (for the cross section of this reaction see [5]), and measuring the resulting γ (1369 keV) decay activity of ^{24}Na (half live 15 h).

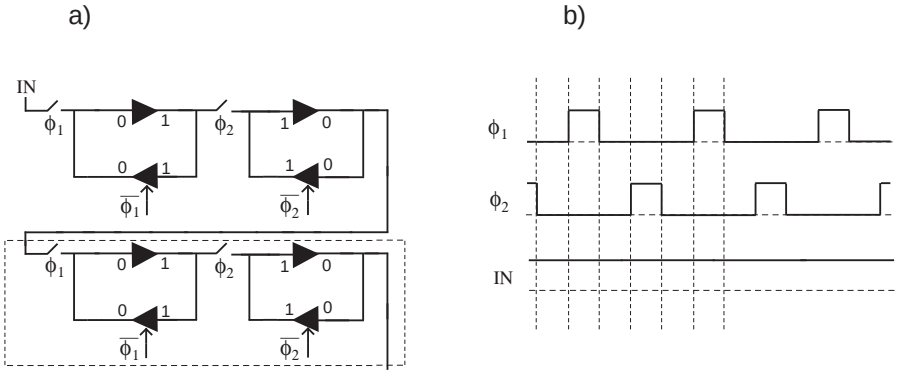

Figure 1: a) Two cells of the shift registers. The switch in the feed back loop is integrated in the inverter structure. b) The most simple signal pattern sent to the chips with equal lengths of the 4 phases.

	n W/L	p W/L
DMILL	2.2/2.4	3.6/3.3
Honeywell	1.8/2.0	3.6/2.0

Table 1: Transistor drain sizes used for the inverters in μm.

The 4-phase shift register cells consist of two SRAMs as shown in Fig.1. The transistor sizes used in the inverters are given in Table 1. The switches connecting the SRAMs are realized as transmission gates, while in the feed back loop a switched inverter structure is used. The design of the circuit is such that both inverters of the SRAMs are equally sensitive to SEU. Charge deposited in those parts of the transmission gates where the logic level agrees with the substrate voltage do not contribute to SEU.

SEU in the cells could be observed by continuously feeding the first cell of the shift register with a constant logic 1 level, clocking it through the register and monitoring any level change at the output of the register simply with a scaler. The shift registers on the precursor pixel readout chip have a length of 104 cells (208 SRAMs), and serve for downloading calibration and threshold data into the pixel unit cells. Since the cells are connected to the pixel chip circuitry representing different capacitive loads at the various nodes of the register, a SEU could be either persistent and be registered in the scaler, or the upset cell could be immediately forced back to the previous state by the circuit and lost, depending in which clock phase the SEU occured. Therefore it was necessary to measure SEU probabilities for the four clock phases individually. This was done either by continuous runs with different respective lengths of the four periods shown in Fig. 1, or by keeping the shift register in a fixed phase for a given time and then flush the data out. The data pattern from the various clock phases could be correctly interpreted taking into account the particular circuit of the shift register with its external loads, and true SEU rates per register could be deduced.

Two DMILL chips and two Honeywell chips were put into the beam. The responses of the chips manufactured in the same technology were compatible. The chips were irradiated both from the front and from the backside, giving identical results.

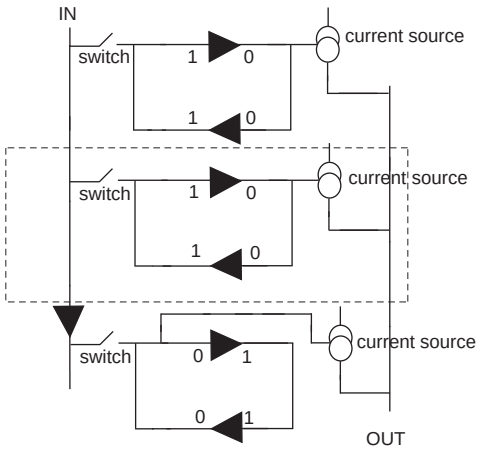

Figure 2: the basic structure of the stand-alone test

In order to check the complicated interpretation of the SEU rates in the different clock phases, arrays of stand-alone isolated SRAMs in DMILL technology were also investigated for SEU. Sixteen SRAMs were connected to identical current sources with the outputs of the current sources being connected to one common out (see Fig.2). Before turning on the beam half of the SRAMs were forced into logic state 1 and the other half into state 0. Then the structures were disconnected from the inputs using the switches shown in Fig.2. When-

ever a SEU occured in one of the SRAMs, a change of the current registered at the common out would be detected. The rates obtained for these isolated structures, recorded with supply voltages of 2.5, 4.0 and 5.0 V, are compatible with the true SEU rates deduced from the DMILL shift register data. Table 2 shows the results for the shift registers in both technologies.

Supply voltage	2.5 V	4.0 V	5.0 V
DMILL	0.8×10^{13}	1.4×10^{13}	2.4×10^{13}
Honeywell	1.7×10^{14}	3.6×10^{14}	6.0×10^{14}

Table 2: Average pion fluence (π/cm^2) between SEUs in DMILL and Honeywell SRAMs for different supply voltages.

3 Conclusions

Given the SEU probabilities, it is not straightforward to predict their consequences on the performance of the CMS pixel readout. The results of SEU are extremely circuit and architecture dependent. A SEU could be persistent and change the logic pattern crucially, or it could occur in a cell where it does not induce any change in the momentary logic pattern. To our knowledge there exists no simulation tool dealing with such effects.

A persistent SEU could influence only single pixels or it could bar control of an entire array of daisy-chained chips leading to the temporary loss of thousands of pixels. Depending on where a SEU occurs it could either be quickly detected from its immediate effect or it could remain unobserved for quite a while and lead to large amounts of corrupt data.

To minimise the risk of SEU, the important register cells should be designed such that the critical charge needed for SEU becomes as large as possible. This can be achieved by several design measures, although at the expense of an increase in power consumption and space. One method is to use maximal supply voltages as can be seen from the data in Table 2. Furthermore, there is the possibility of increasing the transistor dimensions. For example, DMILL structures of four times the minimal size show 10 times less SEU for maximum supply voltages, in spite of them being hit four times more often [6]. However, due to space limitations, increased structures can only be used in the most critical parts of the pixel readout chip. Simple design measures keeping the transmission gate switches of the feedback inverter close to the power rails will considerably reduce their contribution to the SEU rates. Finally SEU immune triplication logic could be considered.

The last resort to cope with SEU effects is to regularly reset the readout electronics, the reset frequency being governed by the expected SEU rates. At LHC the orbit gap of $3\mu m$ every $89\mu m$ could for example be used to reset sequentially parts of the detector, or reload important registers on the chip. Candidates for such actions would be those parts in the peripheral logic, where SEU could lead to catastrophic consequences. Among these are pointers which control data segments and perform data formatting, DAC registers defining chip voltages, local counters defining the event number, and handshake mechanisms that could get blocked due to generation of false token bits. Partial or full reset options must in any case be foreseen in the readout; SEU effects could simply result in their more frequent use than if SEU was negligible.

The pixel trim bits account for about 20% of the transistors in the pixel unit cell, and are used to set the individual thresholds of the pixels. Each pixel has three bits. If a SEU increases the threshold of a pixel, that pixel will become less efficient with little consequences. If the threshold is decreased, however, the pixel gets noisy and will clog an entire pixel column of 126 pixels. The innermost pixel barrel layer has 19×10^6 trim bits and is exposed to a flux density of $5 \times 10^7 cm^{-2} s^{-1}$. In the present design the trim bits are supplied with 2.5 V and designed with minimal size transistors. For the DMILL technology, we expect 120 pixels to get upset per sec, or 1% of the pixels in that layer after 10 minutes. Thus a scheme must be implemented that continuously monitors noisy or dead pixels and, where necessary, downloads the correct trim bit pattern. Such a procedure is in any case required for the setup of the pixel detector. For it to be useful also for correcting SEUs during luminosity runs, without causing too much dead time, it must be designed with a higher band width.

In conclusion, single event upset phenomena have been studied with pions for two SOI chip technologies. The results indicate that such effects cannot be totally ignored at the peak luminosities of LHC. However, reset mechanisms, foreseen anyhow in the readout architecture, will after some adaptation be able to cope with the problem, whichever of the two chip technologies will finally be used.

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