CBPF

Front-End Electronics Test System Status Information

(After ASDQ++ boards TEST at CERN)

LHCb Technical Note

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Abstract

A Front-End Electronics Test System (FEET) has been implemented in order to test the Front-end electronics (FEE), in the production line, for the LHCb Muon System. It has been developed 5 different procedures according to the following tests: Connectivity, Crosstalk, Equivalent-Noise-Charge, Sensitivity and Rate-Method. This document presents the completed work and discusses also some aspects related to the test of ASDQ++ boards where the system has detected 24 channels with problems out of 640 tested channels.

Content

1 Introduction

The **Front-End Electronics Test System** (FEET) [1] has been implemented to test the FEE for the LHCb Muon System. The System was implemented in order to be compatible with the ASDQ++ [2-4-5] and the CARIOCA [3] boards. A total of 40 ASDQ++ boards were tested at CERN. The results analysis was used to evaluate the FEET System as its current state during the test period, and they will be discussed in this document, as well as some rate method related aspects. In the 5th Chapter we present the improvements done after testing evaluation.

2 Proposed Tests

2.1 Connectivity

In an electronic circuit and board development, the assembling phase usually gives the main failure factor because of bad connections between components and print circuit board. For this reason and taking into account that such a test allows easy and fast detection of failures we have considered the connectivity procedure as the first one to be executed in the board test sequence. Connectivity is tested by means of charge injection pulse, having previously adjusted the threshold to a certain value far from noise region. In this way all the path from the input to the output lines is tested.

2.2 Crosstalk

An important requirement for the LHCb Muon front-end electronics is to keep crosstalk between its lines near to zero for the experiment threshold value. An easy way to test such characteristic is setting the threshold to such a value and injecting high frequency and charge value signal into a channel while controlling if the neighbors channels are kept in silence. With this test it is possible to calculate the probability, given a threshold value, to happens a hit due to crosstalk phenomena between front-end input lines.

2.3 Sensitivity and Offset

The correspondence between injected charge and threshold voltage can be obtained using either threshold and charge scan. FEET possibilities sensitivity and offset measurement by means of injected charge scan (between roughly 5 and 150fC) for a few set of threshold voltages.

2.4 Equivalent Noise Charge and True Threshold

Considering a charge sensitive amplifier, noise effects amplitude measurement resolution and, consequently, minimum detectable charge. Because of noise presence, for each charge injection value the amplifier response has a certain statistic distribution. The probability density function describing the amplifier response in the presence of a Gaussian noise can be expressed by:

$$f(Q) = \frac{1}{\sigma_n \sqrt{2\pi}} e^{-\frac{1}{2}\frac{(Q-Q_{in})^2}{\sigma_n^2}} \qquad (1)$$

Given a discriminator threshold V_{th} (which is equivalent to a threshold value in charge Q_{th}), the probability that an input charge Q_{in} results in a discriminator hit is given by:

$$P = \int_{Q_{th}}^{\infty} \frac{1}{\sigma_n \sqrt{2\pi}} e^{-\frac{1}{2}\frac{(Q-Q_{in})^2}{\sigma_n^2}} dQ \qquad (2)$$

Such a equation can be represented in terms of the error function:

$$P = \frac{1}{2} - \frac{1}{2} erf\left(\frac{Q_{th} - Q_{in}}{\sigma_n \sqrt{2}}\right) \qquad (3)$$

The equivalent noise charge (ENC) can be obtained from the sigma value of the derivative analysis of the error function which represents the discriminator response for a injected charge scan for a given threshold. In practice an approximated value can be obtained directly as represented in Fig.1:

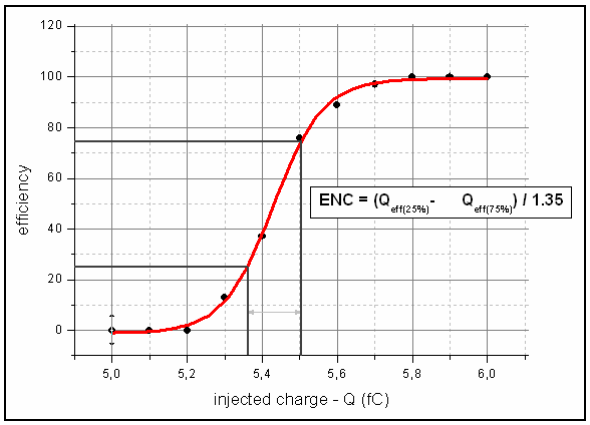


Fig. 1 – Equivalent Noise Charge measurement method illustration.

2.5 Noise Rate versus Threshold Response

As known, theoretically a white noise process contains all frequency components in equal intensity. In practice, given a noise signal presence in a system and if it has an flat bandwidth which covers the system bandwidth range, this noise can be treated, for this system, as an white noise process. Because of these power spectra characteristics of such a noise, evaluating the response of a front-end to the white noise it is possible to reconstruct the characteristics of its own bandwidth spectra.

Considering a Gaussian noise presence in a discriminator input, one can expect a threshold to noise ratio as illustrated in Fig.2 (not considering response time dependence). From equation (2) (in terms of Volts), considering the case without injection and with a signal baseline equal to $V_{offset,}$ one can represent the noise rate crossing threshold level by:

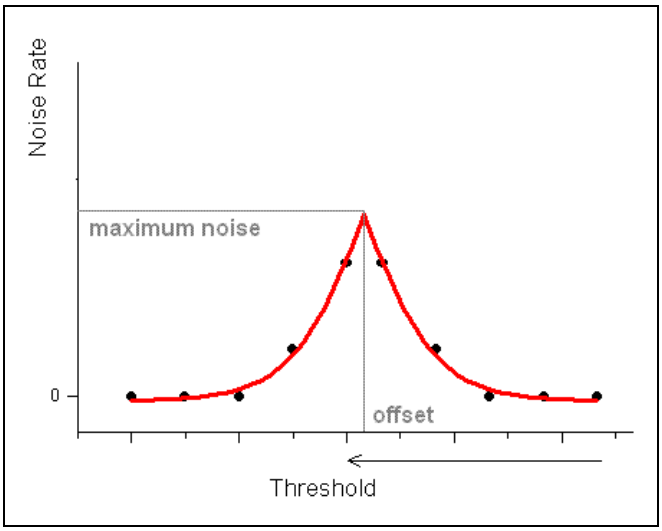


Fig. 2 – Noise rate versus threshold not considering circuit response time limitations.

$$f(V) = f_{n0} \int_{V_{th}}^{\infty} e^{-\frac{1}{2}\frac{(V-V_{offset})^2}{\sigma_n^2}} dV \qquad \text{for } V_{th} \geq V_{offset} \text{ and}$$

$$f(V) = f_{n0} \int_{V_{th}}^{-\infty} e^{-\frac{1}{2}\frac{(V-V_{offset})^2}{\sigma_n^2}} dV \qquad \text{for } V_{th} < V_{offset}$$

(not taking into account the dead time circuit characteristic)

Where V_{th} is the threshold, σ_n provides the equivalent noise in volts and f_{n0} is the sum of amplitude occurrences up to the mean value of the noise Gaussian amplitude distribution (the maximum possible rate is a function of f_{n0}).

If we consider a Gaussian time distribution the threshold to noise ratio can be represented as follows:

$$f(V_{th}) = f_{n0} e^{-\frac{1}{2}\frac{(V_{th}-V_{offset})^2}{\sigma_n^2}}$$

Using the subsequent formula [7] it is possible to calculate the maximum noise rate f_{n0} in terms of cutoff frequencies bandwidth parameters (as the discriminator is sensitive only to positive edge excursions, actually the maximum possible rate will be half of f_{n0}):

$$f_{n0} = 2\sqrt{\frac{1}{3}\frac{f_2^3 - f_1^3}{f_2 - f_1}}$$

Taking into account the observations above one can conclude that by means of threshold scan it is possible to obtain information about 2 important parameters of the circuit located before the discriminator: the bandwidth and the equivalent noise. A preliminary study has been made for the LHCb front-end electronics [4] and we have implemented this analysis to evaluate the method efficiency as a tool of diagnostics for the LHCb Muon Chamber Readout Electronics.

3 System Description

3.1 Hardware

The main building blocks of the Front-end Electronics Test Station are a charge injection board (CIB), an acquisition and counting device and a National Instruments acquisition board.

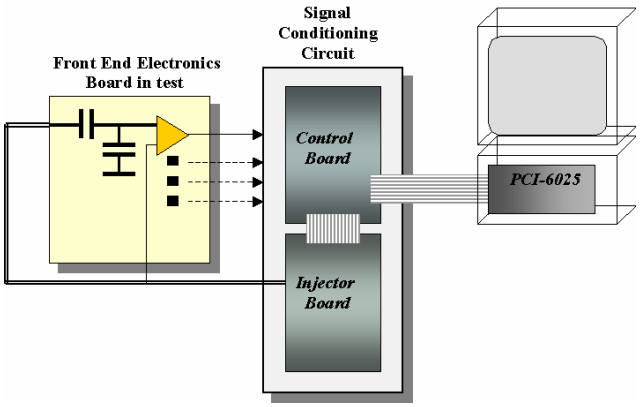


Fig. 3 – FEET schematic diagram.

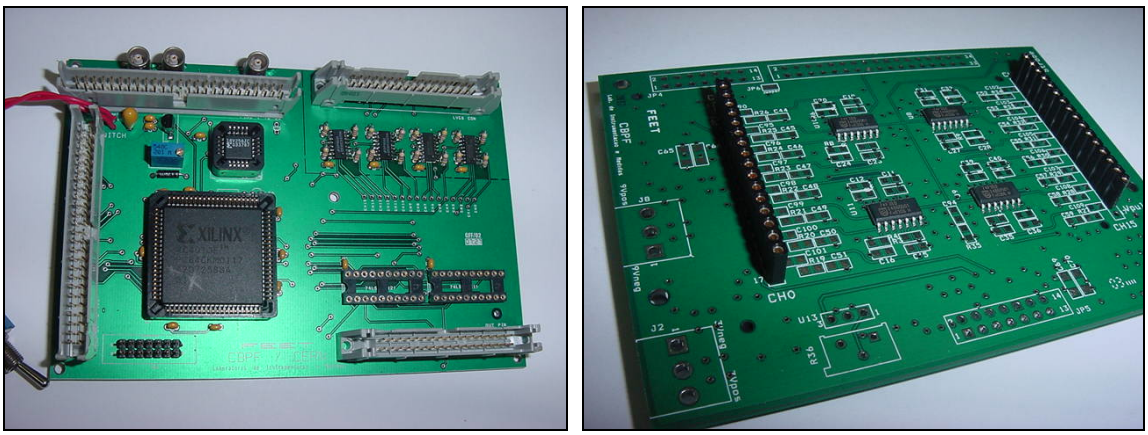


Fig. 4 – Control & Data Acquisition and Injection Boards.

The control board is based mainly on a FPGA (Xilinx XC4010E) VHDL implementation. Such a implementation can be separeted in three blocks:

1) FEB Readout: It receives 16 differential channels from the FEB under test and processes data by means of 8 counters multiplexed to hand out all 16 inputs.
2) CIB Control: The control board controls the CIB logical parameters and assurances that charge injection pulses are synchronized to readout process.
3) Computer data transfer: This block is responsible to carry out parallel data transfer between electronics and PC via the National Instruments board (NI-DAQ PCI6025).

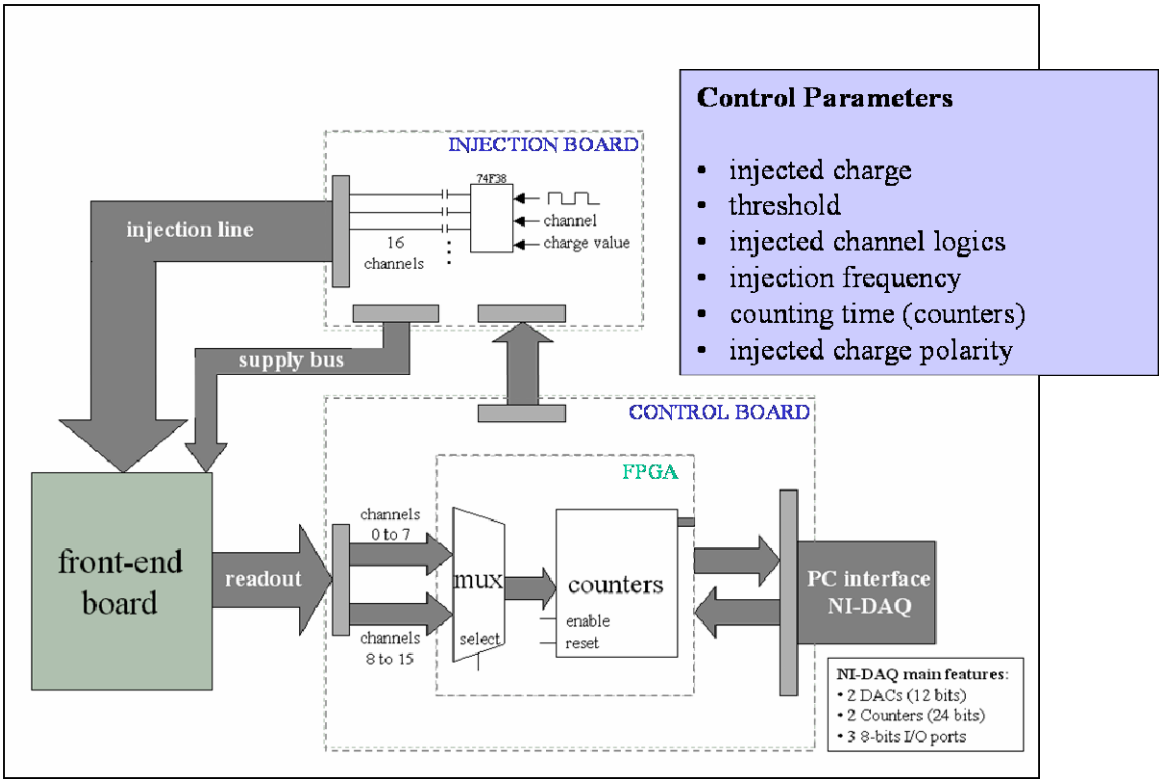


Fig. 5 – FEET data processing diagram.

The injector board contains 16 channels and its circuitry permits a fine tuning of injected charge (in the range of few fC), injection rate control and positive and negative charge injections (all controlled remotely and synchronized to the control board).

3.2 Software

A LabVIEW based program has been developed to control and process data, execute tests, data analysis and archiving. Five procedures have been implemented to test and evaluated FEE characteristics as indicated on chapter 2.

Each test has been implemented in a different panel and all procedures and diagnostics parameters are controlled and accessed from a main panel (Fig.6). Every panel offers real time graphics which allow the operator to follow the acquisition process on-line and to easily debug the board under test in case of failure (see panels in appendix A). It also

has been foreseen an easy way to enter with test and calibration parameters into 2 different panels and to store them to be loaded any time later.

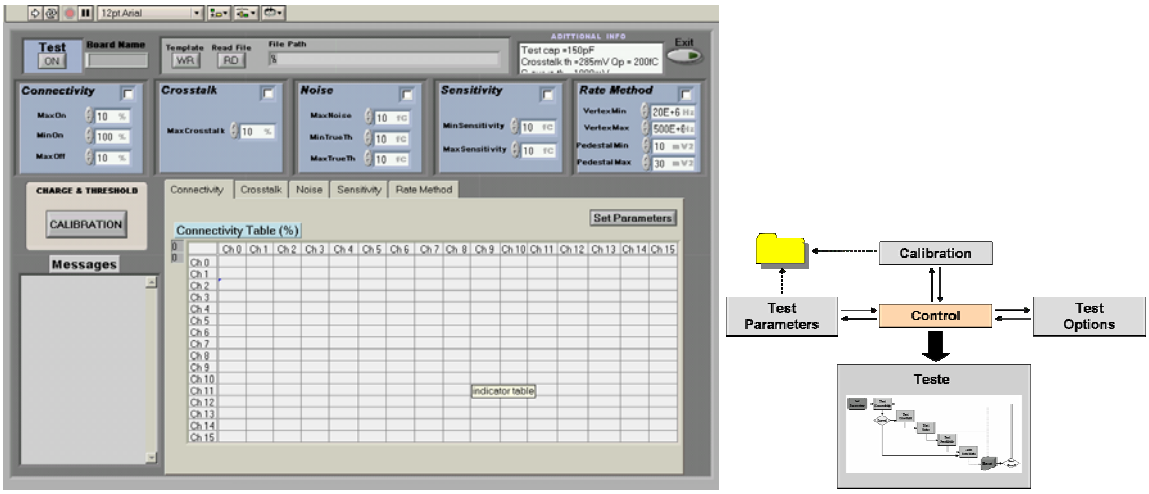


Fig. 6 – Control panel and software general diagram.

4 Test Results

The ASDQ++ boards were separated into two groups, the new ones (30 boards) which arrived at CERN without any previous test and the ones which were already available at CERN by the tests period.

The routine for the tests was based on the diagram presented in the Fig.7. Once a channel connectivity failure is detected (opened or short-circuited) the following procedures, Crosstalk, Noise and Sensitivity, are ignored and the board goes directly to the Rate Method test for analysis purpose.

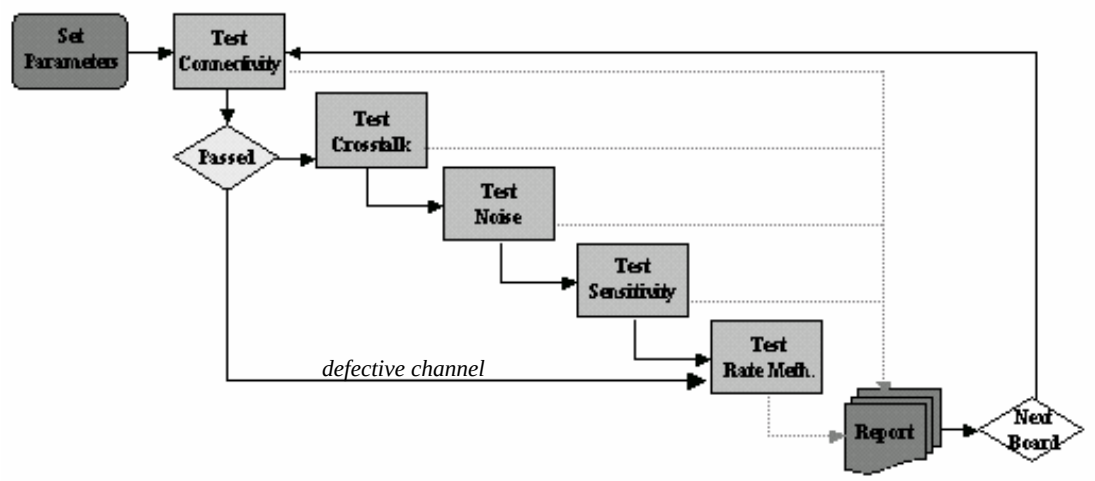


Fig. 7 - Testing sequence block view.

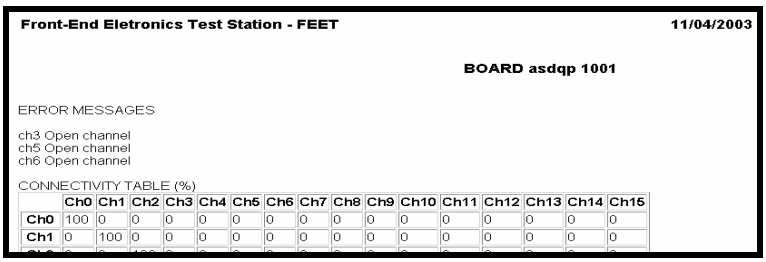
A 150pF input capacitor was used for all the tests. The used threshold value is the one measured at the ASDQ++ board input; only in the Crosstalk Test the threshold was

measured at the PCB connector named ST1, which corresponds to the threshold on the chip. We have set the ATT pin, offered by the ASDQ chip, to +3V, which attenuates the circuit gain by factor 2, see Ref. [5].

During the test of all 640 channels, 24 malfunctioning channels have been individualized (all from the 30 new boards just arrived at CERN) while the boards that were already in use at CERN have not shown any failure.

4.1 Test Report

The software allows to save all the data measured through the test and, when the test is finished, it generates a report file (.htm). The report given comes with the board name, error messages, test tables (with test parameters), date, and some relevant test conditions at the end. It begins as shown in Fig.8.



Front-End Eletronics Test Station - FEET 11/04/2003

BOARD asdqp 1001

ERROR MESSAGES

ch3 Open channel
ch5 Open channel
ch6 Open channel

CONNECTIVITY TABLE (%)

	Ch0	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7	Ch8	Ch9	Ch10	Ch11	Ch12	Ch13	Ch14	Ch15
Ch0	100	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Ch1	0	100	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fig. 8 - Final report document.

4.2 Connectivity

It is the simplest test but the one that will recognize most of the problems, in a very fast way. If there is any opened or short-circuited channel it is recognized by this test and with its results we can avoid doing the other tests on the failing channels. A table from the ASDQp1008 is shown in Fig.9.

CONNECTIVITY TABLE (%)

	Ch0	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7	Ch8	Ch9	Ch10	Ch11	Ch12	Ch13	Ch14	Ch15
Ch0	100	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Ch1	0	100	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Ch2	0	0	100	0	0	0	0	0	0	0	0	0	0	0	0	0
Ch3	0	0	0	100	100	0	0	0	0	0	0	0	0	0	0	0
Ch4	0	0	0	100	100	0	0	0	0	0	0	0	0	0	0	0
Ch5	0	0	0	0	0	100	0	0	0	0	0	0	0	0	0	0
Ch6	0	0	0	0	0	0	100	0	0	0	0	0	0	0	0	0
Ch7	0	0	0	0	0	0	0	100	0	0	0	0	0	0	0	0
Ch8	0	0	0	0	0	0	0	0	100	0	0	0	0	0	0	0
Ch9	0	0	0	0	0	0	0	0	0	100	0	0	0	0	0	0
Ch10	0	0	0	0	0	0	0	0	0	0	100	0	0	0	0	0
Ch11	0	0	0	0	0	0	0	0	0	0	0	100	0	0	0	0
Ch12	0	0	0	0	0	0	0	0	0	0	0	0	100	0	0	0
Ch13	0	0	0	0	0	0	0	0	0	0	0	0	0	100	0	0
Ch14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	100	0
Ch15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	100

Fig. 9 - Connectivity table example (short-circuit between ch3 and ch4).

4.3 Crosstalk

Crosstalk is the second test to be executed in the FEET test sequence. For this test we worked with threshold around 285mV. With such a threshold any of the channels presented crosstalk over 1% of the injected rate. The analysis have indicated that better grounding and shielding are necessary in order to work with a lower threshold value.

4.4 Sensitivity and Offset

Sensitivity tests have shown very stable results. The new ASDQ++ boards sensitivity, with C = 150pF of input capacitance, was around 10mV/fC with a standard deviation of 0.19 as shown in Fig.10.

Fig.11 shows the ASDQp1010 channel-7 graphic and the ASDQp1005 board sensitivity test results.

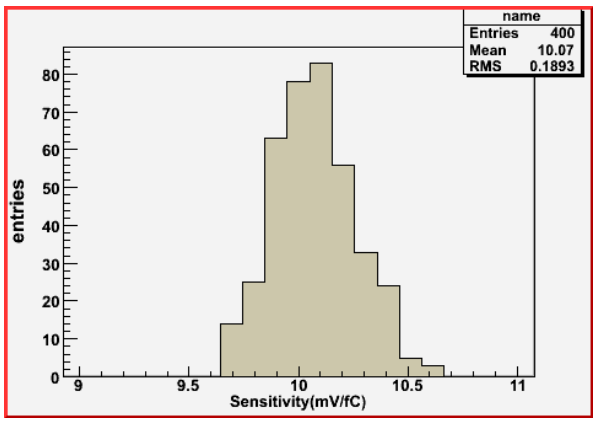
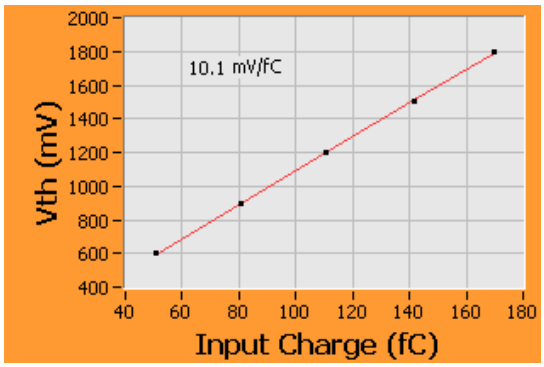


Fig. 10 – Sensitivity distribution.



SENSITIVITY TABLE

	mV/fC	offset (mV)
Ch0	10.0	81.8
Ch1	10.1	52.4
Ch2	10.0	81.8
Ch3	10.0	66.1
Ch4	9.8	68.1
Ch5	9.9	63.6
Ch6	9.8	87.1
Ch7	10.0	41.1
Ch8	10.1	35.7
Ch9	10.2	84.7
Ch10	10.1	71.9
Ch11	10.0	79.6
Ch12	10.1	78.9
Ch13	10.1	95.3
Ch14	10.1	86.7
Ch15	10.0	91.7

Fig .11 - Sensitivity curve and test table examples (given by FEET software) .

Offset results has shown that a better calibration is needed in order to get absolute values. Another important component is the power supply voltage variation dependence

which can make offset calibration change day by day. After tests it has been implemented a new board to regulate the external power source which supplies the test station electronics.

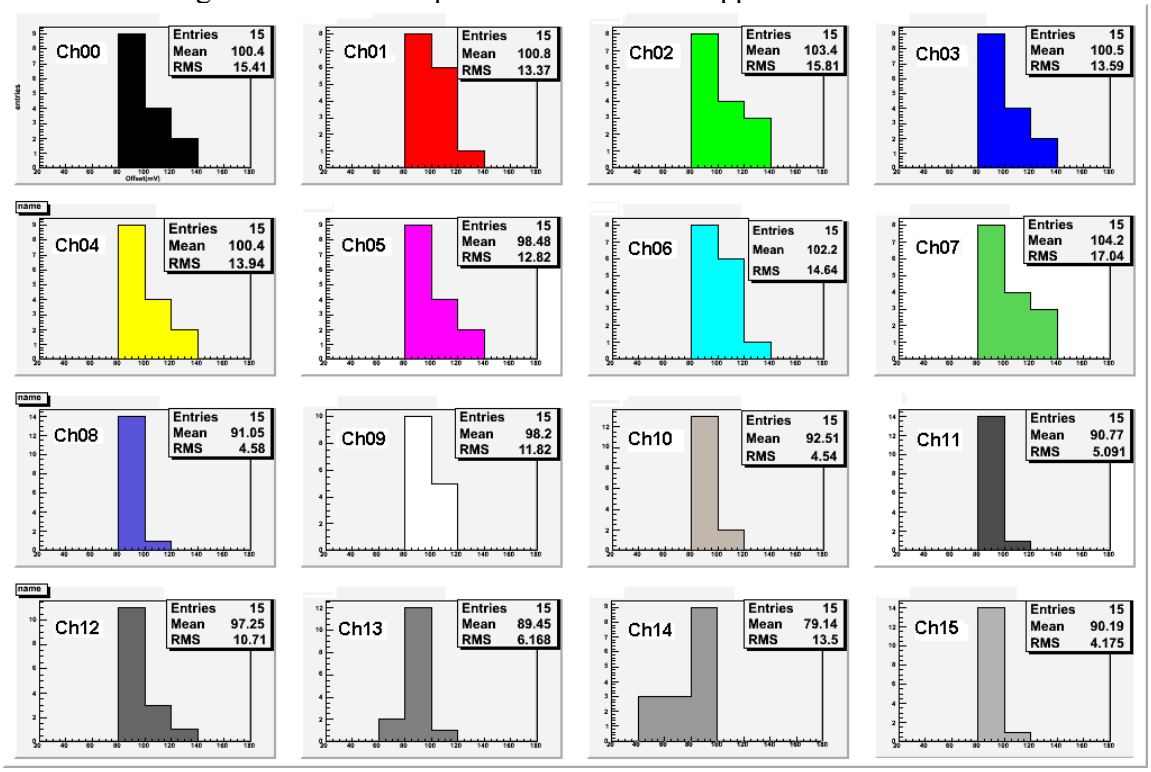


Fig. 12 - Offset results by channel.

4.5 Equivalent Noise Charge and True Threshold

The Noise tests presented stable results and the S-curve acquisition and fitting processes worked as expected, having 100% efficiency through all the tests. The new ASDQ++ board presented a mean value of 1,25fC (Fig.13) while the old boards has given a mean value of 1,5fC (Fig.14).

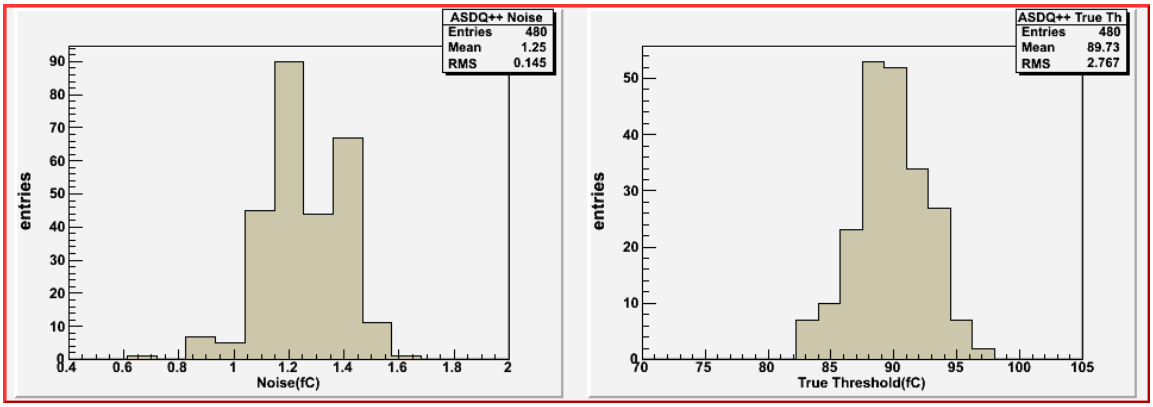


Fig. 13 - ENC distribution.

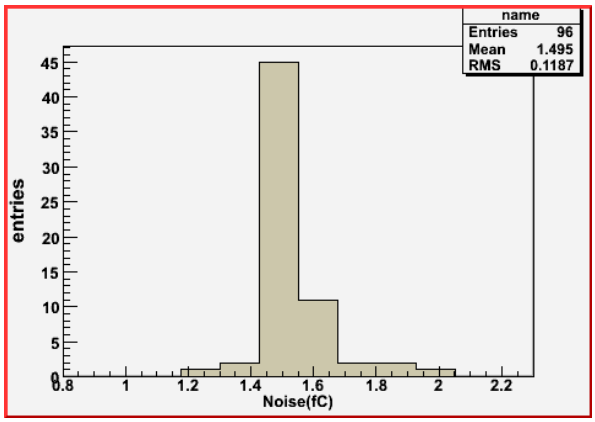
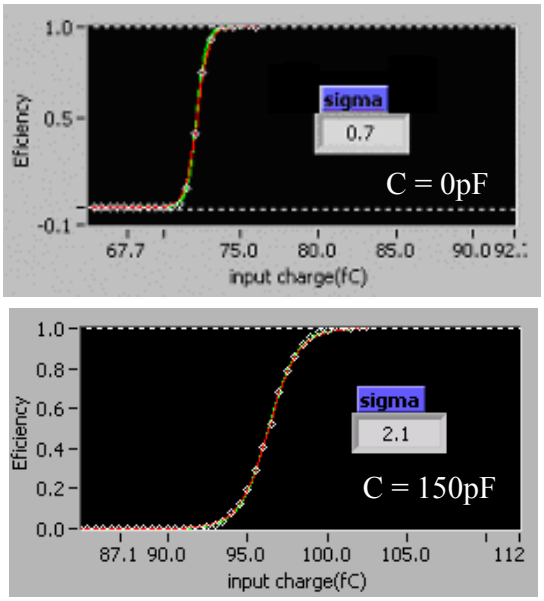


Fig. 14 - ENC distribution for the old boards.

Fig.15 shows the ASDQp1009 test table, and two S-curves (data and fitting), for 0pF and 150pF input capacitance.



NOISE TABLE

	sigma (fC)	true th (fC)
Ch0	2.1	97.4
Ch1	2.0	95.6
Ch2	2.0	94.3
Ch3	2.0	96.9
Ch4	2.1	93.1
Ch5	2.1	97.4
Ch6	2.3	94.0
Ch7	2.2	94.7
Ch8	2.1	98.5
Ch9	2.2	98.7
Ch10	2.1	97.6
Ch11	1.9	96.9
Ch12	2.2	96.8
Ch13	2.1	98.5
Ch14	2.1	98.9
Ch15	2.2	96.9

Fig. 15 - Noise acquisition and fit graphics and result table examples (the values presented here must be divided by ~1.5 to have the r.m.s. noise).

4.6 Noise Rate versus Threshold Response

From the ASDQp1001 rate method test table, it is easy to see how channels 3, 5 and 6 are different due to an open connection. Their behavior is like a channel with input capacitance equal to zero, a clear indication to localize the problem. With the four first columns it is possible to rebuild the test curves. Each graphic contains two curves; each curve is related with a different gain set-up of the ASDQ++ chip. The *vertex frequency* represents the y-axis value and the *th_pedestal* represents the x-axis value of the crossing point between both curves, the third and fourth columns represent the x-axis value when y goes to 0.

Fig. 17 shows a noise rate performance of an approved channel when exposed to the threshold scan procedure: It is possible to see the influence of the 150pF input capacitance on the channel output rate behavior. Fig. 18 shows a rejected channel test response: Such a graphic shows a 0pF input capacitance curve like which indicates an open or broken channel.

RATE METHOD

	vertex_frequency (Hz)	th_pedestal (mV^2)	lATT0V_Xmax (mV^2)	lATT3V_Xmax (mV^2)	slope_0V	slope_3V
Ch0	1630059093	14	71	36	-372	-966
Ch1	1214477328	14	76	39	-340	-856
Ch2	1083974762	13	69	34	-371	-989
Ch3	3574234279	10	29	18	-1126	-2727
Ch4	616347886	12	71	34	-345	-926
Ch5	66066940478	7	26	16	-1334	-2702
Ch6	52513460393	7	26	17	-1295	-2572
Ch7	61693822371	13	55	27	-596	-1836
Ch8	1924862212	12	67	33	-388	-1045
Ch9	3729955810	9	63	33	-406	-937
Ch10	670512540	13	73	36	-338	-893
Ch11	817210111	10	66	32	-363	-931
Ch12	918700736	12	69	34	-360	-942
Ch13	1051200036	13	75	38	-337	-845
Ch14	6433002500	11	59	28	-469	-1311
Ch15	20777431782	11	60	28	-486	-1361

Fig. 16 - ASDQp1001 rate method test table.

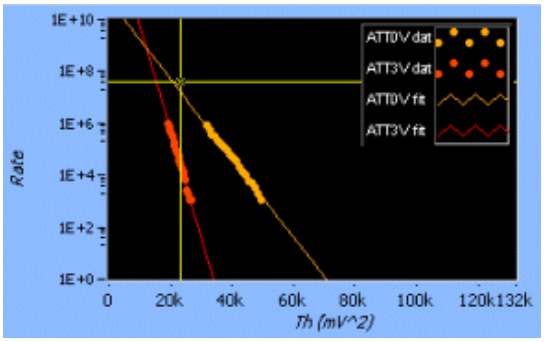


Fig.17 - Test with 150pF input capacitor.

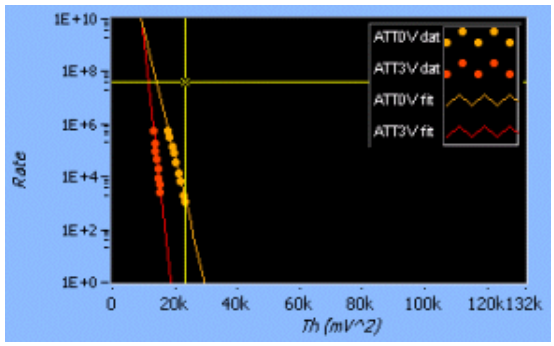


Fig.18 - ASDQp1001 channel-3 result.

In a well-behaved channel test, the curve parameters, given by the rate method table, provide important information but different kind of problems are expected and some times these parameters are not enough to describe a channel behavior through the rate method test. Fig. 19 and 20 show the graphic result of two open channels, the ASDQp1002 channel 7 and ASDQp1017 channel 5, Although the channel in the Fig. 20 test is open, the rate method parameters would respect the values expected. These results show that a diagnostic on the fitting mean squared error (mse) must be taken in account in order to, in case the test presents an mse over the expected value, indicate whether examinations on the data points should be made.

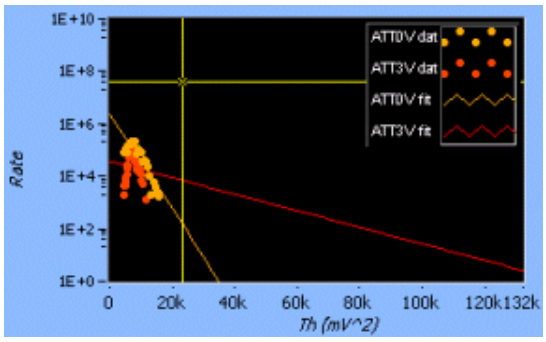


Fig. 19 - ASDQp1002 channel 7 result

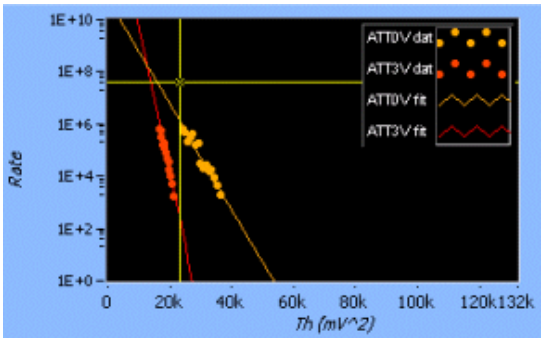


Fig. 20 - ASDQp1017 channel 5 result

Further analysis indicates the efficiency to obtain the equivalent detector capacitance by evaluating the rate method slope.

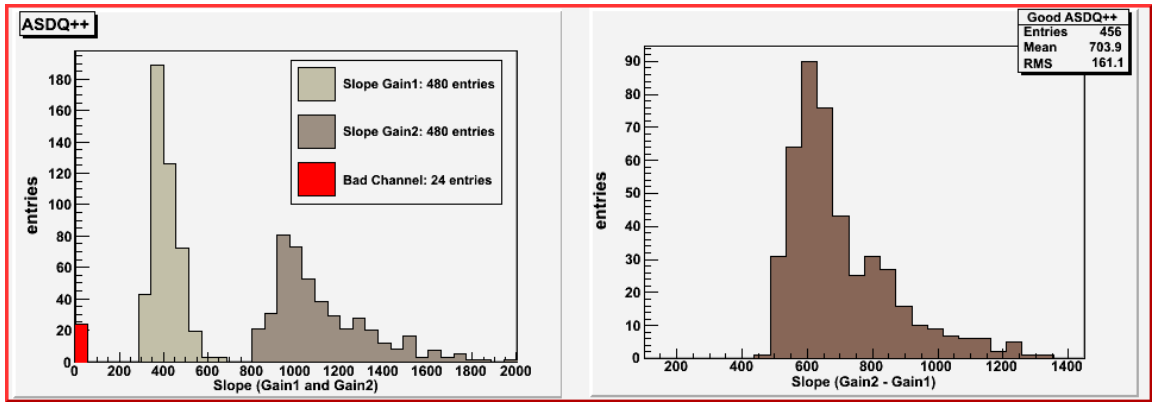


Fig. 21 - Noise rate versus threshold angular coefficients for both ASDQ++ gains (the fault channels were positioned to zero for illustration reasons).

Noise interference between channels has been identified indicating once more that grounding and shielding setup are susceptive to noise feedback. From Fig.22 it is possible to see how channels near the board limits contain higher noise levels when evaluating the vertex frequency given by the rate method curves.

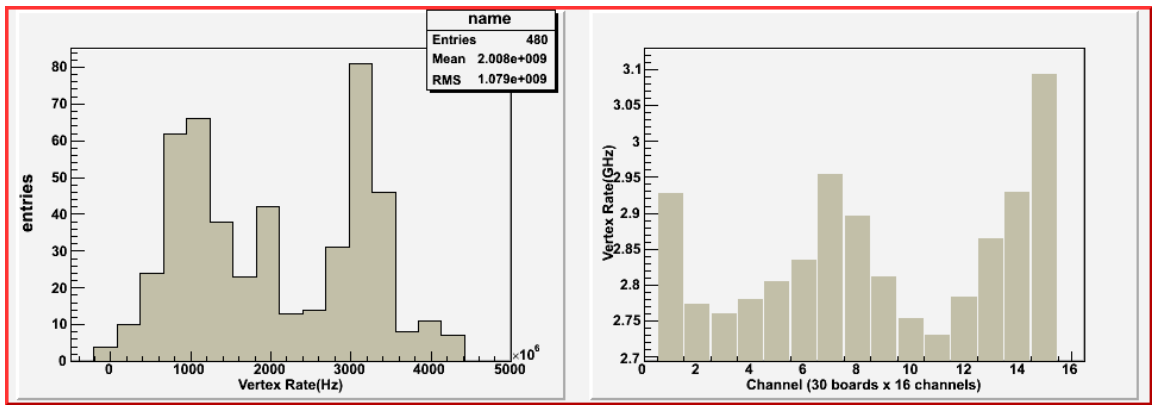


Fig. 22 – ASDQ++ vertex frequency during CERN tests.

4.7 ASDQ++ Diagnostics

The positive-board problems were quickly investigated and most of them were found in the input transistor pin connections as listed in table 1, full information about ASDQ++ board can be found in Ref.[5].

Table 1 - Problems found on the boards after diagnostics indication. Transistors are indicated by Q (the channels numeration is considered from 00 to 15)

ASDQp1001 Channel 03 – component Q68, base lead is not connected to GND Channel 05 – component Q24, base lead is not connected to GND Channel 06 – component Q47, base lead is not connected to GND
ASDQp1002 Channel 7 – component Q69, base lead is not connected to GND
ASDQp1004 Channel 04 – component Q1, base lead is not connected to GND
ASDQp1007 Channel 08 – component Q2, base lead is not connected to GND
ASDQp1008 Channel 03 and 04 – short-circuited between component pads R102-R104
ASDQp1012 Channel 00 – component Q0, base lead is not connected to GND
ASDQp1017 Channel 5 – unknown (Open Channel)
ASDQp1018 Channel 12 – component Q3, emitter lead is connected to GND

Table 2 indicates the defective channels for the negative boards given by the FEET test diagnostics. It should be investigated where the problems are located.

Table 2 - Problems found on the negative boards by FEET diagnostics

ASDQn0003 Channel 01 – Open Channel Channel 02 – Open Channel Channel 03 – Open Channel Channel 04 – Open Channel Channel 05 – Open Channel Channel 06 – Open Channel Channel 07 – Open Channel Channel 14 – Open Channel ASDQn0008 Channel 01 – Open Channel Channel 15 – Noisy Channel ASDQn0009 Channel 01 – Open Channel ASDQn0013 Channel 01 – Open Channel ASDQn0014 Channel 06 – Open Channel ASDQn0017 Channel 03 – Open Channel

5 System Improvements

To solve grounding imperfections two new boards have been projected: an charge injector board with 1 layer only for grounding a another only for the supply net (Fig.23) and a power supply board to guarantees stability on the supply voltage. For the shielding, a faraday cage was constructed.

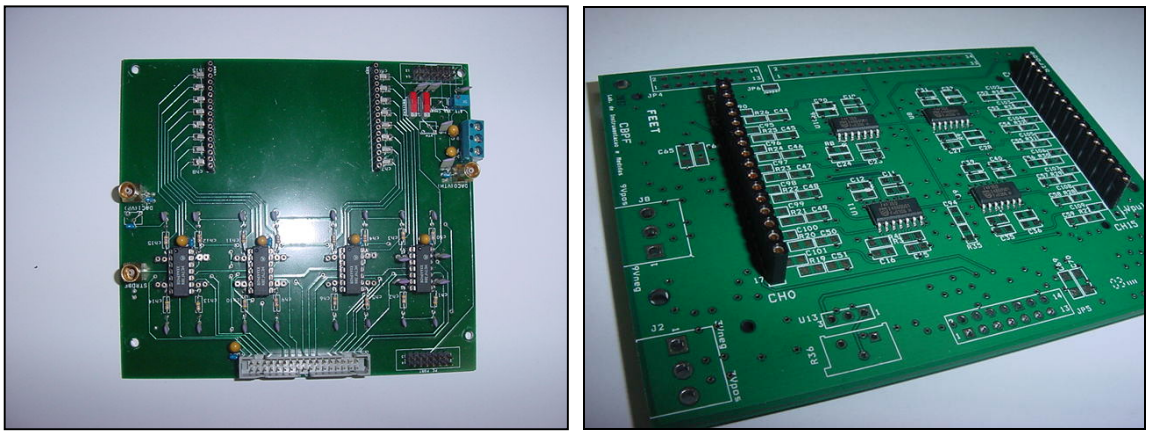


Fig. 23 – Old and new Injection Boards.

Noise analysis with 150pF input capacitance have been performed. It has shown stability and satisfactory noise levels to measure front-end characteristics.

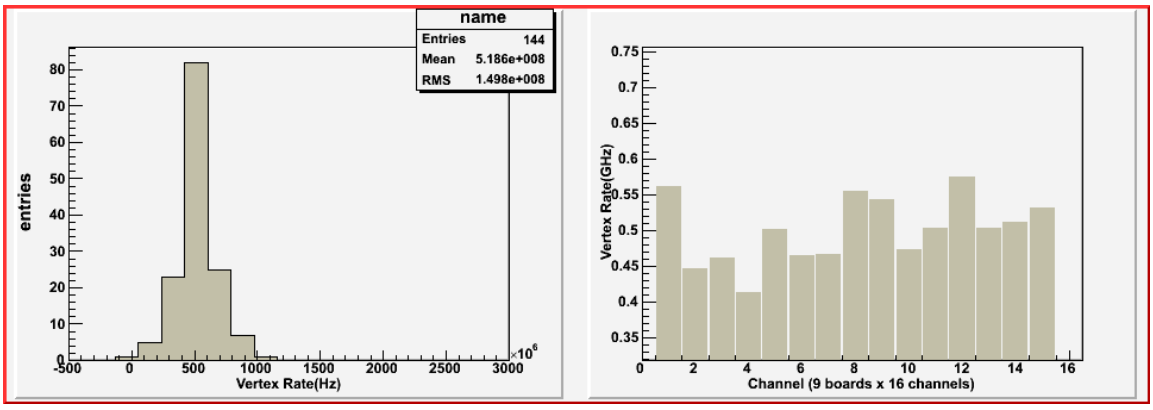


Fig. 24 - ASDQ++ vertex frequency after grounding and shielding improvements.

With the new setup it was possible to measure crosstalk with 150pF input capacitance and a threshold as low as 5.5fC. It has been verified that injection does not add noise to system. Fig.25 shows the noise level with and without injection. Up left table shows crosstalk for a threshold of 5.5fC and injection of 60fC, lower figure shows noise counting when injecting a 60fC charge to channel 7 for a threshold below 5.5fC and figure up left shows the noise behavior for a threshold scan (without injection). All tests have been performed on the same front-end.

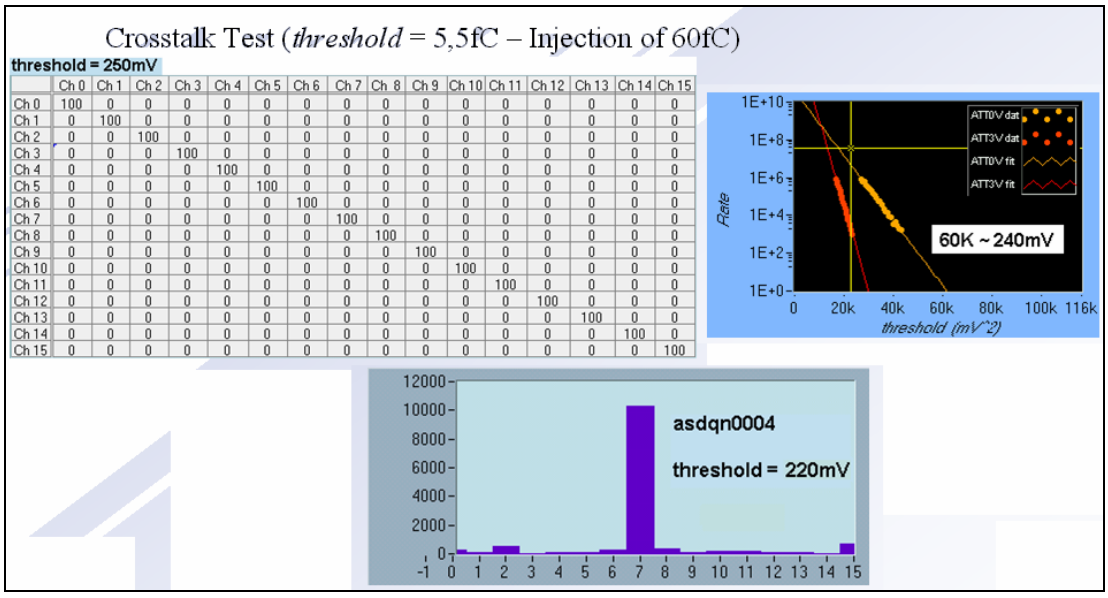


Fig. 25 - Crosstalk test at 5.5fC.

6 Conclusions

This note presents the architecture and results obtained with the FEET System up to December 2003. The first test results meet the expectation, the system could identify 14 out of 40 boards tested with problems, 24 out of 640 channels, but also indicated few components to be adjusted (numerical values presented must be taken as reference). Improvements on the shielding and grounding have been realized offering satisfactory results in all test procedures.

Our main goal was to develop a bench test station for the LHCb front-end electronics and to have an excellent test efficiency on identifying functionality problems on the boards. First analyses indicate good possibilities in the use of noise rate versus threshold method as an in locus diagnostic tool.

7 Acknowledgements

We would like to thank A.Kashchuk, G.Carboni, B.Schmidt, A.Barbosa, J.Miranda and A.Massafferi for support and useful discussion.

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Appendix A: FEET Software Test Panels.

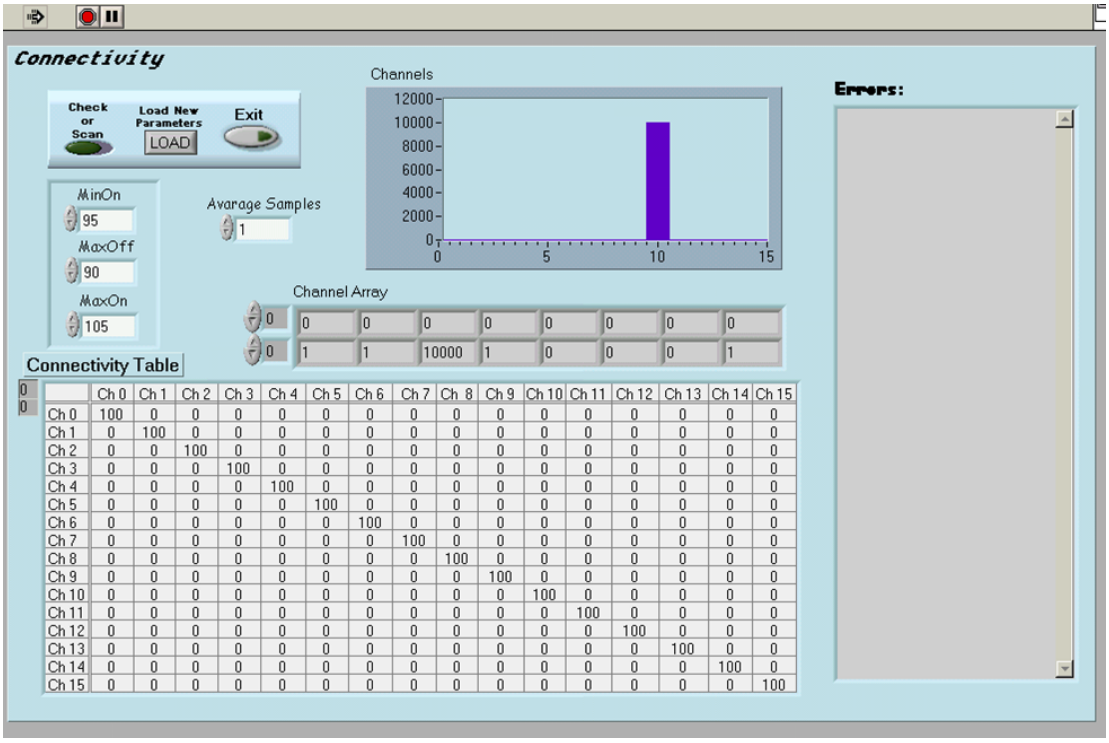

Fig. A1 – Connectivity.

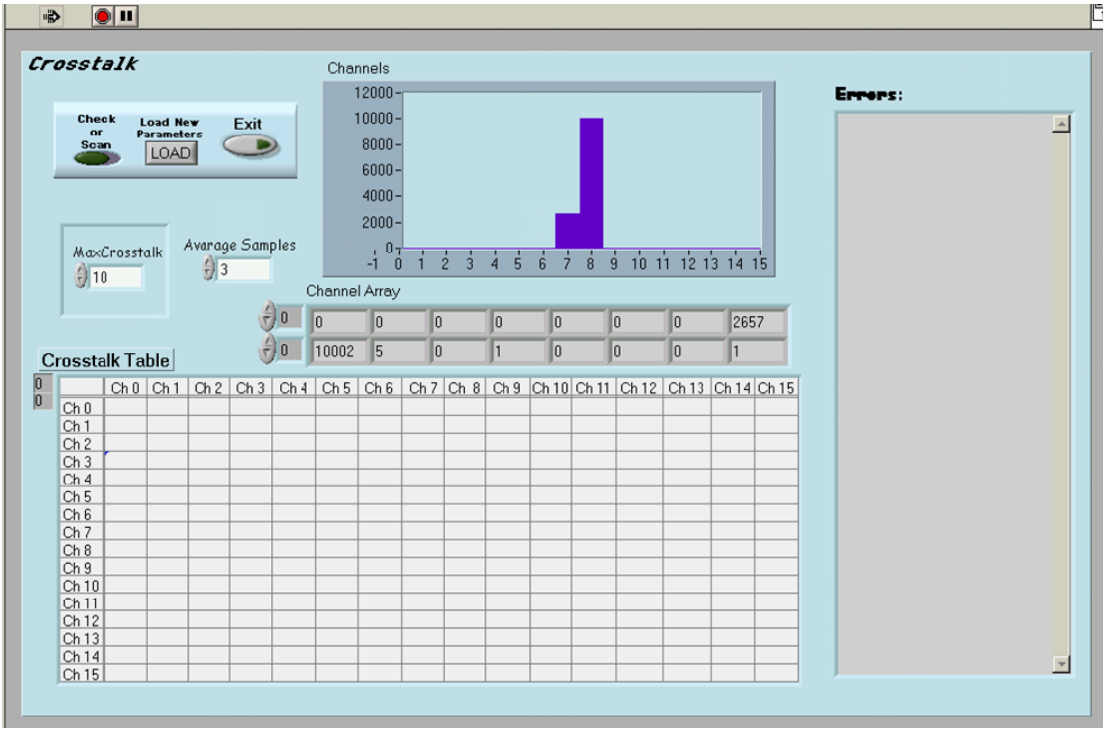

Fig. A2 – Crosstalk.

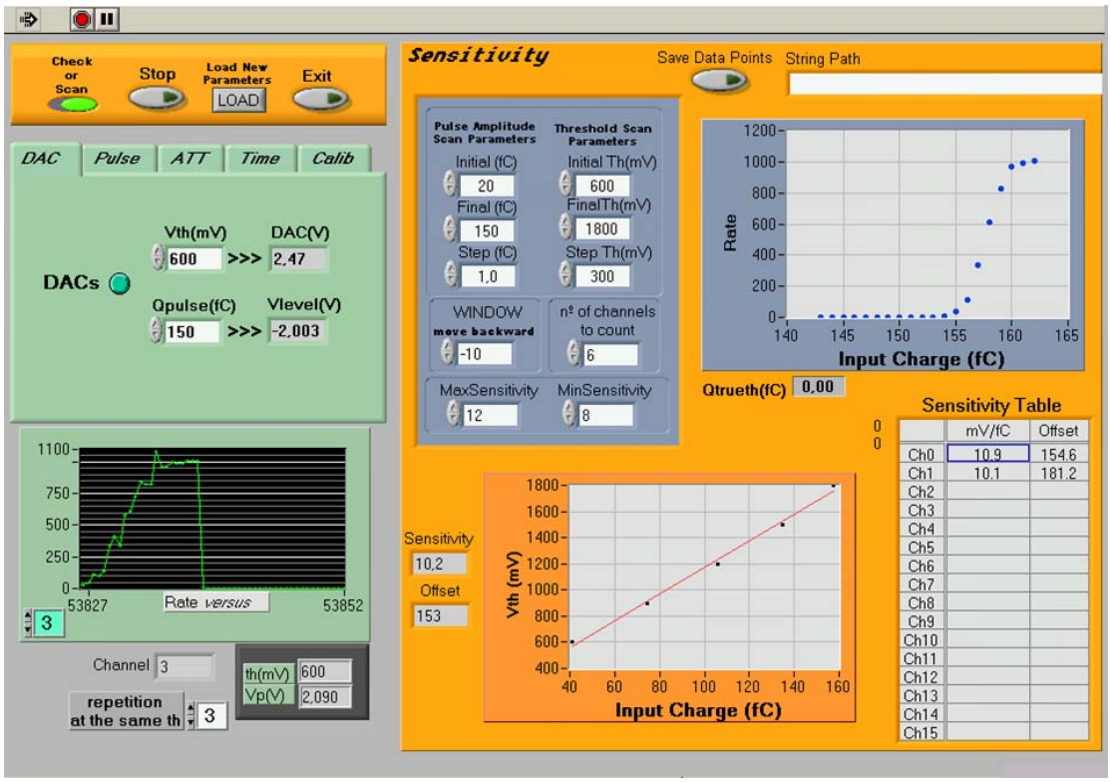

Fig. A3 – Sensitivity and Offset.

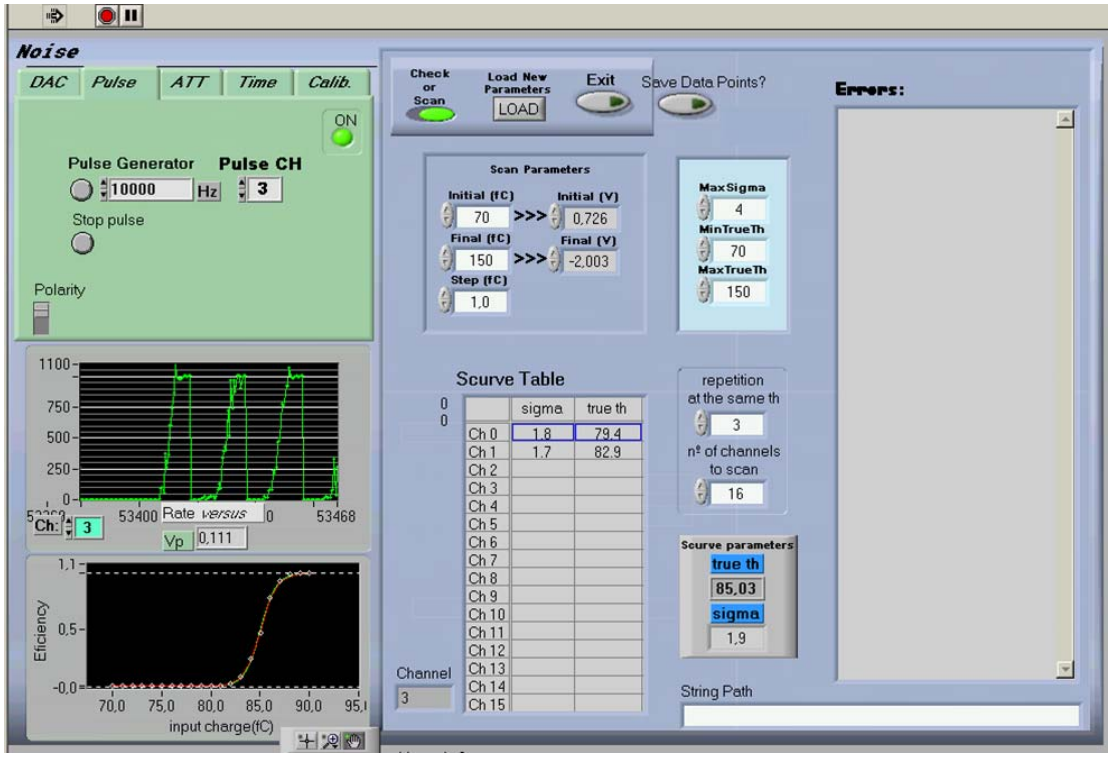

Fig. A4 – Equivalent Noise Charge and True Threshold.

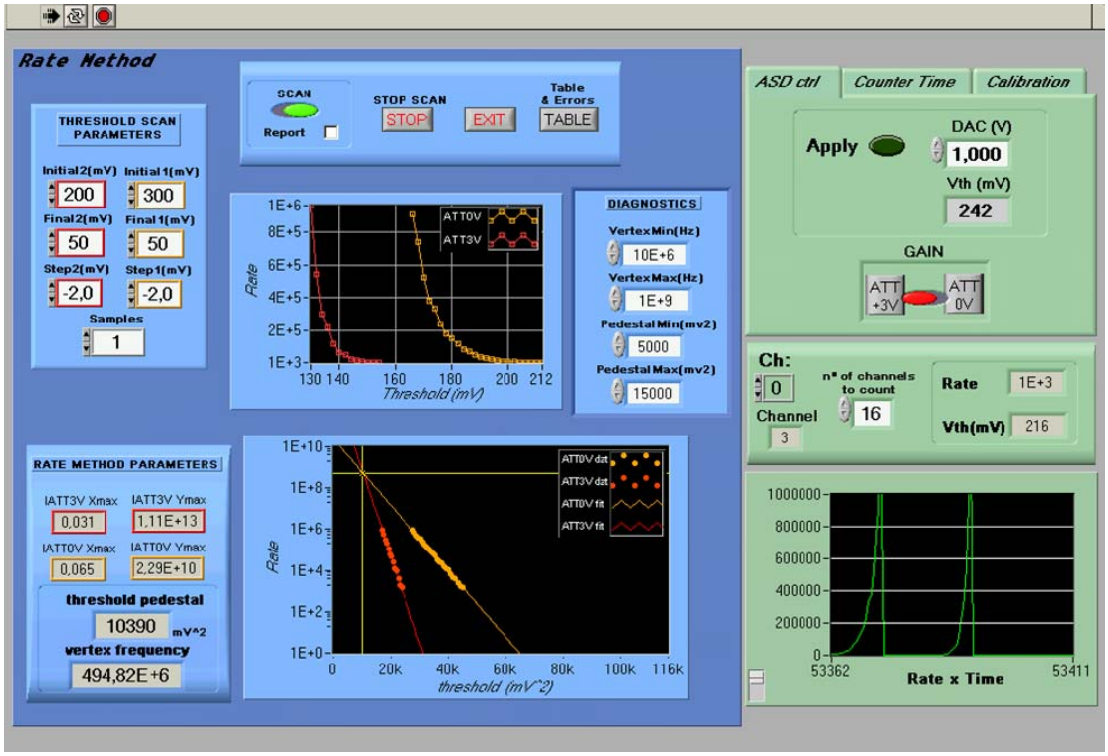

Fig. A5 – Noise Rate versus Threshold.

Appendix B: Circuits schematics.

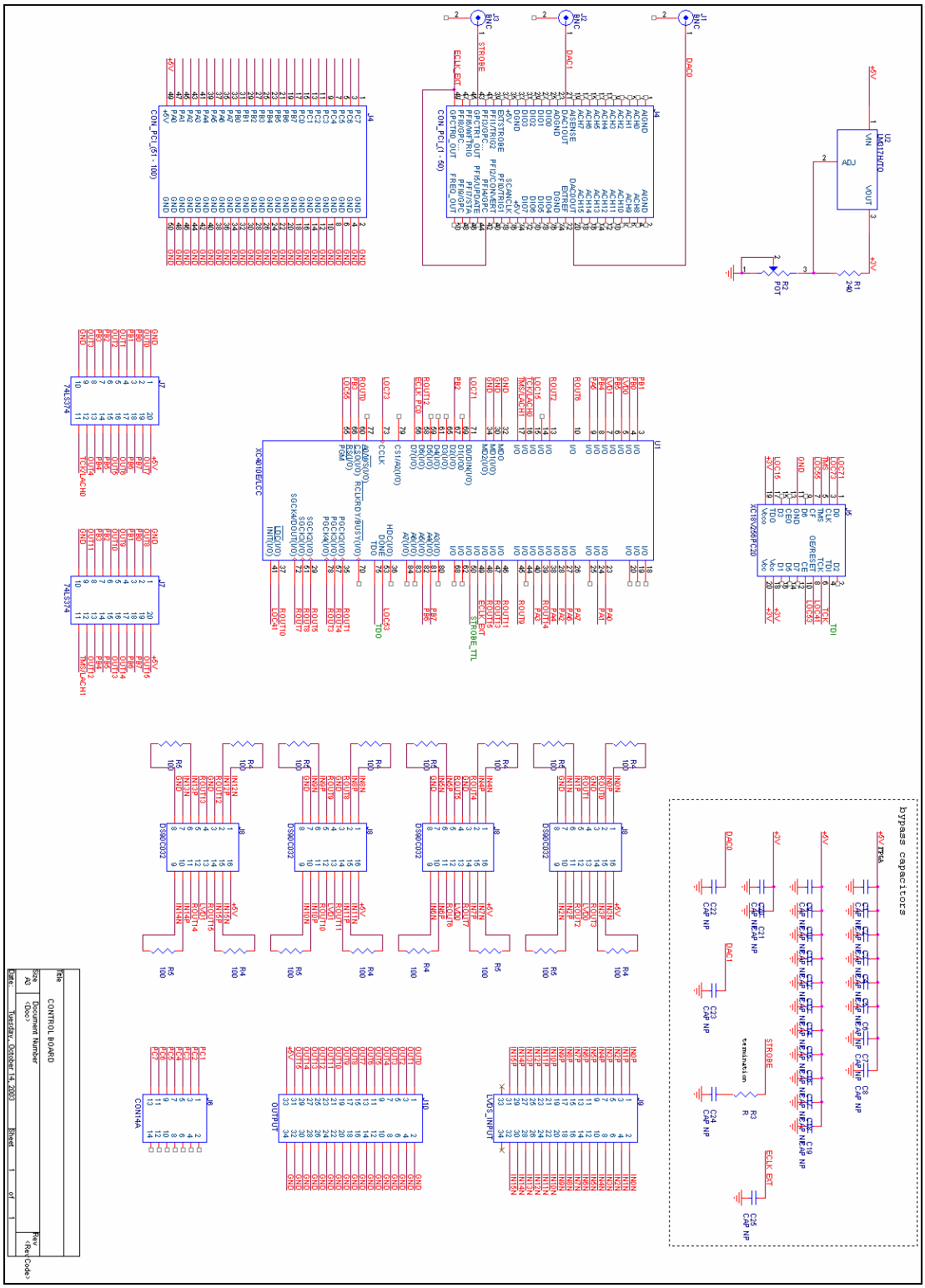

Fig. B1 – Control board schematics.

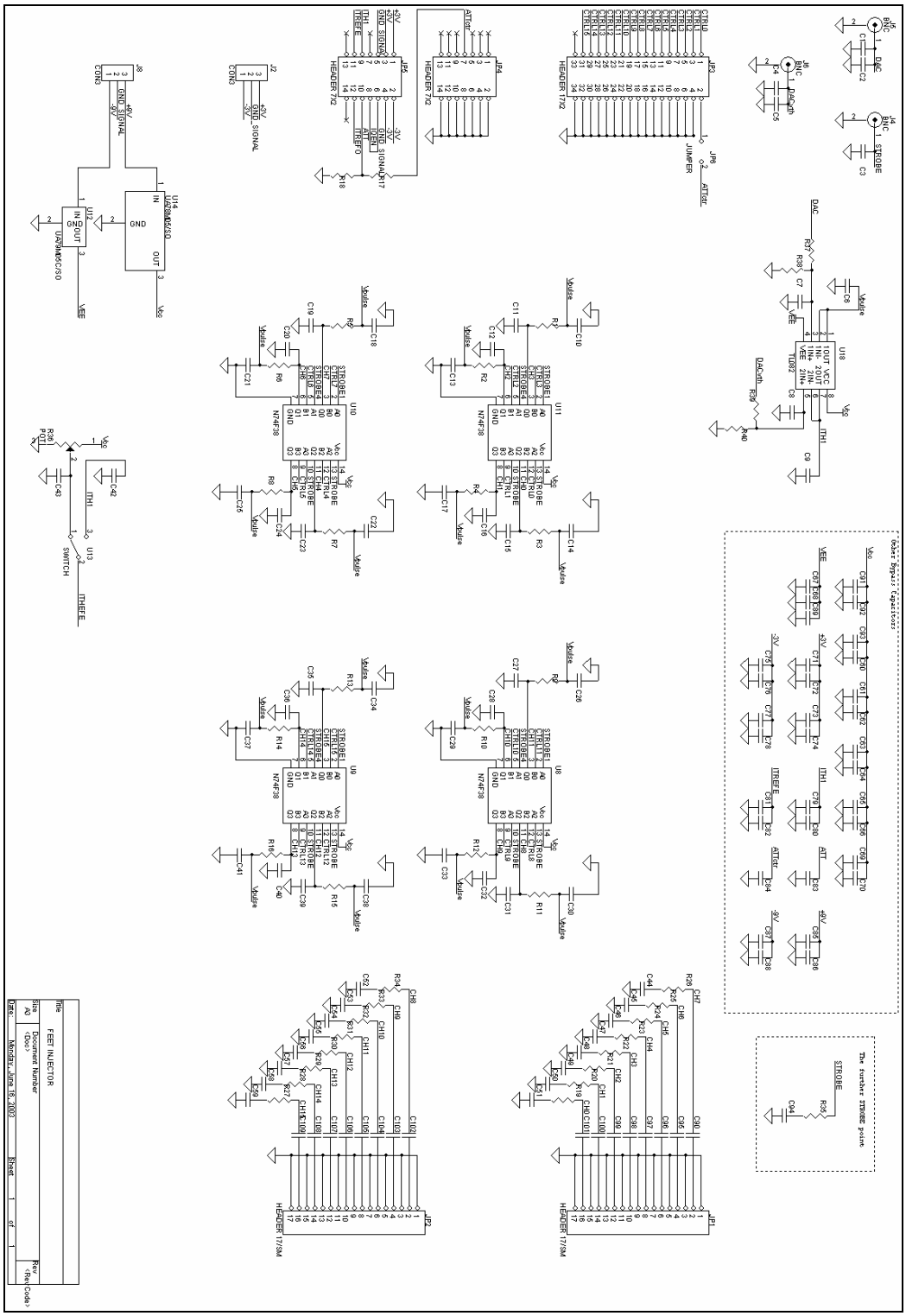

Fig. B2 – Charge injector board schematics.

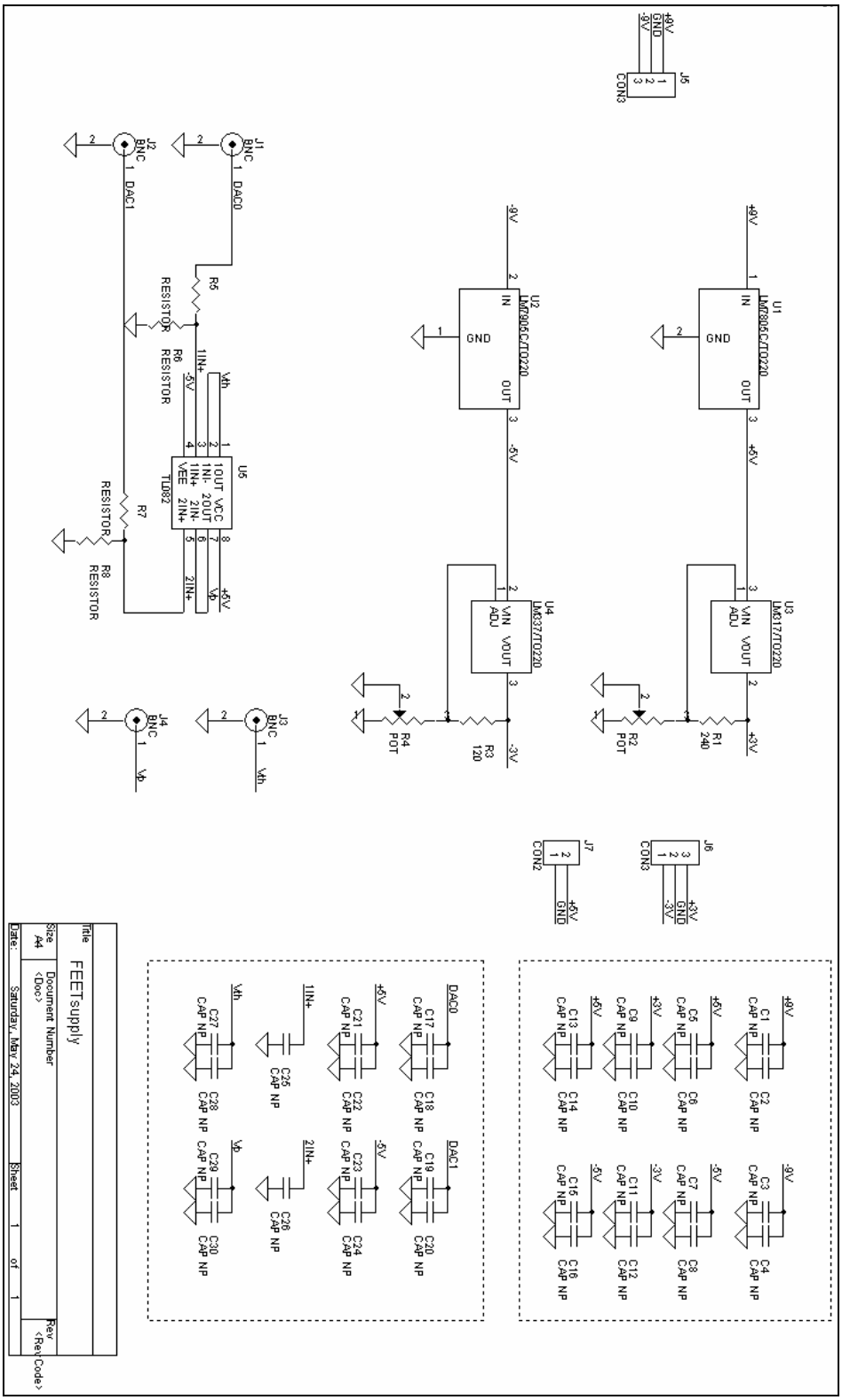

Fig. B3 – Supply regulation schematics.