Software for a FASTBUS Segment Manager/Interface Module

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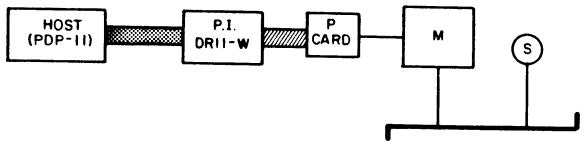
ABSTRACT

An implementation of the FASTBUS standard subroutines in software and firmware for the LeCroy Model 1821 Segment Manager/Interface Module is described. These routines permit complete management of a standard FASTBUS Segment at full FASTBUS speed and support arbitration within the Segment. Data acquisition and transfer rates are presented.

Support for interfaces to CAMAC, ECL links to Event Buffers, and the DEC PDP-11/VAX UNIBUS is discussed. Implications for present and planned data acquisition architectures using multiple Segments are reviewed. A special hardware readout mode for LeCroy high density TDC and ADC data acquisition modules is also discussed.

Introduction

The Model 1821 FASTBUS Segment Manager/Interface (SM/I) is a progammable FASTBUS Master. Its original design intent was to provide a readout module and tester for the LeCroy FASTBUS 1800 Series of data acquisition modules. As more FASTBUS experience was gained, the 1821 SM/I's programmability provided users with a great deal of flexibility in designing and implementing FASTBUS data acquisition systems. The intent of this paper is to describe the current status of the software and also to describe various architectures that have already been implemented (Figures 1 and 2).



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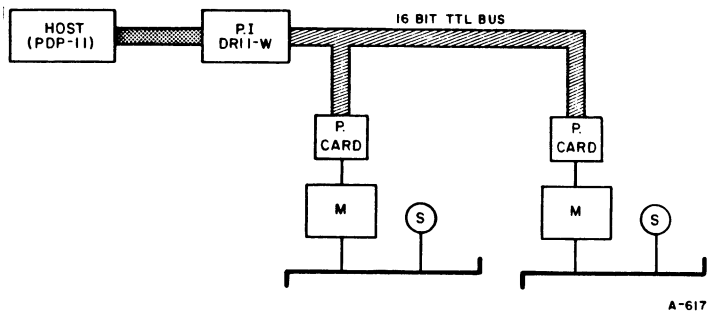

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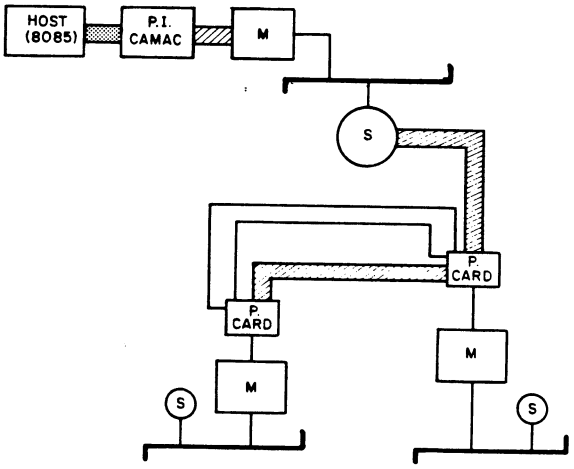

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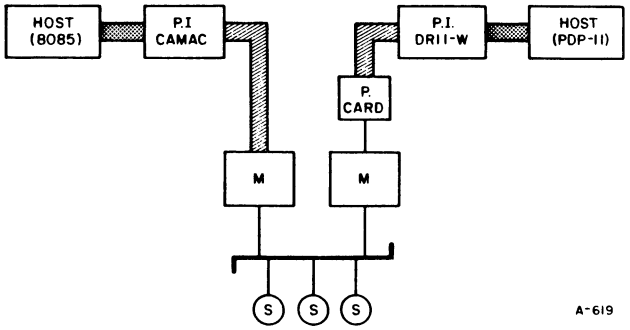

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Figure 1
FASTBUS Architectures Implemented at LeCroy

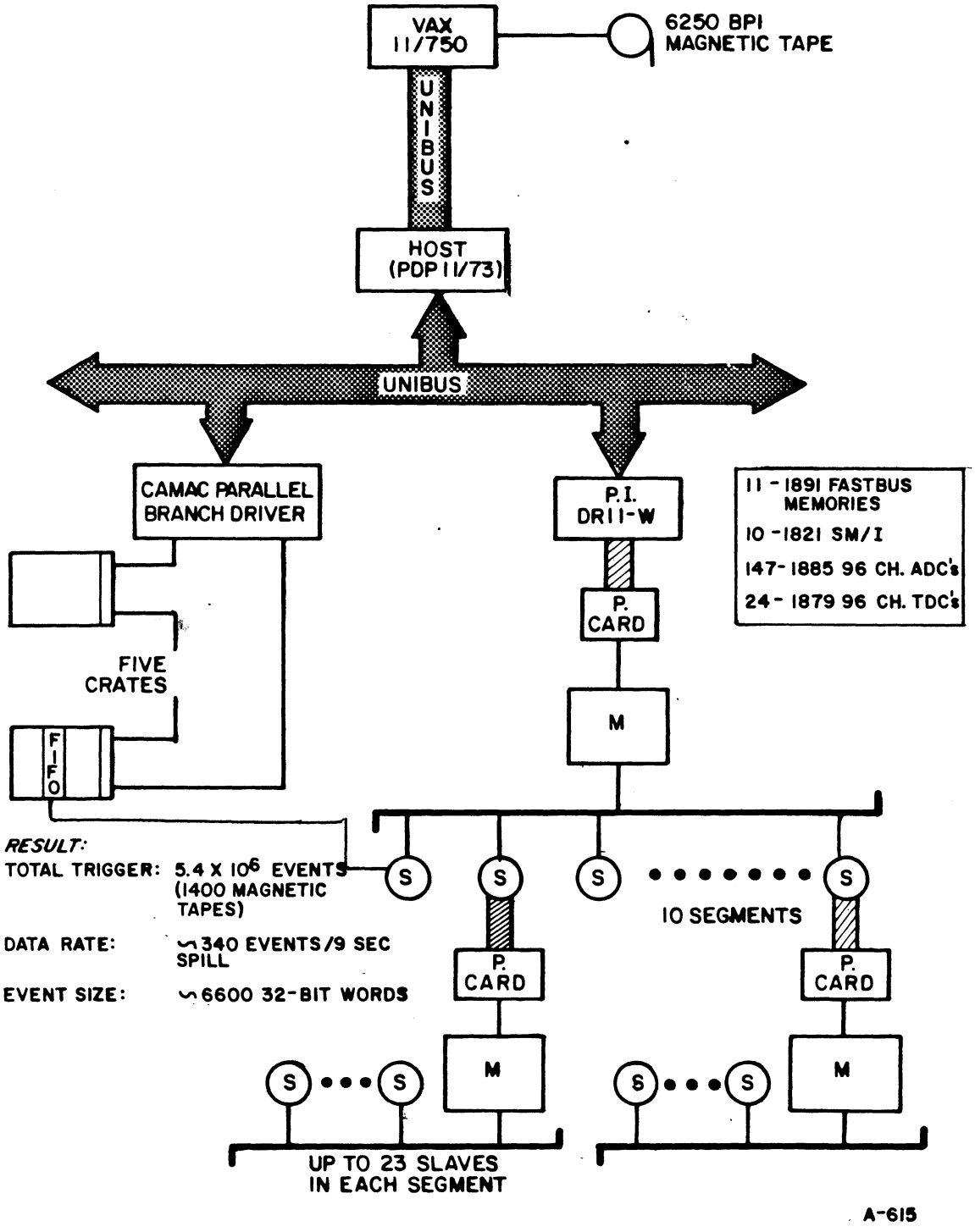

Figure 2
FASTBUS Architectures Implemented by Experiment 653 at Fermilab

1821 SM/I Hardware

The 1821 SM/I has been described as a previous paper[1]. However, a short description may provide insight into the software implementation. The 1821 SM/I is a double width FASTBUS module consisting of two boards, the 1821-1 and the 1821-2.

The 1821-1 provides the FASTBUS interface and control. It consists of a high speed ECL sequencer capable of fetching and executing over 30 million instructions per second. The sequencer micro-instruction word is 64 bits wide and its instruction memory is 256 words deep. Each word is divided into 8 nearly independent fields, each capable of a micro-operation. Because of its high speed and the width of the instruction word, the sequencer can execute over 100 million operations per second in certain applications. Figure 3 shows on the following page a block diagram of the sequencer.

The second board, the 1821-2, provides the HOST interface system. It consists of 8 I/O registers, sequencer program memories (PROM and RAM), a 4K X 32-bit data memory, a 8K 10-bit pedestal memory, and the pedestal subtraction hardware. It allows the user to bypass the on-board memory and route data directly to the HOST, or indirectly to the HOST via DMA transfer from the on-board data memory.

1821 Instruction Word

The sequencer instruction word is 64 bits wide. It is divided into 8 fields, 7 that are currently used, and the 8th field which is reserved for future hardware upgrades. Table 1 describes the fields.

Table 1

OP-CODE	Defines the instruction to be executed. There are 11 instructions currently defined.
CONDITION CODE MULTIPLEXER	Defines the Condition Code to be tested.
BUS DEFINITION	Defines HSDATA and IAD Bus sources.
HSDATA	Is an 8-bit data field that can be loaded onto the HSDATA Bus.
STROBES	Defines the strobes that latch or set different conditions within the Sequencer.
DATA CONTROL	Defines the mode of the 32-bit Register (either BYTE or WORD), whether data is piped to other subsystems.
FASTBUS PROTOCOL	Defines the FASTBUS lines to be SET/RESET, and the mode (SLAVE or MASTER).

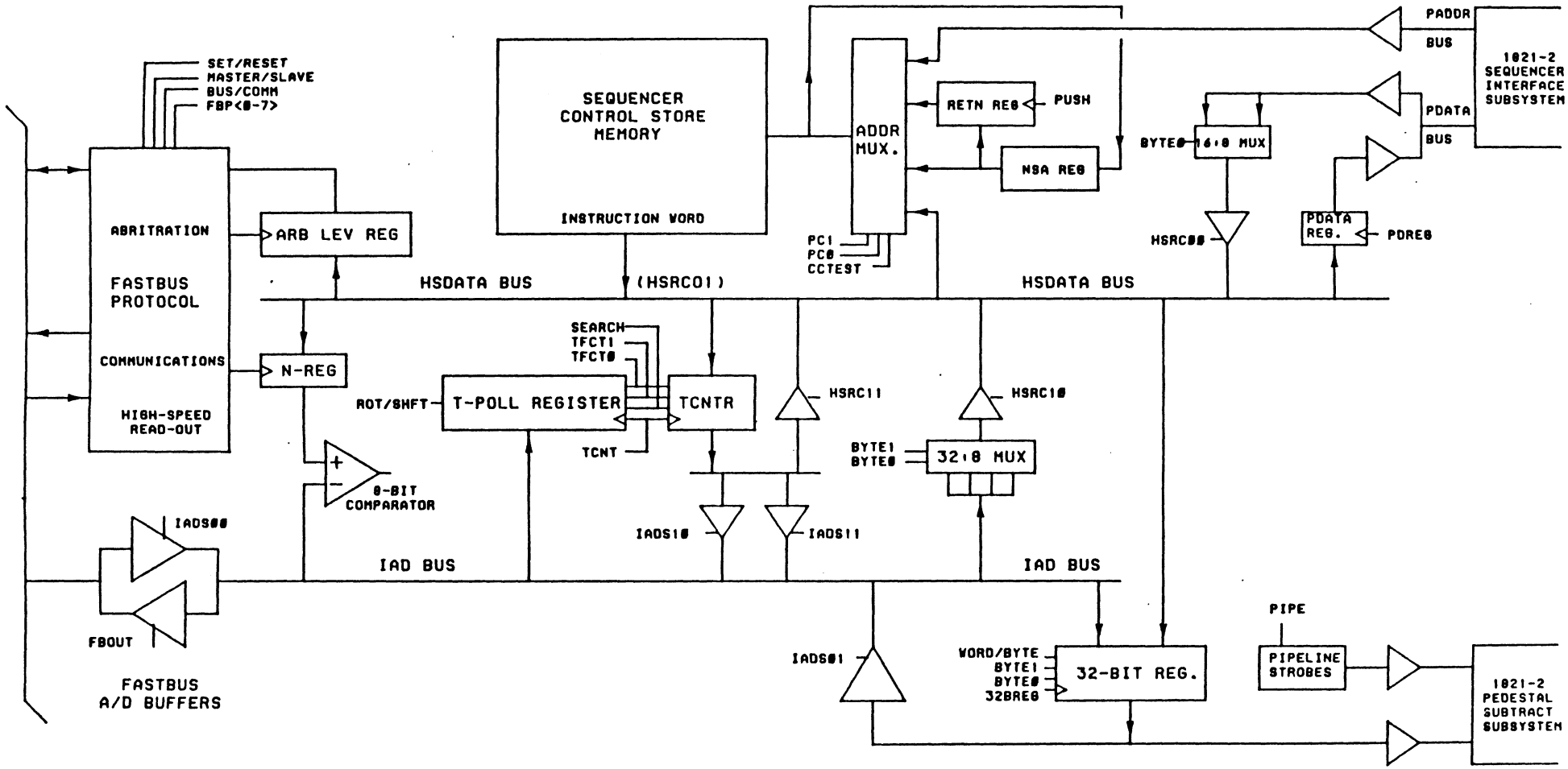

Figure 3
Block Diagram of the Sequencer on the 1821-1 Board

Because of the bit slice design of the sequencer, operations within each field are executed simultaneously. The sequencer instruction set consists of 11 instructions. Although small, it does provide the user with the ability to execute all standard and non-standard FASTBUS protocol. Of the 11 instructions, only 6 have been used in the firmware that will be described in this paper. Table 2 describes the instructions and their functions.

Table 2

Instruction	Use
START (STRT)	Fetch address on INITIAL WORD ADDRESS lines (IWA).
RETURN (RET)	Fetch address in RETURN ADDRESS REGISTER (RAR).
NEXT (NXT)	Fetch address in NEXT SEQUENTIAL ADDRESS REGISTER (NSAR).
JUMP (JMP)	Fetch address on HSDATA Bus.
CJMP	Fetch address on HSDATA Bus if CC bit is TRUE, otherwise fetch address in NSAR.
CALL	Fetch address on HSDATA Bus and latch NSAR address into RAR.
CCAL	Fetch address on HSDATA BUS if CC bit is TRUE, otherwise fetch address in NSAR.
NOTE: The following OP-CODES are of limited use.	
NCAL	Fetch address in NSAR, and latch it into RAR.
NRET	Fetch address in RAR, and latch NSAR into RAR.
LSTR	Fetch IWA address, and latch NSAR into RAR.
CRET	Fetch address in RAR if CC bit is TRUE, otherwise fetch IWA address.

A useful feature of the micro-instruction word is the ability to dynamically test the state of over 170 unique conditions, including all FASTBUS Master, Slave and bus management signals. Other conditions which may be tested include internal timers, Host interface lines, Personality Card signals, and 8 user defined conditions. The appropriate test condition must be selected with the condition code multiplexer on the preceding micro-instruction. The user may then use the CJMP micro-instruction to branch to the address specified on the HSDATA bus if the Condition Code (CC) is true.

The High Speed Data bus (HSDATA) can be driven by internal 1821 registers, the instruction word, or FASTBUS depending on the state of the bus definition field. Similarly the Internal Address bus (IAD) can be driven by internal 1821 registers or FASTBUS. When the HSDATA bus is driven by instruction word, the data is derived from the HSDATA field immediately following the bus definition field.

The 8-bit strobe field allows the user to control the function of the TCNT/TPOLL register, reset internal timers, load the PDREG or load the 32-bit register. The data control field

allows selection of the operational modes of the 32-bit register (either byte or word). It also provides control of the sequencer pipeline.

The FASTBUS PROTOCOL field allows the user to set or clear FASTBUS signals. Different signals are set or cleared depending on the mode (MASTER or SLAVE).

High Level Language Implementation

A group of primitives has been written in micro-code that allow the user to perform all but the most complicated operations. Table 3 lists all the primitives that have been implemented. These micro-codes routines conform to the FASTBUS software specificiation[2]. All of the routines can be executed via the HOST, while some can be called from within a micro-coded program executed via the HOST.

Table 3

FPAC/FPAD	Primary address cycle - control/data space
FPACM/FPADM	Broadcast address cycle - control/data space
FPWNTA/FPRNTA	Secondary address cycle - write/read
FPW/FPR	Data cycle - write/read
FBARB	Set arbitration level
FBREQ	Initiate arbitration cycle for bus mastership
FPREL	Release bus mastership
FPRBUS	Pulse RB signal line
FPRBL	Read a block of data from an addressed slave

Table 4 lists a group of micro-code routines that have been specifically implemented for LeCroy data acquisition modules, but are generally applicable to any slaves.

Table 4

TPSCAN	Initiate a T-Pin scan of the segment
TPINRD	Initiate a broadcast (type specified by the HOST), scans the Segment, and readout all slaves that have asserted their T-Pin.
HDRBL	Uses a special hardware feature of the 1821 to readout a slave at a higher speed than the normal FASTBUS block transfer - FPRBL
READTDC	Read only a specified channel of a TDC until SS=2.

The micro-coded routines described in the previous tables are currently called by FORTRAN routines with the same name. The FORTRAN routines are responsible for downloading parameters to or unloading parameters from the 1821. The procedure for doing this is simple and straightforward. The source of the PDATA bus must be selected by writing the appropriate data in Register 0. If data is to be passed to the sequencer, then the appropriate data must be loaded in Register 2. Once this has been accomplished, the micro-code must be executed. Figure 4 shows the procedure for executing the micro-code.

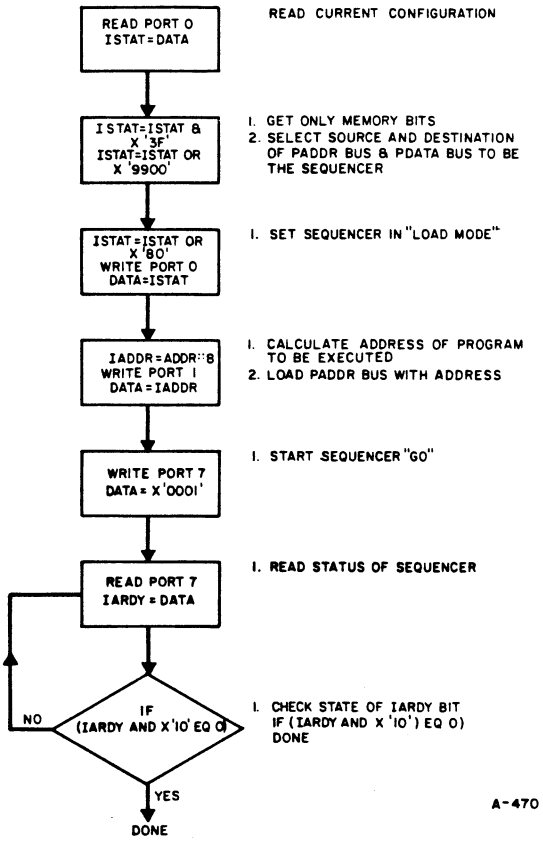

Figure 4
Block Diagram of Subroutine EXEC21

As one can see, in order to execute the different micro-coded routines, the user need only modify the value written to Register 1, the PADDR bus.

The standard PROM 0 Version 6 Update 3 has been implemented with a transfer address table. This allows modifications within the micro-coded routines without any modifications to the user source code. Preprogrammed timeouts along with a subset of the standard FASTBUS error codes have also been implemented. In most cases, it is expected that PROM 0 will provide the user with all the firmware necessary to communicate with a FASTBUS Segment.

For the more experienced user, a cross assembler is available[3]. Figure 5 shows a subroutine written in the source code for the cross assembler. The cross assembler is written in FORTRAN and adaptable to almost any HOST. The implementation referenced throughout this paper is for a DEC PDP-11/34A. A definition file, source listing of the standard PROM 0, flowcharts and runtime documentation will be provided to any interested user.

```
ARBIT; Arbitrate for FASTBUS Mastership

;This routine will cause the 1821 to raise its AGK line. This will cause the hardware to
;arbitrate for mastership of the FASTBUS.  The routine will wait for a GK response
;signifying a successful request.  If no GK is returned from the arbitration hardware the
;route will time out and return to the idle loop with an error code=20 decimal in
;the PDREG.

ARBIT:    NOP D #20 & CLKPD & SETAGK     ;Initialize PDREG and start
                                         ;arbitration
          NOP 0 & TIMER & IFT IGK        ;Reset timer. test: GK=1?
ARLOOP:   CJMP ARWON & IFF T4096         ;If GK=1. won arbitration.
                                         ;Also.  test:  timeout?
          CJMP ARLOOP & IFT IGK          ;If no timeout, loop back
                                         ;and test:  GK=1?
ARLOST:   JMP IDLE & CLRAGK              ;Timed out.  clear AGK and go
                                         ;back to idle loop
ARWON:    JMP IDLE & CLKPD & CLRAGK      ;Won arbitration.  clear PDREG
                                         ;and go back to idle loop
```

Figure 5
Source Code for META29M Cross Assembler

The 1821 SM/I has been interfaced to CAMAC via the LeCroy Model 2891 and to the DEC UNIBUS™ via the DR11W and the 1821/DEC. DMA transfers of up to 4 Megabytes/sec have been measured when the DR11W has been configured for N-cycle burst mode. The software driver for the DR11W is available upon request. DR11W compatible interfaces are also available commercially from other manufacturers[4].

Interfacing to bus structures and other LeCroy modules is accomplished by specific Personality Cards. Table 5 shows the LeCroy Personality Cards that are currently available or will be available in the near future.

Table 5

Personality Card	Bus/Module	Status
1821/DEC	UNIBUS™	Available
1821/ECL	LeCroy 1892 Memory	Available
1821/QBUS	QBUS™	Near Future
1821/VME	VME/VMX	Near Future

These Personality Cards have been used to implement the architectures shown in Figure 1. A FASTBUS to VME Interface for the Model 1821 SM/I has been designed and built by Harvard for UA1. It will be presented at this conference.

For debugging user written micro-code, the 1821/MON is also available. The 1821/MON Monitor Accessory allows the user of the 1821 SM/I to monitor execution of 1821 micro-code with single-step and halt-on-address capability. The monitor also allows the user to change the clock frequency of the 1821, and displays the address and state of the HSDATA Bus when the 1821 is halted. The simple control panel and small size of the 1821/MON make it an invaluable aid to programming and interfacing the 1821 SM/I. This provides the user with the ability to:

1. Display the micro-code
2. Single step micro-coded routines
3. Stop execution at a predefined address

Current Status - FASTBUS Data Rates and Architectures

As can be seen from Figure 1, many different architectures have been implemented and tested. Table 6 displays some measured Master/Slave data rates obtained with LeCroy FASTBUS modules.

Table 6
(All transfers are 32-bit words)

Master	Slave	Rate	Mode
1821	96-Channel TDC	9 MHz	Block
1821	96-Channel TDC	5 MHz	Random
1821	96-Channel ADC	7 MHz	Random
1821	1 Megabyte Memory	1.3 MHz (5.2 MHz)*	Block

*Predicted data rate using Texas Instruments ALS232 FIFO not yet available.

NOTE: The preceding rates do not include the digitization times or the time required to establish the AS-AK lock.

Of the FASTBUS architectures that have been implemented, the architectures depicted by Figures 1A and 1C are used routinely at LeCroy for the production testing of the 1800 Series FASTBUS modules. The architecture depicted in Figure 1A employs the standard PROM 0, while the architecture depicted in 1C employs firmware that is still under development. This firmware allows the Master in the primary Segment to communicate via the Slave (LeCroy 1892 Memory) with a maximum of 16 secondary Segments.

The architectures depicted in Figures 1B and 1D have only been used to demonstrate that the architectures are feasible. No serious measurements have been made. DMA's were tested from each Segment shown in Figure 1B and bus arbitration between different Hosts was tested as shown in Figure 1D. Both architectures employed PROM 0.

Figure 2 depicts the FASTBUS architecture that has been employed by Experiment 653 at Fermi National Accelerator Laboratory[5]. The system consisted of 11 FASTBUS Segments, 1 primary Segment containing 11 LeCroy 1891[6] FASTBUS memories, and 10 secondary Segments each containing a LeCroy 1821 SM/I, a LeCroy 1810 CAT, and varying numbers of LeCroy 1885 ADC's and 1879 TDC's. The experiment took data this summer. The results are shown on the figure.

The experimenters used the standard PROM 0 as a basis for implementing their own micro-code. They were also responsible for the first implementation of the Microtec cross assembler.

Conclusion

The 1821 SM/I is possibly the most versatile and highest speed Host interface available commercially today. The programmability of the 1821 SM/I allows the user to communicate with any Slave using FASTBUS standard software, with the ability to support non-standard protocol. The variety of commercially available Personality Cards provides the user with direct connection to CAMAC, UNIBUS, VME, or any computer that supports a parallel I/O interface. Thus, the 1821 SM/I bridges the gap between today's high speed data acquisition modules and existing control and acquisition systems.

Acknowledgements

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References

1. W. Farr, L. B. Levit, R. Roush, "A FASTBUS Segment Manager and Interface Unit", IEEE Trans. Nuc. Sci., NS-31 (1984)

2. "Specifications for Standard Routines for FASTBUS", FASTBUS Software Working Group, FSDG085

3. Microtec™ META29M, Microtec Research Inc. P.O.Box 60337, Sunnyvale, CA 90488

4. The XT-170 Peacemaker is a high speed bi-directional interface that fits into any full size slot on an IBM PC/XT. It permits DMA transfers between the PC and any DR11W compatible peripherals. It is available from IGC, Inc., 1290 Motor Parkway, Hauppauge, NY 11788, (516) 582-8828

   The SAIVME-DR11W VME bus to DR11W Interface provides bi-directional transfers between VME bus and any DR11W compatible peripherals. It is available from Science Applications International Corporation, 2109 W. Clinton Avenue, Huntsville, AL 35805, (205) 533-5900

   In principle, both of these devices should provide an interface between the 1821 SM/I using the 1821/DEC Personality Card and their respective buses. Since we have not had a chance to test these devices at LeCroy, we can assume no responsibility for their operation.

5. "Measuring Charm and B Decays Via Hadronic Production in a Hybrid Emulsion Spectrometer", E-653, FERMILAB, J. Dunlea, A. Gauthier, J. Kalen, S. Kuramata, G. Oleynik, N. Reay, K. Reibel, R. Sidwell, N. Stanton, THE OHIO STATE UNIVERSITY; AICHI UNIVERSITY, UNIVERSITY OF CALIFORNIA AT DAVIS, CARNGIA-MELLON UNIVERSITY, FERMILAB, KOBE UNIVERSITY, NAGOYA UNIVERSITY OKAYAMA UNIVERSITY, OSAKA CITY UNIVERSITY, UNIVERSITY OF OKLAHOMA, SCIENCE INSTITUE OF OSAKA PREFECTURTE, UNIVERSITY OF KOREA, UNIVERSITY OF OTTAWA, YOKOHAMA NATIONAL UNIVERSITY

6. The 1891 FASTBUS Memory has been discontinued. Its replacement is the 1892 FASTBUS Memory.