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WORK AT NIKHEF-H ON FASTBUS

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Abstract:

This paper summarizes the present and future activities on FASTBUS at NIKHEF.
Since in this workshop 'well-known' hardware modules will already be treated and a review will be given on FASTBUS routines, emphasis will be given on the FASTBUS modules developed at NIKHEF and the software implemented or to be implemented for those modules.
A description will be given of the hardware and software test environment for FASTBUS modules.
Finally a description of the activities concerning the L3 and DELPHI experiments will be given.

Test environment

NIKHEF has two VMEbus test systems from Compcontrol BV with the following hardware configuration:

- 8 MHz 68000 CPU, 16 Kbyte on-board RAM, occupying one slot;
- 2 × 512 Kbyte memory, occupying two slots;
- 1 floppy disk/SASI interface, occupying one slot;
- 1 8-inch double-sided floppy disk drive;
- 1 20-Mbyte Winchester disk;
- 20 slots VME crate.

The Operating System is CP/M 68K. An assembler and C is supported. We installed RTF68K (1), as a native compiler.

The VMEbus test systems are connected via a serial link to our network of APOLLO workstations.

On the APOLLO workstations all CERN cross-software has been installed, including pushers and linkers, except for the cross FORTRAN compiler, which will be installed as soon as the CERN version, written in PASCAL, is available.

On the VMEbus based testsystems version 2.0 of the PILS (2) interpreter has been installed. The compiler version will be installed later.

Some remarks concerning the system dependent PILS - Host interface:

- Terminal I/O is made via MoniCa (a RAM version of MoniCa is linked with PILS);
- Disk I/O makes use of the TRAP 2 calls of the BDOS (the Basic Disk Operating System of CP/M 68K);
- The external interfaces to FORTRAN libraries, like FASTBUS, HMINI, MINIGD3, are compiled on another host, from which the CUFOM output is sent by a terminal line to the APOLLO's, to be linked to PILS.

Concerning FASTBUS equipment we have:

•1 FB crate	STR 103
•1 FB monitor module	STR 160
•1 FB module FIORI	STR 164
•1 VME - FB interface complete (FB module CFI + VME dual I/O register VFIVC)	STR 300/302
•1 FB diagnostic module FDM	STR 161
•2 FB active extenders	STR 178
•1 FB kluge card	STR 144
•1 FB kluge card	STR 159
•4 TDC's	LRS 1879
•1 Calibration and Timer module	LRS 1810
•1 Segment/manager interface	LRS 1821

So we are able to test the whole chain of CERN cross-software and can use part of the FB routines (3), by implementing a modified version of FBMON, an interactive Fastbus testprogram (4), or FDMTST(5).

Present FASTBUS activities

As NIKHEF is responsible for the readout of trigger data of the muon chambers of L3, a project has been started to construct a muon-trigger interface (fig. 1). The muon trigger interface feeds the first and second level trigger. The data transferred by the interface contains 'hit-cells' only. A cell in the muon detector is defined by a group of 24 wires for the middle muon chambers and 16 wires for the inner and outer chambers (we only treat here "p-measurements", though we also make an interface for the "z-chambers").

Number of electronic channels:

... Chamber ...	... z-wires ...	... p-wires ...
MO (outer layer)	3,456	5,536
MM (middle layer)	-	6,000
MI (inner layer)	3,520	3,672
---Total---:	6,976	14,208

Twelve FB crates are needed for the total read-out of the muon chambers.

The interface consists of three parts:

1) - The PC

The Personality Card is connected to the TDC via its auxiliary connector and the FB auxiliary backplane.
Its function is to collect hit information of the wires during drifttime. It logically OR-s the information of two adjacent wires, and sets a memory when one of them is hit.
There are 48 of these memories on one PC.

2) - The PCC

The Personality Card Controller, is a FASTBUS module located in the same crate as the TDC's, that deliver their hit information to it via the PC's. One PCC can handle all PC's of one crate.
Its function is to read the PC's in the proper sequence, gather the data of each cell and compare the data with the threshold (number of hit wire pairs) set for that cell.
It then sends its data to the "hit array" of the first level trigger and to the Multi Port Multi Event Buffer of the second level trigger.

3) - The MTC

The Muon Trigger Controller might be a VME module. Its function is to distribute signals such as:
'start read-out' and 'reset' PC's to all PCC's.

Furthermore there is the PC bus.
The PC bus is a flat cable, connecting all the PC's in one crate to the PCC.
It consists roughly of three parts:
The data bus (48 bits).
The control bus, which contains signals to control the PC's during data taking.
A daisy chain, to control the read-out sequence of the PC's.

A prototype of the PC is now available and will be used in the test set-up.

As the PCC is not yet designed, a 'PCT' (Personality Card Test Module) is under construction. The PCT simulates roughly a PCC, and a TDC. The PCT must send commands to the PC's and read data back via the PC bus.

In a further stage one has to do with the grouping of cells over the TDC's. They must be stored in RAM space of the PCC.

The order of read-out of the PC's by the PCC is a daisy chain type. The PC's are read in the sequence of their physical location.

Foreseen is in test possibilities, like writing six times 8-bit datawords into the PC hit-memories and then reading them back.

External control must be implemented, for example:
as input to the PCC:
enable collect, start encode, clear hit memory, stop encoding, and as output from the PCC:
encode busy, FASTBUS busy, start error, PC error.
For a more detailed description, see reference 6.

Future FASTBUS activities

A small prototype of the middle layer of the muon chambers, for momentum measurement, has been constructed (fig. 2). It consists of 5 × 24 wires, from which at least in the beginning, 24 will be connected via a pre-amplifier and a discriminator to a few TDC's.
These TDC's will be read out by the 1821 LRS segment/manager interface.

Only programs for the read-out of the TDC's are foreseen at the moment - just to test the prototype in the magnet field in the test bundle at CERN next year.

Later on data has to go, via an ECLine and an LRS 1891 memory on the sub-detector crate to the event builder, a combination of the General Purpose Master and the Block Mover (7).

The inner detector of DELPHI is under construction at NIKHEF (8).

The vertex chamber has 24 sections of 24 wires on which accurate drift-times need to be measured. A number of 576 channels has to be read out by LTD's.
The number of channels of the outer trigger part is substantially higher - 5×160 anode wires and 5×200 cathode strips. The wires and strips will be treated in the same way: a pre-amplifier with limited band width sends the data to a 7(8)-bit FADC.
So 1,800 channels amplitude measurement by FADC's is necessary. As discussions on the design of the LTD's and FADC's are still going on, it is difficult to give a detailed read-out scheme. Also the third-level trigger is not 'fixed'. It is clear that at the moment we are in the design phase, but we hope to start hard- and software activities on FASTBUS within 1 year.

Conclusions

A test environment for FASTBUS has been created. CERN FB routines have been implemented. The writing of test programs will start this year. In the beginning they will not be too complicated, due to the fact that part of the hardware is still in the design phase. Concerning the read-out, discussions are still going on, and one is still in the stage of proposals.

Figure Captions

(1) - The L3 Muon Trigger Interface.

(2) - The prototype of a middle-layer muon chamber.

REFERENCES

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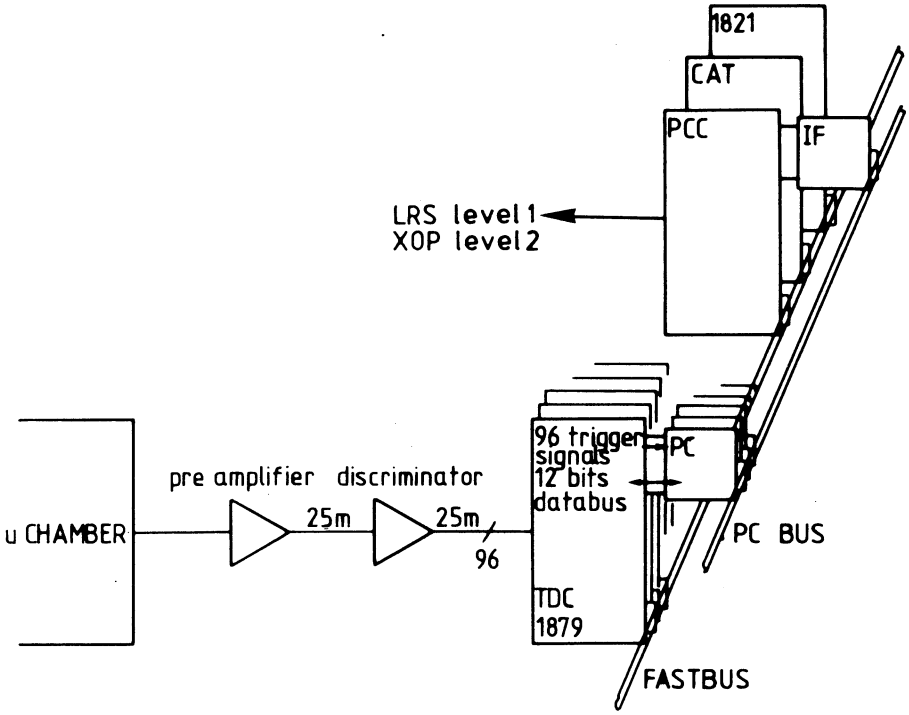
1821
CAT
PCC
IF
LRS level1
XOP level2
96 trigger signals
12 bits databus
PC
PC BUS
u CHAMBER
pre amplifier
discriminator
25m
25m
96
TDC 1879
FASTBUS

FIG. 1

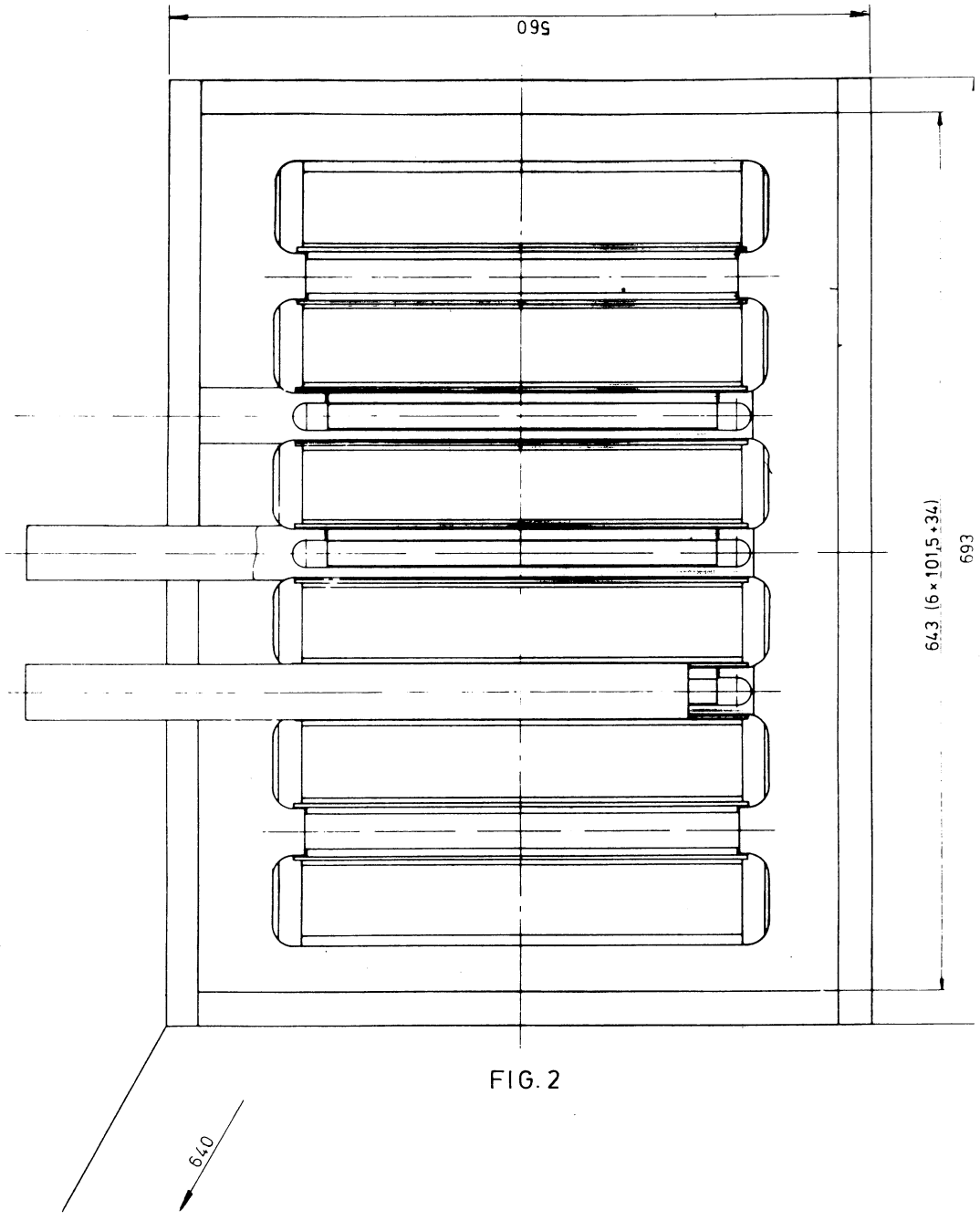

FIG. 2