Results of a Sliced System Test for the ATLAS End-cap Muon Level-1 Trigger

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Abstract

The sliced system of the ATLAS end-cap muon level 1 trigger consists of about 500 inputs. It completes almost entire functionalities required for the final system. The six prototype custom chips (ASICs) with the full specification are implemented in the system. The structure and partitioning are also conformed to the final design. With this sliced system, we have made validity check of the design, performance and long run tests for both the trigger and readout parts in detail. We report the outline of the sliced system along with the final design concept, and present results of the system test and discuss possible improvements for the final system.

I. INTRODUCTION

After submitting the ATLAS trigger design report for the level 1 muon end-cap system [1], we have concentrated to develop the custom ICs to be used for the system. Recently we have nearly completed the prototype ASIC fabrications. We will use seven ASICs and six prototypes have been ready. Before moving into the final phase of the IC production, we have built a sliced system using the developed ASICs in order to investigate the design validity and performance of the final system.

The Sliced system consists of all the components for the TGC (Thin Gap Chamber) electronics system from very input part that receives the chamber hit signals to the last logic part to supply trigger candidate signals for muon central trigger processor interface (MUCTPI), which generates the final level 1 trigger with muons detected in ATLAS.

In order to perform the slice test, we have developed independently a C++ based trigger simulation code. The code has been constructed to imitate the hardware system as much as possible; a logic of an ASIC is implemented as a method with the similar way for input/output signal handling in the simulation code. The simulation results are used to verify the validity of actual logics put in the ASICs, and to evaluate overall the sliced system itself. Thus if we find some discrepancy of results between the simulation and the test setup, we can spot immediately the source in the system, which gives inconsistency.

The first integration test of the full chain slice test (SLT) has been started at KEK in September, 2001, in which only one coordinate (r) of total two (r and φ) signal processing has been done while both two signals processing with r-φ coincidence check has been performed in SLT in 2002. The software framework that controls the hardware initialization and run control has been also changed from SLT2001 to SLT2002, though the detailed discussion of the software will be found in the other presentation in this workshop [2].

In this report, we discuss overall TGC electronics system in the next section. We, then, discuss in detail the SLT setup, components (modules and ASICs) used in 2001 and 2002 tests in section III. The test results are presented in section IV, and we summarize the results in section V.

II. TGC SYSTEM OVERVIEW

Figure 1 shows an overview of the TGC electronics system [3], which consists of number of identical branches (as a unit of 12 (eight endcap and four forward sectors) plus one (inner small TGC)) for each trigger segment, which

covers one sixths of one side. Electronics components for a segment are mounted on two parts; on-detector and off-detector (USA15) parts. The on-detector part is further separated into two parts, one is called PS board that is installed just behind the detector, and the other one is HS crate that is installed at the outer rim of an endcap chamber.

Digitized signals from Amplifier- Shaper- Discriminator (ASD) boards [4] attached directly to TGCs are inputted to Slave Board (SLB) ASICs (SLB IC) after synchronized and bunch crossing identified in Patch Panel (PP) ASICs (PP IC). SLB performs local coincidence to identify muon tracks

coming from the interaction point with $p_T \geq 6$ GeV/c, and output information of r, ϕ and Δr, $\Delta\phi$ for every muon candidate. The PP and SLB ICs are mounted on a single board called PS board. The output signals of SLB are fed into a High pT board, which is installed in an HS crate and is approximately 15m apart from the corresponding PS board. The HpT board contains HpT ASICs (HpT IC). An HpT IC combined information from several SLBs to make a global coincidence to find muon tracks with $p_T \geq 20$ GeV/c. HpT IC also makes data compaction to send its output over about 90m distance with serial data transmission.

Figure 1: Schematic view of ATLAS endcap muon level 1(TGC) electronics system

Signals for r (wire hit information of TGC) and ones for ϕ (strip) are separately processed in the different streams up to high p_T coincidence operation, and the sector logic (SL) installed in the off-depart combines these two streams and makes a coincidence in r-ϕ to identify muon signals in three dimensional space. Two highest p_T muon candidates per trigger sector (72 sectors/side) are selected after successful r-ϕ coincidence, and the information is sent to the MUCTPI. Functionalities and performance of the three ASICs (PP, SLB and HpT) has been discussed in detail in ref. 5.

Since hit information for both coordinates will be used not only for the trigger decision logic but also used as the second coordinate information for the ATLAS muon reconstruction in offline analyses, a readout system must be implemented. Readout data are processed in SLB ICs, each of which implements L1 buffer and de-randomizer, and at every L1A signals, data are serialized in SLB ICs and are sent to a data distributor/ concentrator, which is so called Star Switch (SSW). Basic concepts and functionalities of SSW

will be found in ref. 6.

ROD receives readout data through the G-link for one trigger segment unit (13 inputs), buffers in FIFOs, which are prepared for every input and builds up as an event fragment for every bunch crossing identification, and sends them to ROB, which is already in the ATLAS DAQ realm. The data gathering from 13 input FIFOs and TTCrx to form one fragment needs an on board microprocessor. ROD used in the present SLT implements 32bit RISC chip of Hitachi SH4. This chip is used for arbitration of an internal bus connected with it and input and output FIFOs.

Both a PS board and an HS crate as a part of an on-detector part are installed in radiation critical region so that modules (PS board, HpT and SSW boards) will suffer from single event upsets. We could anticipate the radiation levels of 2.11×10^{10}h/cm^2/10yr and 1.42×10^{10}h/cm^2/10yr in a PS board and an HS crate respectively. Since every module mounts a few FPGAs or CPLDs and ASICs, we have to monitor such the occurrence always during experiment, and

restore correct bitmap data as soon as possible if an SEE is detected in a chip. HSC and CCI have been introduced for this purpose. A pair of HSC and CCI makes one single operation of HS crate control. CCI is put in a crate in the counting room (USA15). Its counterpart HSC module is a remote crate controller at HS crate so that CCI can control an

HS crate as if this is own crate. A CCI always monitors the partner HSC. If the HSC reports an SEU in its controlled electronics modules, the CCI can send data with JTAG protocol over G-link embedded optical link in order to restore FPGA or ASIC configuration promptly [7].
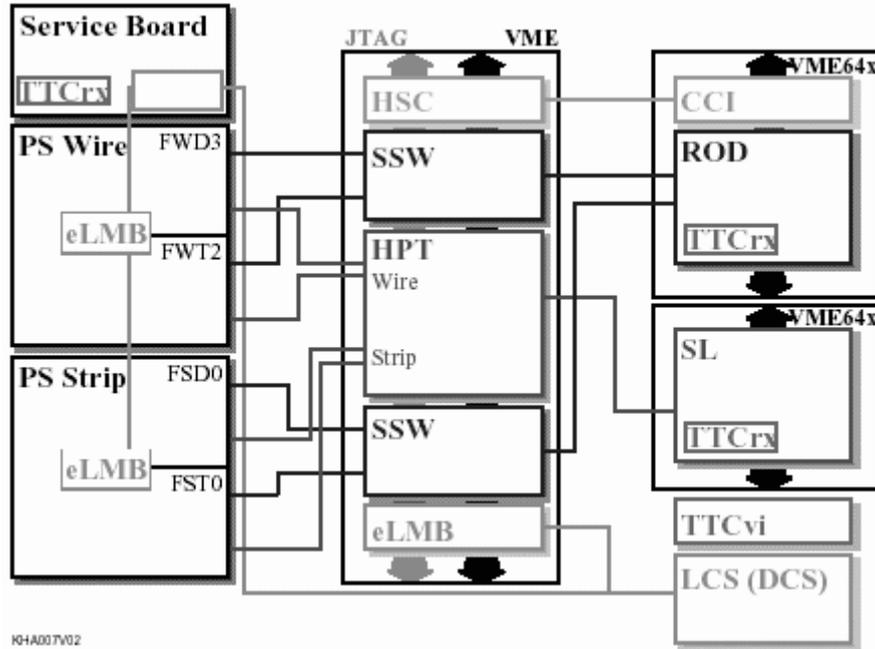
Figure 2: modules and connection diagram for Slice test setup

III. TEST SETUP

The scale of the present SLT setup corresponds to a one quarter of the forward sector of one octant, which has three forward sectors. Numbers of channels used for wire and strip are 256 and 192, respectively.

Final design version has been applied to all the electronics modules used in SLT except PS boards. We have produced PS boards for both wire and strip temporarily dedicated for SLT. Except PS boards, all other boards are implemented in VME bus modules.

Overall connection diagram of SLT is shown in Fig. 2. As actual TGC system, the SLT system is also separated into three sections. The middle and last columns in the figure are installed in two independent VME crates while the components in the first column, which are service board (Service Patch Panel; SPP) and PS boards, are put isolated on a desk and are powered independently. Pulse pattern generators (PPG) and interrupt register module (INT) (both are VME modules) are used to emulate the ASD output signals. We can program the signal inputs for PPGs. Programming the same input signal patterns as one used in the simulation, we can make output comparisons directly and immediately. INT is used to synchronize the output timing of number of PPGs. PPGs and INT are installed in further different VME crate. Hence we have used at least three VME crates in the SLT setup.

Every VME crate has own independent PC running Linux

system. PC is neither in a form of VME module nor mezzanine board to be installed on a VME module. We use BIT3 PCI/VME interface module for the VME-PC connection throughout.

We have at least three PCs in the system. We need only one (Root PC) for the integrated SLT, which controls the initialization for modules, and data taking management. We have implemented CORBA based VME access system in order to access VME modules installed in a crate, which is not connected directly to the Root PC. With this CORBA system, one can access any VME modules from any PC. Hence any PC can be a Root PC for SLT. We have used two different software frameworks for SLT2001 and 2002. This system with CORBA has been made by us ourselves, and used extensively in SLT2001 as a part of its software framework.

In SLT2002, we have made another software system on top of the ATLAS online software framework [8]. As distributed nature of the system is more emphasized in this software system, each PC simply access modules installed in directly connected crate, which the PC connects via BIT3 interface. The configuration database used in this framework keeps the relationship information of modules and a corresponding crate, and its connected PC. A Root PC (the crate controller) can immediately recognize a PC, which can control the module from the database. Thus if the root PC wants to access a particular module, it asks to the corresponding PC to access via information server embedded in the run control system of the ATLAS online software

system. The detailed discussion of the software frameworks for SLT is done in ref. 9.

IV.   TEST RESULTS

A   Trigger Part

We have done the trigger part verification in the SLT system by inputting hit patterns (commonly used for the simulation input) and comparing the output with the one of the simulation. In the simulation, we have set the muon p_T momentum infinite throughout two SLTs. The modules checked in this trigger test are

1. PS board, dedicated for SLT, two ASICs on board, PP IC, Rohm 0.6μm full custom, and SLB IC, Rohm 0.35μm full custom,

2. HpT board, a 9U VME board with full specification for forward sectors, and full specification HpT IC on board processed with Hitachi 0.35μm Gate array, and

3. SL board, a 9U VME64 extension board with full specification for forward sectors.

The data links between modules are

1. LVDS 7m between PS board output and HpT board, actually, 15m cables will be used in the ATLAS experiment, and

2. G-link 10m with optical fiber between HpT and SL, 90m optical data transmission is foreseen in the ATLAS.

We have inputted hit patterns generated by VME PPG modules 40.08MHz external trigger rate, and found no discrepancy of output comparison with patterns of one-, two-, and ≥3 hits cases. We have found no mal functioning in the long-term stability test under normal 40MH trigger condition. Since we have tested only trigger processing test using only r coordinate information, we have not tested at all SL in SLT2001. In SL2002, as we have introduced the φ-trigger, we could examine the r-φ coincidence performance without SL. SL is still under-construction.

Latencies measured in the components are listed in Table 1. Total latency can be calculated with measured values listed in this table together with the cable delay estimation and ones consumed in the detector and central trigger processing [1]. The latency up to MUCTPI (namely without the central trigger processing time) is estimated as 1.2μs, and one to individual front-end electronics of sub-detector parts is estimated as 2μs. These values are well cleared our upper value constraint of 1.25 and 2.05μs.

Table 1: Latency measurements

Component	Measured Delay (ns)	Estimated Delay in BC (TDR)
PP IC	47	2
SLB IC	49	3
HPT	33	3
SL	161	7
Sub Total	290	15

Estimated Latency	Latency measured (ns)	Latency estimated in TDR (ns)
up to MUCTPI	1176	1250
up to Front End	1976	2050

B   Readout Part

In the readout test, we have tested following modules,

1. PS board as one used in the trigger test: readout part (L1 buffer, de-randomizer) of SLB IC on board is tested in the test,

2. SSW: 9U VME board with full specification, general purpose VME module (PT4) has been used instead of SSW in SLT2001, and

3. ROD: VME64 extension board with full specification for one full trigger segment, an on board RISC chip Hitachi SH4 (167 MHz) is used for the data collection, arrangement with bunch crossing identification, reformatting and transfer.

The same input patterns used for the trigger test have been used also in the readout test. In SLT2001, we have generated TTC relevant signals (L1A,BCR and ECR) with a PPG module while we have generated these signals using TTCvx - TTCvi - TTCrx chain in SLT2002. Several necessary application programs and items concerning TTCvi have been added in the software framework and its configuration database [2].

In the test we have verified the correctness of the data transfer from PPG to ROD via SLB and SSW. The data links are LVDS 7m (instead of 15m) from SLB to SSW and G-link from SSW to ROD. We found no problem for data transmission from PPG to ROD. We have verified also functionalities of SSW (FPGA firmware installed in FPGAs on PT4) for data framing and compression from two SLBs, and found no data loss under the operation of L1A rate of 78KHz. The long term test for 10^5 cycles has been done and correctness of data transmission as well as SSW functionalities have been established.

We have developed the boot program and kernel program for SH4 RISC chip. The kernel program reads data stored in total 13 input FIFOs, TTC bunch crossing ID and trigger

word at L1A, and arranges event data in accordance with the bunch crossing ID. Datasets stored in input FIFOs has the header and tailor. The kernel program should remove these words, and extract the relevant information before rearrangement. Then it finally pushes data on readout FIFO, which is connected to ROB input channels via s-link [9]. The bandwidth of the internal bus connected for input and readout FIFOs, SH4 and ancillary RAM, which is used for cache during data reformatting is very critical for event formatting with 100 KHz. We have measured this bandwidth in a standalone benchmark test. The bus access time is measured as 200ns for four bytes (data length of no hit) per one FIFO. Total access time with 13 input FIFOs, two FIFOs for TTC including SH4 software access time and readout FIFO is then estimated as 5μs (200KHz). Since an input FIFO will store data fragmentation of 40byte length if corresponding trigger sector has hit information, it will be hard to keep processing under 100 KHz L1A trigger.

C   Control Part

We have checked functionalities of two modules HSC and CCI in the control system test. Two modules are connected with G-link. With this connection., VME accesses of the HS crate (remote crate) can be done by accessing the CCI module at local side. We have confirmed this accessibility in the test so that we can access the remote HS crate as if this crate is directly connected to the PC in which the CCI crate is connected. One of the main purposes of HSC-CCI crate is to rewrite bitmaps of FPGAs that are installed in the HS crate remotely by accessing CCI via JTAG protocol. In this case we must use specially designed J3 back plane in the HS crate. We have confirmed the JTAG functionalities from CCI to modules in the HS crate via HSC also in this test.

We have tested the access to the ICs mounted on the PS board also. The ICs to read/write their registers on a PS board are PP, SLB and JRC (JTAG Routing Controller). Except SLB IC, we could perform JTAG accesses to the other two chips, namely PP and JRC. As we have small bugs in JTAG accessing control part of SLB, to check the access of SLB IC is the next issues with forthcoming SLB IC. For both JTAG access tests of the ICs on the modules of the HS crate and PS boards, we have made long-term repetition tests. We observed no errors in 10^{10} accesses for ICs on VME modules, and 10^7 for a PP IC on the PS board.

V.   SUMMARY

For two years, we have made the slice tests for the TGC electronics system. We have confirmed the trigger logic validity for both r (wire)- and ϕ (strip)- parts. We have measured latency for the level 1 trigger signal generation. We have found less latency than expected in TDR. Although we need more careful verification, we have confirmed the validity of r-ϕ coincidence in the off-line analysis. This operation should be done in future in SL (Sector Logic module).

The readout part worked fine even in a long run test with the readout rate of 78KHz instead of 100KHz. This measurement is done with only one input FIFO used in ROD. For using full 13 input FIFOs and maintaining 78KHz readout rate or more, we need a little device for increasing the bandwidth of the internal bus in ROD. We introduced in SLT2002 new module SSW in the read-out part instead of its prototype. Based on the results in SLT2002, we have to fix the final design of SSW soon.

We have confirmed its basic functionality for CCI-HSC pair. The JTAG operation has been worked successfully for individual front-end ASICs and FPGAs.

VI.   ACKNOWLEDGEMENTS

VII.   REFERENCES

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