SELF TRIGGERED, SINGLE TURN BEAM POSITION MONITOR FOR ELECTRON STORAGE RINGS*

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Abstract

A VME based single turn beam position monitor has been developed to improve diagnostics for the NSLS UV ring. A monopulse network processes the PUE pulses, generating the sum and difference signals. An analog processing board amplifies, rectifies, and holds the signals. A digital board then digitizes and stores the data. The system can measure 32,000 turns of bipolar PUE signals from button type electrodes (1nS per lobe) at a 170nS repetition rate, with bunches separated by 18.9nS. The system makes useful measurements over a 40dB dynamic range of beam current. At full current the resolution is 50 microns.

1 INTRODUCTION

The ability to measure beam position on a turn by turn basis allows operators to increase the injection efficiency and reduce radiation levels by optimizing the injection process. It also enables the measurement of non-linear beam dynamics through phase space tracking. These measurements are particularly difficult when using the button type pickup electrodes (PUEs) commonly found in light sources. The signals are bipolar with no delay between the two 1nS wide lobes (figure 3 trace A). This makes the direct use of commercial sample and hold amplifiers impossible and the use of integrators difficult. Synchrotron oscillations can introduce substantial jitter in the arrival time of PUE signals with respect to the ring timing system, making externally gated rectifiers impractical. The analog front end described in this paper accurately samples the amplitude of the PUE pulse in the presence of timing jitter

2 SYSTEM DESIGN

One unit of the system is shown in figure 1. Monopulse networks are used to generate sum and difference signals from the PUE pulses. The sum and difference signals are then rectified, stretched, and held by the analog boards. The outputs from two analog boards are processed by each digital board. Once digitized, the CPU calculates the beam position and transmits the data to the control system via ethernet.

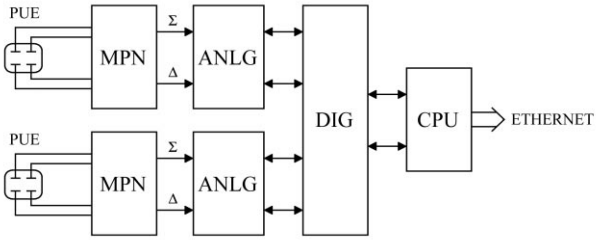


Figure 1: Simplified system block diagram

2.1 Analog Board

A simplified block diagram of the analog board is shown in figure 2.

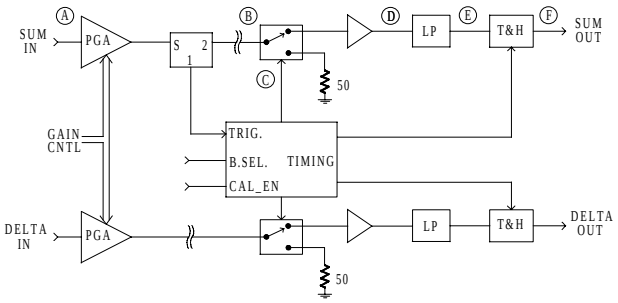
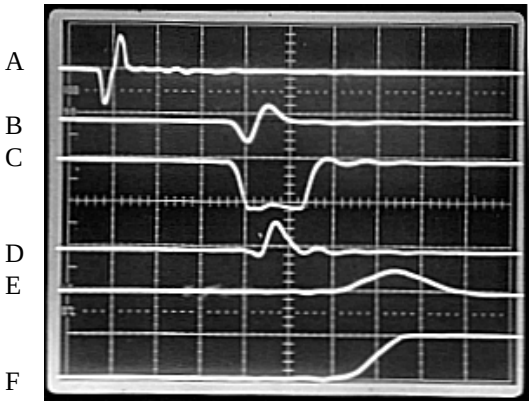


Figure 2: Analog board block diagram



5nS/Div

Figure 3: Analog board waveforms

* Work performed under the auspices of the U.S. Department of Energy.
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The associated waveforms are shown in figure 3. The sum input (trace A) is amplified by the programmable gain amplifier (PGA) and split two ways. The PGA is consists of two GaaS FET multiplexers, two amplifiers, and 1 attenuator. The selectable gains are -6dB, +12dB, and +24dB and are controlled by the digital board via the P2 backplane. Splitter output 1 triggers the timing circuit and splitter output 2 is routed to a SPDT GaaS FET switch via a coaxial delay line. The delay line compensates for delays in the timing circuit so the gate arrives at the switch at the correct time to rectify the sum signal (traces B and C). When the gate drops low the positive going lobe passes though the switch (trace D). A 50 MHz gaussian lowpass filter then stretches the pulse (trace E), allowing the track and hold amplifier to accurately sample the signal (trace F). The delta signal is processed similarly.

The digital board drives the bunch select (B. Sel.) input with a 10nS pulse, selectively enabling the timing circuit only for the chosen bucket. A PUE sum signal arriving during the 10nS window triggers the timing circuit, generating control signals for the GaaS FET switches and the track and hold amplifiers.

The output offset voltage can be measured with no beam in the ring by pulling the CAL. EN. bit high and applying pulses to the B. Sel. input. This generates the same timing signals that would normally be produced by the PUEs. This is useful for measuring and correcting drift in the electronics. The linearity of the analog board at three different gain settings is shown in figure 4.

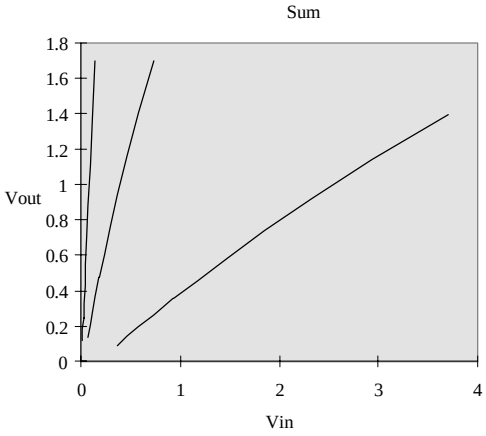

Figure 4: Analog board linearity

2.1 *Digital Board*

The digital board (figure 5) is a four channel transient digitizer with 12 bit resolution, 8MHz maximum sampling rate, and 32 Ksamples of buffer memory. Pretrigger and posttrigger timing modes have been implemented, allowing the trigger to appear at the beginning, middle, or end of the sampled data.

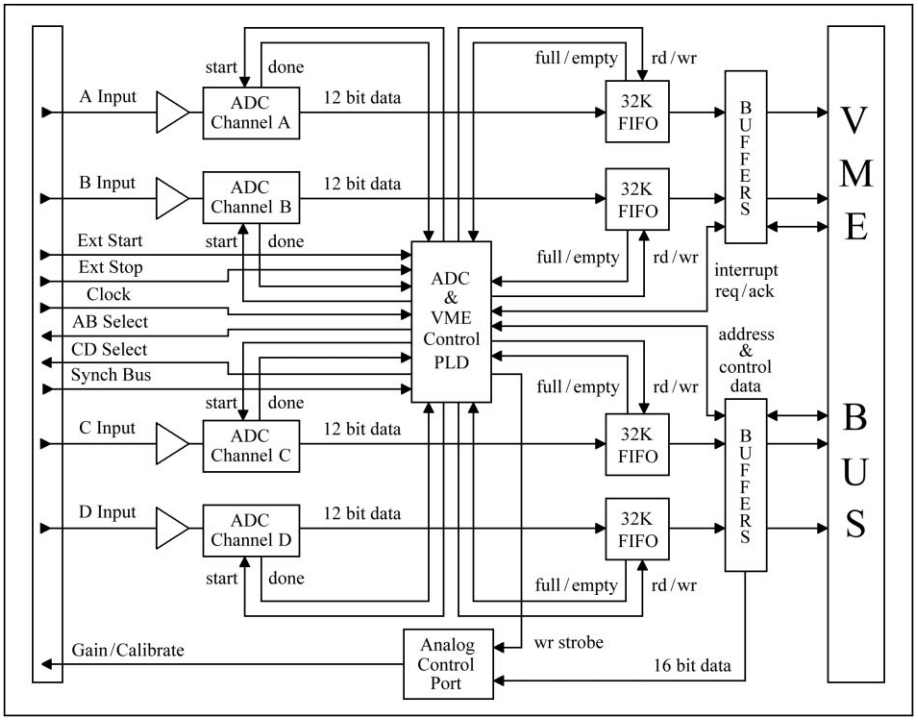

Figure 5: Digital board block diagram

Triggering and halting the data acquisition process can be accomplished either externally, or internally under software control.

The unit provides an independently delayed bunch select pulse (AB Select and CD Select) for each analog board. Each delay generator has a range of 150nS with a resolution of 0.3nS. External timing signals that are locked to the beam rotation period (Clock and Synch bus) drive the state machine and delay generators. A 16 bit TTL port on the P2 backplane (Gain/Calibrate) controls the PGA gain on the analog boards.

The VME interface provides slave functions with standard A(24)D(32) single and block data transfer modes. Interrupt level and interrupt vector ID can be defined by the application software.

3 PERFORMANCE

Turn by turn beam position measurements in the NSLS UV ring are shown in figures 6 and 7. Only the first 200 turns are shown for clarity. The graphs show the horizontal orbit distortion to stored beam resulting from the injection kicker magnets. The bump is not closed and a large residual betatron oscillation results. Prior to turn 47 the beam is undisturbed and the noise floor is visible. The noise is 0.1mm RMS at 750 mA and 2mm RMS at 25 mA. Note in figure 7 the noise is periodic, and probably due to RF pickup. Improved shielding in the production version of the analog board should improve the noise performance. The noise floor measured on the bench is 50μM.

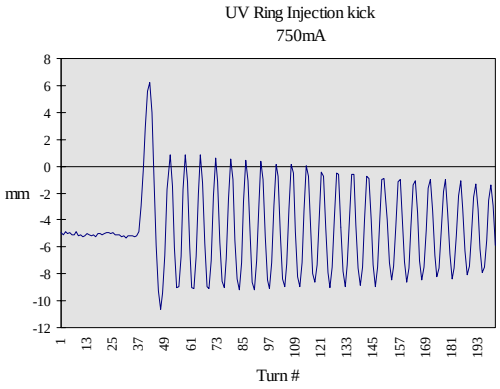

Figure 6

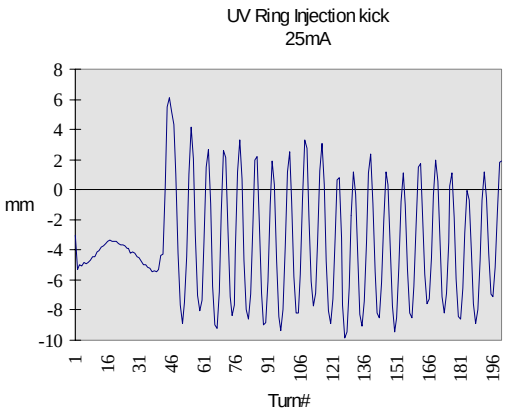

Figure 7

4 ACKNOWLEDGEMENTS

The authors would like to thank Jack Tallent for his assistance breadboarding and prototyping this system.

Analog board layout by 4DI, Inc. 97 Marcus Blvd., Hauppauge, NY 11788.

5 REFERENCES

[1] http://www.nsls.bnl.gov/Systems/SingleTurn/singleturn.htm