COOLER INJECTOR SYNCHROTRON CONTROL HARDWARE AT INDIANA UNIVERSITY CYCLOTRON FACILITY[#]

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Abstract

This paper describes the control hardware at IUCF for the newly commissioned 200 MeV CIS ring. A combination of "commercial off the shelf" and custom "in house" hardware makes up DAC, ADC, and timing control for this synchrotron. The focus of this paper is on the custom designed hardware.

1 INTRODUCTION

The control hardware designed and manufactured at IUCF meets strict specifications combined with self-calibration, self-diagnostic, I/O protection, and serviceability options not attainable commercially. The CIS control system is comprised of three primary subsystems, timing, ramping and non-ramping, all which interface with the host control computer via distributed VME buses. IUCF's custom ramping subsystem has two main components, Sequencers and Ramping Analog Heads, with a third, Timing/Frequency Heads, planned in the future. The 6U VME Sequencer is a timing computer and data sequencer that provides digital inputs and outputs and a high speed fiber optic bi-directional data stream to a Analog Head. The Analog Head receives data from a Sequencer and converts the data to a single 18 bit DAC output channel and collects 16 bit ADC data returning it to the Sequencer. The timing subsystem consists of a master Sequencer which time synchronizes and triggers all the other Sequencers and Brookhaven V102 delay modules [1]. Together the Sequencers and the V102's provide all the digital timing input and output signals needed. IUCF's non-ramping system consists of custom 3U VME modules, which are low speed, high precision, 16 bit, 4 channel DAC's or ADC's. Both ramping and non-ramping analog sections employ optical data isolation for high noise rejection, very low drift voltage reference, extensive I/O protection, self-calibration, and self-diagnosis hardware for calibration or functional problems. All the IUCF modules have many front panel LED's indicating operational states, error conditions and histories. As well, all IUCF hardware can be "hot swapped" in and out of the VME crates for faster servicing. In total well over a hundred IUCF VME modules control the CIS ring. Commercial VMIC [2]

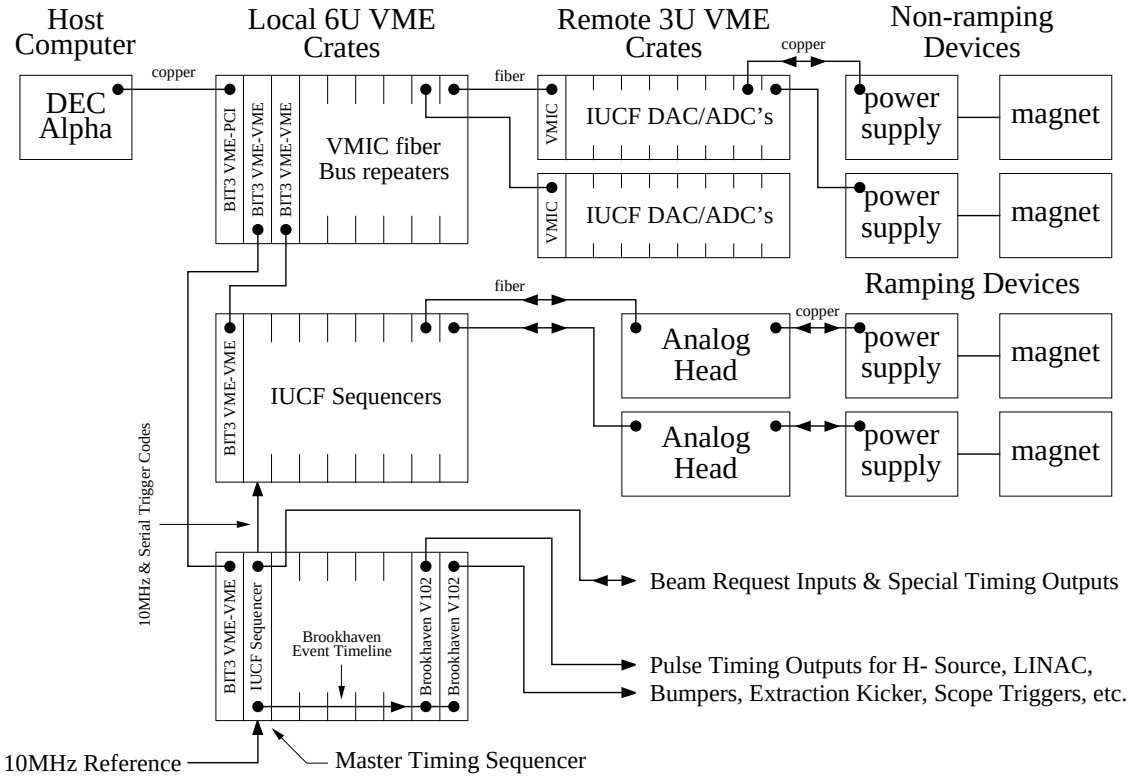

Figure 1: CIS Control System Overview

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fiber and BIT3 [3] wired VME bus repeaters fan out control to many VME crates from a single DEC Alpha desktop workstation. Figure 1 shows an approximate arrangement.

2 SEQUENCERS

IUCF Sequencers transmit and receive ramping data to IUCF Analog Heads over 10 megabyte/second glass fiber links. Each Sequencer provides 8 front panel digital ports, which can be individually configured to be 50 ohm series or parallel terminated inputs or outputs. Special I/O ports synchronize and exchange serial trigger codes to other Sequencers and provide phase locking of all Sequencer clocks. VME interrupt capability is also provided. The front panel of the Sequencer contains 24 tri-color LED's that provide a wealth of diagnostic and operational information.

The sequencer board contains a large multi-ported DRAM (Dynamic Random Access Memory) that is either 4, 8, 16, or 32 Megabytes depending on the SIMM installed. Its ports tie to the VME bus (A32; D32 D16 D8EO BLT UAT [4]), an on board FPGA (Actel A1240XL [5]) based hardware timing and data processor called the Sequencer Processing Unit (SPU), and a local bus that plugs into a daughter DSP card. From the VME bus the board appears as plain RAM memory, except for some reserved locations. The DSP port allows memory access just like the VME port.

Internally, the SPU reads instructions and data from this memory, processes it, transmits data out the fiber port to a remote head, and writes data received from the fiber port into this memory. The SPU can output digital data on the front panel, send serial codes to another Sequencer, interrupt the VME host, test digital inputs, test for serial codes coming from another Sequencer, and more. By design, SPU executes all instructions in exactly 1 uS except for special delay instructions. These delay instructions execute in 1 uS plus N times 100 nS or 1 uS, or wait for an external event. In this way the SPU allows for totally flexible and precise timing of digital and analog control signals.

To use a sequencer, the host VME computer writes an instruction stream (I.E. download a binary program) into a block of memory locations, set the SPU's program counter, and start the SPU executing. The SPU then executes through this instruction stream which normally would send ramping data out the fiber interface to an Analog Head. The Analog Head acknowledges with an ADC sample which is sent back to the Sequencer and recorded in main memory. In this way, a diagnostic ramp of the supply output is available for inspection. Additionally, the SPU can write digital data out the front panel or to the digital outputs on the Analog Head. Also, a typical SPU program would wait at certain points for external triggering from the master timing Sequencer, so that all analog ramps will be timed together as required to run the synchrotron.

3 GLASS FIBER LINK

Sequencers talk bi-directionally to the Analog Heads through a 10 megabyte/sec fiber link. 32 bit Sequencer data is broken into 4 bytes and serialized at 120 Mbaud using AMD TAXI transmitter (Am7968 [6]). The high-speed serial PECL data is converted to 1300 nm optical data using a Hewlett Packard HFBR5103 transceiver which allows for up to 2 Km transmission. At the Analog Head the same optical transceiver and the AMD TAXI receiver (Am7969) convert the optical data back to parallel bytes. Data from the Analog Head is sent back to the Sequencer in exactly the same way.

The AMD TAXI receiver and a local crystal PLL provide a local 10 MHz frequency reference that is phase locked to the driving Sequencer, which in turn is phase locked to the master timing Sequencer. In this way all remote data can be timed exactly to specific cycle of a master 10 MHz clock. Also, upon reception, parity bits and the data packet framing is checked for possible transmission errors. If an error does occur, the Analog Head requests the data be resent. Any data errors, signal strength loss, or phase lock problem shows up on front panel LED's and a history of these errors are kept.

4 RAMPING ANALOG HEADS

The Analog Head provides the interface between the Sequencer's ramping data stream and the power supply under control. This head is composed of fiber optic Interface card and an Analog card that slides in DIN 3U card cage, but does not use a backplane. The front panel has power, analog I/O, digital I/O, fiber, and backup connectors. The Interface card translates the incoming 10 megabyte/sec fiber data into a 32 bit word which is sent to the Analog card as parallel data over a 96 pin DIN connector that connect the 2 cards. Also, the Analog card sends a 32 bit response back

This command word is used to control all operation of the Analog card. Control bits within this 32 bit word provide for large set of command instruction to the card. Primarily, 18 bits of this data is sent to the 18 bit DAC (Burr Brown DAC729KH [7]) which controls the connected power supply through the output channel. The 18 bit DAC is jumper selectable for 0 to 10 volt or –10 to 10 volt output. Normally, the card responses by taking a 16 bit ADC (Burr Brown ADS7805P [7]) value from one of three input channels and sending it back to the sequencer over the fiber. A different card command writes or reads 4 bits of digital I/O data.

Other commands allow for remote calibration, testing and re-calibration. This is accomplished by calibrating the 24 bit sigma-delta ADC (Analog Devices AD7712AN [8]) with an onboard ovenized 10 volt reference (Linear Technology LT1019 [9]), then using the 24 bit ADC to

measure the gain and offset of the 18 bit DAC. Finally, the octal trim DAC (AD8842) outputs are changed to re-calibrate the 18 bit DAC. In this way better than 1[PPM/C temperature drift can be realized without having an ovenized DAC.

IUCF Analog Heads achieve outstanding analog noise rejection since they are individually fully isolated from ground and since they are normally located within a few feet of the power supply under control. Data isolation is provided by glass fiber and power isolation is provided by low capacitance, 120 VAC, linear power supplies.

The DAC output can detect an overload condition and reports this to front panel LED and to the hosting Sequencer. Transorb's and fuses protect all external connections from severe abuse. Output relays provide quiet outputs while the Analog Head is powering up and also provide for active redundant switchover.

IUCF's ramping system allows for active redundant connections for critical applications in a primary/backup arrangement. If a primary ramping system should detect a fault and the primary Analog Head is plugged into an active and ready backup Analog Head then the primary can release control and let the backup take over. A large set of fault conditions are continuously tested by hardware and any detected fault condition will cause the switchover. Programming bits in control registers allows for masking of each fault individually.

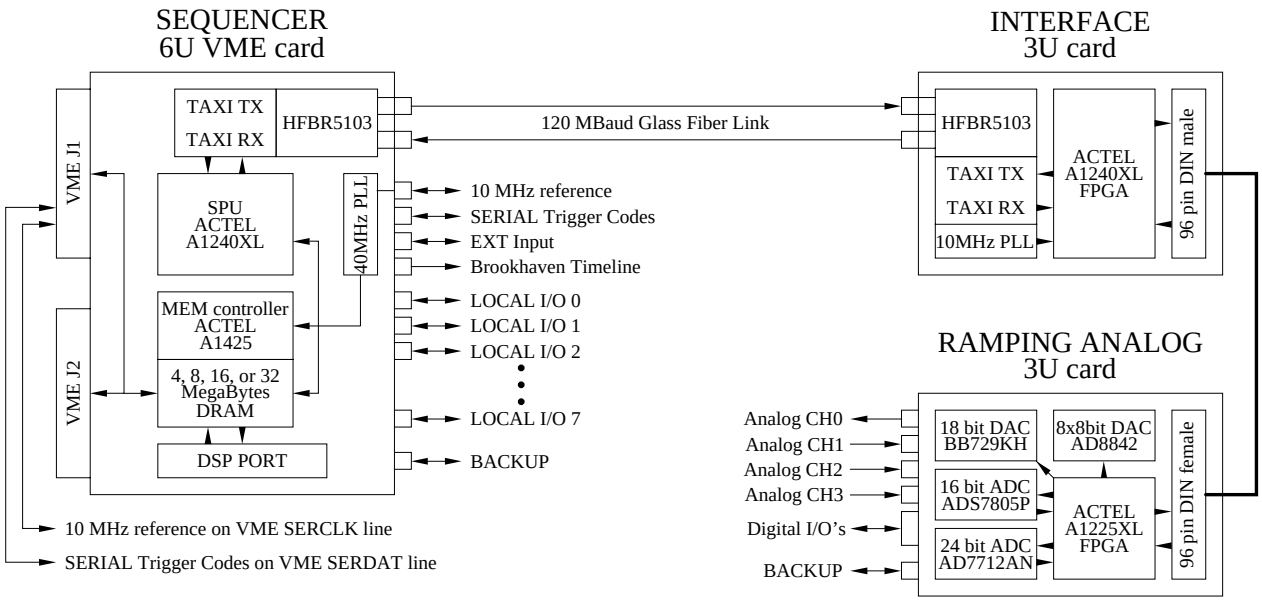

Figure 2: Ramping System Modules

5 NON-RAMPING DAC/ADC'S

IUCF's non-ramping DAC/ADC module provides four 16 bit, -10 to 10 volt, opto-isolated, individually switch selectable DAC or ADC channels, in a 3U VME package. The basic ADC works by digitally timing a voltage comparator's output whose inputs are connected to the an ultra linear ramp and the voltage to be sampled. The basic DAC is a digitally controlled integrator whose output ties to an ADC channel for feedback control. The ADC conversion's result steers the integrator up or down until the precise voltage is obtained. The main drawback is its very slow speed, but it is still more than fast enough for human controlled non-ramping devices. The main advantage is its absolute precision, and almost perfectly even DAC steps (DNL is much less than 1/16 bit). This gives the operator consistent power supply control, even when changing only one DAC step at a time.

This unique "in house" design achieves analog conversion has +/- 0.01 percent absolute full-scale accuracy over the operating temperature range, with a maximum of +/- 1 bit zero error. This design accomplishes this by continuous self-calibration of the ultra linear ramp for positive full scale and zero. It tests positive, zero, and negative full scale for tolerance. Should the unit not meet specification, front panel LED's will show the fault and the host computer can also query for this condition. Each DAC output is checked for a 1.5 bit tolerance, which if not met will show a fault condition as well.

6 REFERENCES

[1] http://www.rhichome.bnl.gov/Hardware/timeline/eventsys.htm
[2] http://www.vmic.com/products/chap8/hw_repeat_index.html
[3] http://www.bit3.com/
[4] ANSI/IEEE STD1014-1987 IEC821 AND 297
[5] http://www.actel.com/products/fpga_devices.html
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