DIGITAL LLRF CONTROL SYSTEM DESIGN AND IMPLEMENTATION FOR APT SUPERCONDUCTING CAVITIES*

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Abstract

With a rapid development of the digital signal processor in recent years, a full digital control system for the superconducting section of APT is designed and implemented by using TI's C6x processor. A digital control system is first modeled and simulated using Matlab/Simulink. Simulation results confirmed the feasibility and flexibility of the digital control system for LLRF feedback system. Due to flexibility of DSP, different control algorithms will be implemented and compared in the system. Particular attention will be paid to the inherent pipeline delay problem associated with a digital control system and its effect and limitation on the overall system performance.

1 INTRODUCTION

The advance of digital signal processors and high performance digital data acquisition and conversion devices in the last few years makes it possible to have a full digital LLRF control system design for superconducting cavity of APT due partly to the narrow bandwidth of a high Q cavity. The advantages of the digital system over the analog one include flexibility and versatility provided by digital signal processor. Due to enormous computational power of DSP, it becomes feasible to implement sophisticated control and digital filter algorithms[1]. However, on the other hand, its drawback is added time delay in data conversions and computations associated with digital systems.

The digital control system implemented in the LLRF includes a digital I/Q demodulation circuit, DSP, and D/A converter. In the digital I/Q demodulation circuit, 50MHz IF signal is sampled by a fast 40MHz A/D converter which generates a data string of I, Q, -I, -Q, …. The output of the A/D is fed into a PLD, which separates I and Q components of the data string and applies adequate sign swap. The digital I and Q signals are sent to two digital decimate filters (DDF) whose outputs are digital I/Q with an update rate up to 1MHz. The DSP reads the decimated I/Q signals from DDF and processes with a chosen control algorithm. The output of the DSP is sent to a D/A converter, and the output of the D/A converter is directed to the amplifier control module of the LLRF system. The total time delay through the digital control system, which includes A/D converter pipeline delay, I/Q decomposition and digital decimate filter delay, DSP I/O time delay, DSP processing delay, and D/A pipeline delay, is in the order of 2-5μs. The time constant of a high Q superconducting cavities is typically in the order of 500-1000μs. Therefore, the phase margin reduced by the digital control system is only at maximum about 3-5 degree which is a very good trade off for the advantages of the digital control system over analog one.

2 LLRF SYSTEM

The basic requirements of the LLRF control system for superconducting cavity is specified in terms of amplitude and phase stability of the cavity field in the suputerconducting cavity. In our case, the control requirements are 1% of amplitude error and 1° of phase error for the cavity field. These requirements are for entire accelerator RF systems, therefore, the individual RF system needs tighter control margin than that. On top of these, the LLRF system must be reliable and robust.

The overall LLRF system for APT's superconduncting system is given in Reference [3]. The RF operating frequency is 700MHz. Here we have one LLRF control system for multiple superconducting cavities driving by one klystron. The amplitude and phase control of the cavity field is accomplished by control I/Q components of the klystron driving signal. The multiple cavity fields are vector-summed before fed to the LLRF control system. The RF signals are converted to an IF frequency of 50MHz and sampled at 40MHz sampling rate. The DSP processes the incoming data and sends the corrected I/Q signals to the klystron. In order to reduce the effect of the beam noise on the cavity field, a digital feed forward control is implemented.

In the centre of the digital control system is a TI's TMS320C6201 digital signal processor, which performs maximum of 1,600MIPS with a 200MHz internal clock. An Analog Devices' AD9042, whose maximum sampling rate is 41MSPS with 12bits accuracy, is selected for A/D converter. An additional DSP may be required to perform supervising and communicating with VXIbus system. A digital decimate filter (HSPS43220 from Harris) is used between ADC and DSP to synchronise I/O data and to perform additional digital filtering functions. The decimation filter also provides additional enhancement on the signal accuracy and dynamic range.

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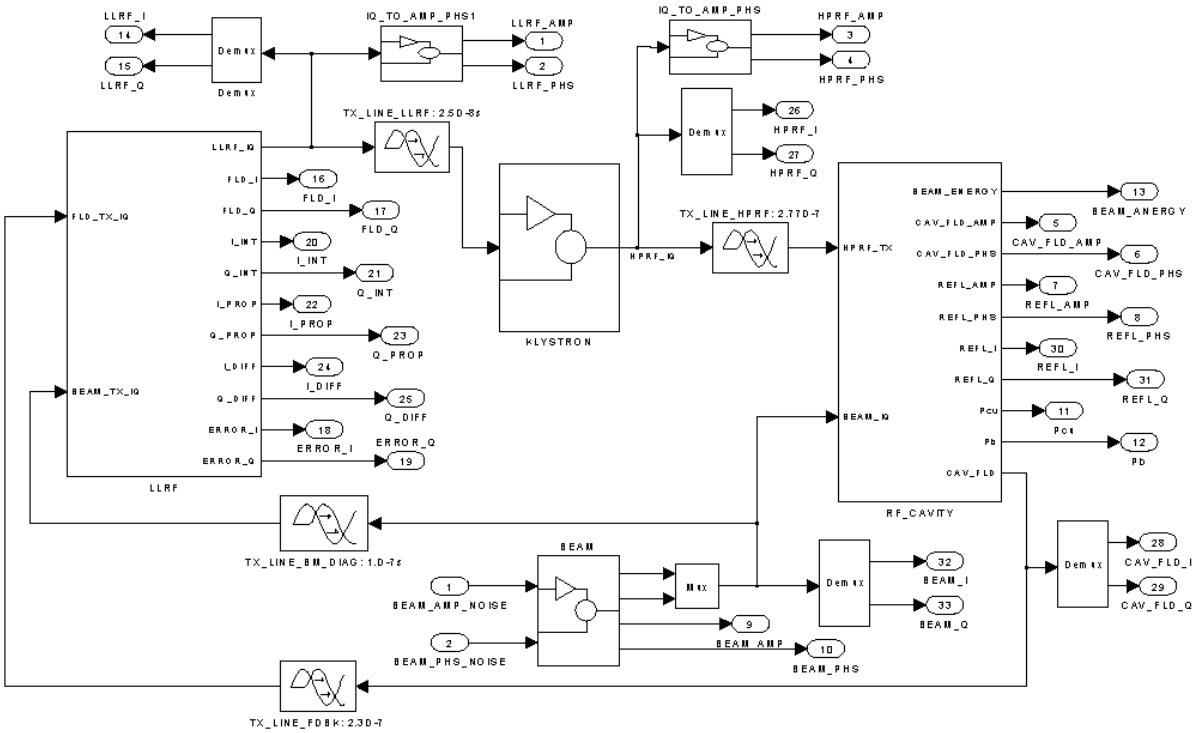

Figure 1. LLRF model

For example, for a digital loop bandwidth of 5kHz, the data should be processed at a rate of 50 KSPS. The filtering rate reduction from 20 MSPS to 50 KSPS provides a 52 dB improvement in the signal accuracy and dynamic range. The system clock from the backplane is 40MHz with a 10MHz synchronise clock. Both A/D and D/A converters are operated at 40MHz clock. Two DDFs are driven by a 20MHz clock generated by I/Q decomposition PLD. The data I/O of the DSP is also uses 40MHz clock. The internal clock of the DSP is 200MHz by multiplying 5 of the system clock. Total processing time will be in the order of 200ns to 1μs, which includes both I/O time and data processing time, depending on the complexity of the control algorithms. A cable delay is about 700ns. Data conversion of the A/D converter is 75ns with 40MHz clock. The time delay over the digital decimate filter is about 40ns when the DDF is operated at 1MHz output rate with filtered bandwidth of 250kHz. D/A conversion time delay is only 25ns. Summing the above together, the total time delay of the digital control system is about 2μs to 3μs which is significantly lower compared to 500μs time constant of the superconducting cavities. Notice that the phase shift caused by the time delay of the digital control system is about 3 degrees at 2 kHz.

3 MODEL SIMULATIONS

A Matlab/Simulink model is developed to simulate the system response and perform the stability analysis of the control system. Simulink, a companion program to Matlab, is an interactive system for simulating nonlinear dynamic systems. It can work with linear, nonlinear, continuous-time, discrete-time, multivariable, and multirate system. It is extremely useful for us in both system level and board level design. It helps us to verify system designs and performance, optimise control parameters, perform stability analyses. This model has been applied and proven on a number of LLRF control system designs. The overall model is given in the block diagram form by Figure 1. In this model, only LLRF sub-model is a discrete subsystem, all others are continuous system.

First, in order to verify the time delay effect of the digital control system over the system performance and stability, we simulated both the original system and the system with an added time delay contributed by the digital control system. The result is given in Figure 2 which reveals that the added time delay dose not give a significant effect on overall system performance due to a dominant pole at a lower frequency contributed by the

superconducting cavities. A simple PID controller is used in the above simulation. PID gains are chosen by using the Nonlinear Control Design Blockset to have a desired performance of the cavity field. The klystron is operated at 80% from the maximum power in the saturation curve.

HVPS ripple is evaluated for white noise to determine the worst-case frequencies. For a 1% ripple at 2 kHz caused a 3.0% peak-to-peak amplitude error and a 1.6° peak-to-peak phase error. This indicates a need for local feedback loop around the klystron to correct for HVPS ripple in the superconducting cavities.

An H^{∞} controller is implemented around the klystron to reduce the ripple effect from HVPS. The H^{∞} controller includes an estimator and a PI controller. The control gains are determined by an optimal control algorithm. The simulation results together with the original data without the local control loop are given in Figure 3. The ripple noise is reduced significantly by introduce a local feedback loop around the klystron. In this section, Lorenz-force detuning is not included due to its limited effect on the cw beam operation.

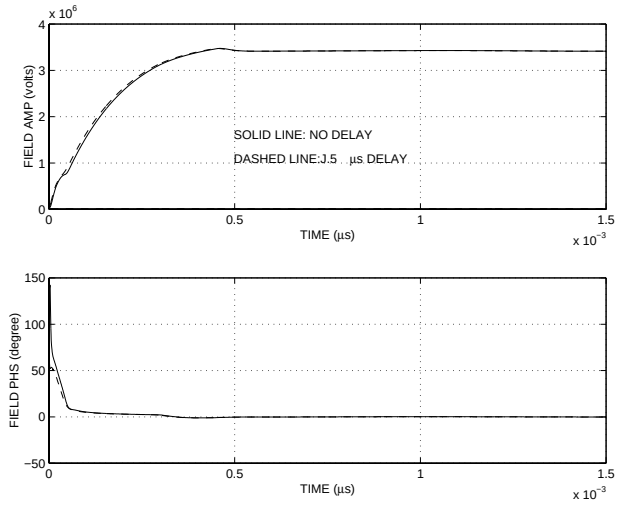

Figure 2. Cavity field response

The effect of the microphonic noise is modelled by a low frequency sinusoidal noise in the superconducting cavities. With a relatively higher gains for PID controller bellow 150 Hz, we can expect that the microphonic noise could be suppressed effectively with the global PID control loop. The simulation results confirmed the effectiveness of the digital control system on reducing the microphonic noise in the superconducting cavities.

The effect of the beam noise on the cavity field is also analysed using the Matlab/Simulink model of the LLRF control system. The cavity field response of the beam noise is first simulated with a normal digital PID controller without beam feed forward. The low closed-loop bandwidth of the superconducting system places less stringent demands upon the beam forward. Beam forward signals are only required with signal bandwidths of around 10 kHz. With manual gain adjustment, the beam forward is able to reduce the error caused by 1% beam amplitude noise and 1 degree beam phase noise at 2 kHz from 0.40%/0.11° to 0.01%/0.02. This demonstrated that beam forward is both necessary and could be easily implemented for the superconducting system[2].

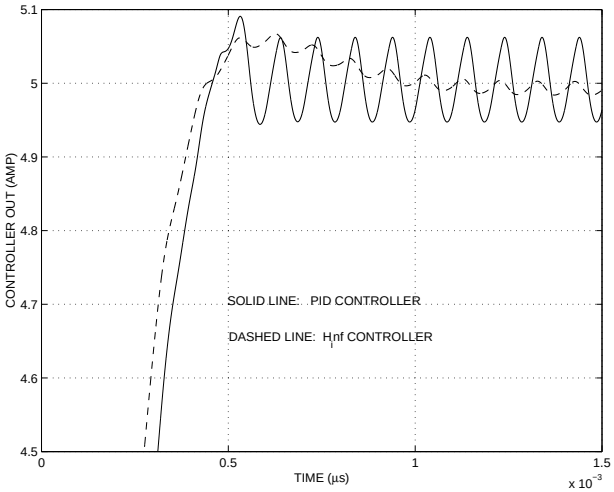

Figure 3. Cavity field with a local control loop.

4 CONCLUSIONS

A digital control system design has been developed for the superconducting cavities of APT. Application of the fast TI's C6x DSP together with the high speed and high performance devices for data conversion makes the implementation of the hardware design both feasible and reliable. The simulation results reveal that the time delay associated with the digital control system is acceptable and has no significant effect over phase margin and stability of the overall superconducting system. With the help of beam feed forward and local fast response control loop around the klystron, the cavity field of the superconducting system can be controlled in the range of the design requirements. Further investigation is required to compare the hardware and system performance with the simulated results given in this paper. The comparison between the simulations and experiment data will be conducted as soon as data is available.

5 REFERENCES

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