Performance and Radiation Tolerance
of the ATLAS CSC On-Chamber Electronics

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Abstract

The on-detector electronics for the ATLAS Cathode Strip Chamber (CSC) performs amplification, analog buffering, and digitization of the charge signals from individual cathode strips. Working in a high-rate environment (strip hit rate up to several hundred kHz) the system requires a signal-to-noise ratio of 200:1 and a minimum dynamic range of 10-bits. The implementation of the on-chamber electronics to meet the CSC requirements is described, along with a discussion of the proposed system architecture and how it minimizes the problem of radiation induced errors and failures.

I.   Introduction

The CSC system forms the forward section of the muon spectrometer of ATLAS. It consists of 64 chambers. Each chamber consists of four layers. There are 768 precision (x) and 192 (y) strips per chamber. The readout pitch is 5.547mm. Strip capacitance is 20-50pF. Interpolation is performed only on the precision strips. Front end electronics are located on ASMI and ASMII boards within Faraday shields along the narrow edges of each chamber, as
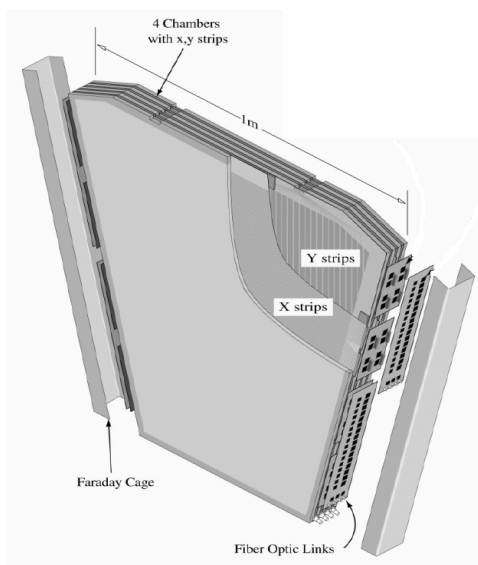

Figure 1. CSC Chamber

shown in Figure 1. Each chamber consists of ten ASMI assemblies and five ASMII assemblies. Transition boards provide shielding and optimal mapping of signals between the preamplifiers on the ASMI and the sampling and digitizing functions on the ASMII. .

There are eight ASMI assemblies and four ASMII assemblies dedicated to the precision strips. Two ASMI assemblies and one ASMII assembly service the transverse strips.

The outer skin of the chamber is ground. A continuous strip of copper exists around the perimeter of the cathode planes to connect to the skins. The purpose is to provide a low impedance connection at all points on the chamber. The Faraday shield is connected to the chamber by bolts. These bolts also serve as ground connection point to the skin and provide a connection within the Faraday shield to the circuit boards. Low voltage, +6VDC is brought to the circuit boards from a remote power supply via bulkhead terminals. Three multimode fibers are connected to the ASMII via SC bulkhead fiber connectors. Bulkhead connectors are used to maximize the effectiveness of the Faraday shield.

The ASMI assembly consists of eight custom CMOS preamplifier-shaper ICs [2] with 12 active channels and one reference channel. for coherent noise reduction.

The ASMII assembly stores analog samples, digitizes the samples to 12-bits then serializes the ADC data to two gigabit optical links to the off-detector electronics. Control to the sampling and digitizing circuitry is provided via fiber optic link from the off chamber electronics.

II.   System Architecture

The ATLAS CSC system architecture is illustrated in Figure 2. Charge from ionized gas induced on the cathode strips is amplified on the ASMI module by the preamp shaper. Bipolar 7th – order shaping is performed. Twelve active channels are used. The twelve signals along with a reference signal are sent to the ASMII via the transition board. These signals are connected directly to the a custom CMOS switched-capacitor analog memory (SCA) [1]. The SCA consists of an array of 12x144 storage cells with simultaneous read-write capability. Control of the SCA is. sent over an Agilent Technologies G-Link optical link operating in the single frame mode with a 20-bit data field operating at an 40MHz frame rate.
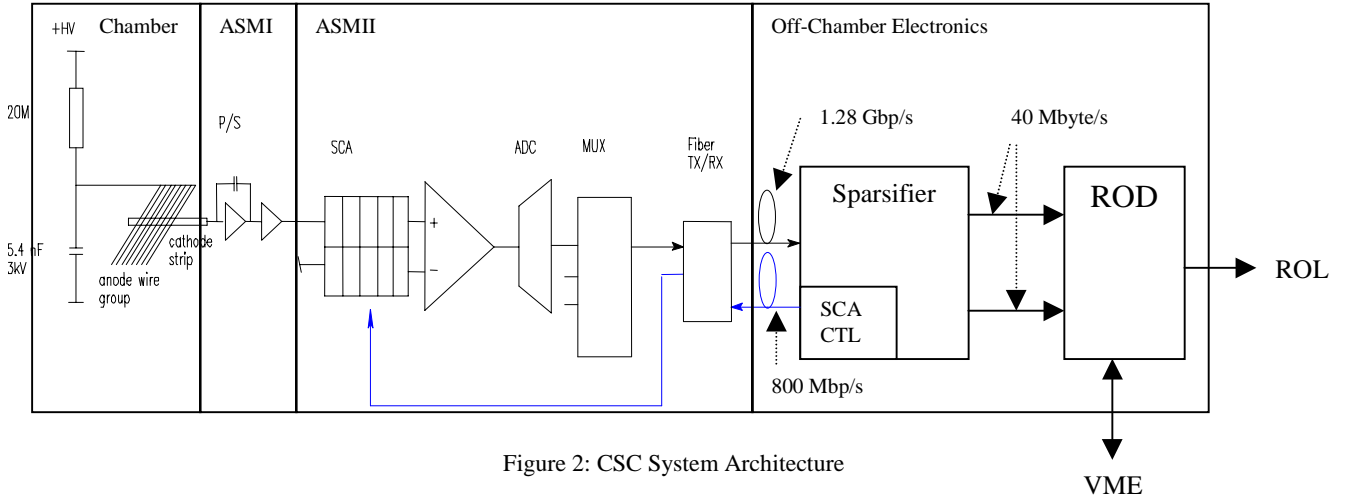
Figure 2: CSC System Architecture

Data is transmitted from the ASMII over two G-Links to the off-chamber electronics at a rate of 640 Mbp/s per link or 1.28 Gbp/s total. The aggregate chamber rate is 6.4 Gbp/s. There are two end-caps with each end-cap consisting of 32 CSC chambers. Total data rate per end-cap is 206 Gbp/s or 412 Gbp/s for the entire CSC system. Each of the "downstream" G-Link data links operate in the 16 bit single frame mode with a frame rate of 40MHz. Only raw data is transmitted from the chamber. When a trigger is received the off-chamber electronics initializes the SCA read, only at this time is meaningful data transmitted. Between triggers the G-Link transmits fill frames to maintain link synchronization.

III. Signals and Noise

Muons generate about 75 electron-ion pairs (Landau peak). About 12% of charge is collected by the precision cathode in 100ns. The average signal size expected is 144fC where the central strip of the cluster receives approximately half of the charge or 72fC. The electronics noise should not degrade the position resolution of the system. The required input referred noise as a function of the average charge is calculated by the following expression:

$$\sigma_{x,elec} = \frac{\sqrt{3} \cdot d \cdot ENC}{Q_\lambda} \le 33 \mu m \qquad (1)$$

Where d = strip pitch, ENC = equivalent input noise charge, and Q_λ = total charge induced on cathode plane. From this expression the the calculated required noise limit is:

$$ENC \le 0.5 fC = 3100 e^- \leftarrow Total\ input\ referred\ noise \quad (2)$$

The required signal to noise ratio is calculated as:

$$SNR_{max\ strip} = \frac{Q_{\lambda,cent}}{ENC} = \frac{72 fC}{3100 e^-} = 145 \qquad (3)$$

The dynamic range required for a 98.5% efficiency is calculated as follows:

$$\frac{Q_{fs}}{Q_\lambda} \ge 5, \quad \therefore Q_{fs} \ge 5 \cdot Q_\lambda = 725 \cdot ENC \cong 360 fC \qquad (4)$$

where Q_{fs} is the full-scale charge. Preamp/shaper gain for V_{FS} (positive lobe of bipolar waveform) is defined as:

$$P/S\ Gain = \frac{V_{FS}}{Q_{FS}} = 4.7 mV / fC \qquad (5)$$

Quantization noise as a function of the full-scale charge and total input referred noise can be calculated by:

$$\frac{Q_{FS}}{2^{Nbits} \cdot \sqrt{12}} << ENC \quad \therefore Nbits >> 7.7 \qquad (6)$$

To minimize the quantization noise of the ADC such that the predominant noise source is the preamp/shaper an Analog Devices AD9042 12-bit ADC has been selected. Concern over gain and offset variations as well as exposure to radiation was also a criterion for this selection.

IV. High Rate Performance

The ATLAS muon CSC is subject to a high background rate environment. The overall background rate expected is 10^7 Hz per chamber. Background consists of 50% charged particles, 50% neutron and γ. Charged particle background is rejected by a timing window around trigger or by pattern recognition of non-projective tracks. Out-of-time background suppression is performed off-chamber in the Sparsifier, neutron rejection is performed off-chamber in the ROD or offline.

Neutral particles produce short-range electrons that are generally confined to only one layer. However, neutrals that hit anywhere in the chamber induce charge on all strips by anode-cathode crosstalk defined as:

$$Q_{cross} = \frac{C_{ac}}{C_{filt}} \cdot Q_{anode} \cong 10^{-4} Q_{anode} \qquad (7)$$

where C_{ac} is the capacitance from a strip to the anode wire (~ 0.5 pF), and C_{filt} is the high voltage filter capacitance (~ 5 nF). Some of the neutrals can produce very large charges:

- 50% of neutrals above Q_{FS}
- 1% of neutrals above $6 * Q_{FS}$

The cumulative result of this induced charge on all of the strips behaves like electronic parallel noise, thereby degrading both the position resolution and efficiency of the chambers

IV. Sampling

The number of waveform samples that can be transmitted off detector is limited by the optical link bandwidth. Because of the 35 ns maximum drift time of the CSCs, it is impossible to select a set of four samples at 40 MHz that guarantee inclusion of at least one sample before and after the peak of the preamplifier waveform (see Fig. 3 below).
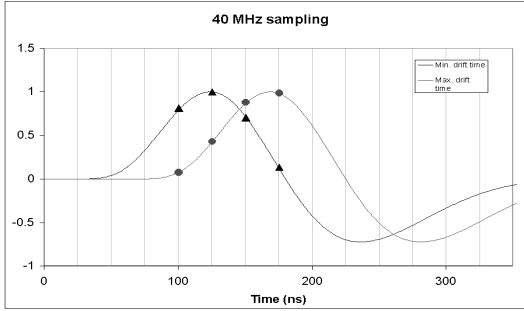
Figure 3. 40 MHz Sampling

The L1 trigger incurs a latency that includes cable delay and electronics processing by the TIM module and the off-chamber back of crate cards. This latency is estimated to be 98 bunch crossings. Additional latency is incurred by signal propagation from off-chamber to on-chamber electronics and the readout latency of the SCA. An additional 27 bunch crossings is estimated for this latency. The total estimated latency is 125 bunch crossings. The worst-case latency condition occurs for the maximum L1 trigger burst rate defined as eight consecutive triggers each spaced at 125ns intervals. The SCA is read-out at a rate of 6.67 MHz (150ns). Since 15 clock cycles are required to readout one time sample the 8th trigger arrives before the first time sample of the first trigger is readout. Beam studies have indicated that four time samples are adequate. The pipeline depth required for eight triggers would then be 32 bunch crossings. The pipeline depth of the SCA is 144 bunch crossings. Since the L1 trigger latency has been estimated as 125 bunch crossings and the required pipeline for an

eight trigger burst is 32 bunch crossings the SCA pipeline depth of 144 bunch crossings is not adequate. To circumvent this problem we have chosen to sample at a rate of one-half the bunch crossing rate or 20 MHz. Figure 4 illustrates the case of 20 MHz sampling. Again two waveforms are shown to illustrate the maximum drift-time of 35ns; now the peak and its neighbors are selected for the worst-case drift times.
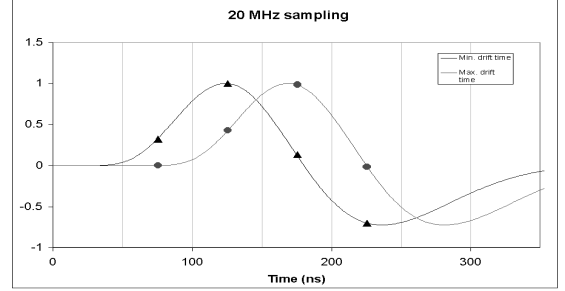
Figure 4. 20 MHz Sampling

The SCA pipeline depth is effectively doubled to 288 bunch crossings. Studies of existing beam test data were analyzed by decimating the 40 MHz sampled data by a factor of two. Decimation was done for both even and odd samples. The result of the analysis indicated no increase in inefficency.

V. Preamp/Shaper and ASMI

Each ASMI contains eight preamp/shapers supporting a total of 96 channels per ASMI. Each ASMI contains edge connectors that directly plug into cathode plane fingers that protrude from the chamber. On each side of the chamber four ASMI modules pick up two planes.

The Preamp/Shaper ASIC has been fabricated in a 0.5 μm CMOS technology. Table 1 summarizes the measured characteristics of the preamp/shaper ASIC [2].

Technology	0.5 μm CMOS
Channels	16
Die size	2.78 x 3.96 mm
Architecture	Single-ended
Intended Cdet	20 – 100 pF
Input device	NMOS W/L = 5000/0.6 μm, Id = 4mA
Noise	1140 + 17.6 e-/pF
Gain	3.8 mV/fC
Max. linear charge	450 fC
Class AB Output swing	To power supply - 250 mV
Pulse shape	7th order complex Gaussian, bipolar
Pulse peaking time, 5% - 100%	73 ns
FW1%M	340 ns
Max. output loading (3% distortion)	500 Ω, 500 pF
Crosstalk	0.8% adjacent, 0.5% non-adjacent channel
Power supply	Single +3.3V
Power Dissipation	32.5 mW/chan

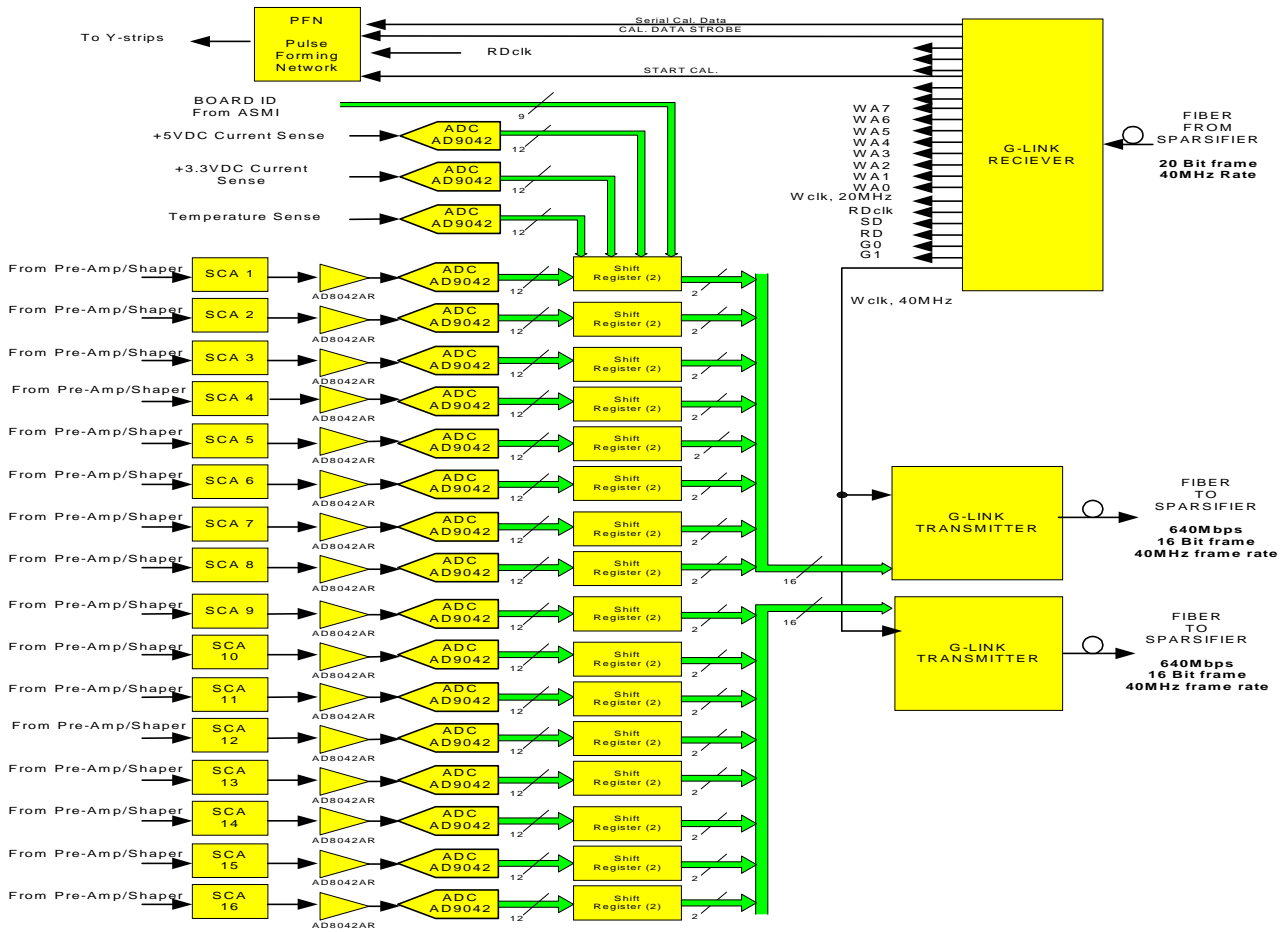Table 1. Preamp/Shaper Specifications

Figure 5. ASMII

VI. ASMII

All on-chamber signal processing excluding pre-amplification and shaping is performed on the ASMII. Each ASMII is capable of processing 192 channels. There are four precision ASMII's and one transverse ASMII per chamber. Signals from the preamp/shaper are sent to the ASMII from the ASMI through a transition board. Each preamp transmits 12 channels and one reference channel to each SCA. The purpose of the reference channel is to subtract coherent front end noise at the output of the SCA. The ATLAS LAr Calorimeter SCA has been modified for use in the muon system. By applying the correct voltage to a dedicated pin on the SCA operates in muon mode where cell's are continuously read-out to a dedicated ADC. The SCA outputs are then quantized to 12-bits by Analog Devices AD9042 ADC's. Each 12-bit ADC output is split into two 6-bit data streams that are converted to serial data at 40MHz bit rate. COTS shift registers will be used for this application. Each ADC then occupies two data lines of the G-Link serializer. The G-Link transmitters are configured to operate with a 16-bit input word in the single frame mode at a frame rate of 40 MHz. There are two optical transmitter links, each link supports data transmission of eight ADC's. Four additional parameters are transmitted. Board ID is a hard-coded address corresponding to the physical location of each ASMII. Current sensing resistors will monitor the ASMI +3.3VDC and ASMII +5VDC supply currents. Temperature will be monitored on the ASMII. Each of these parameters are transmitted by streaming the digitized word of into two unoccupied shift register bits.

An optical link is used to provide the control signals to the SCA and calibration circuitry from the off-chamber electronics. An HP-1024 has been selected for this application. This approach removes the burden of having a radiation hardened SCA controller on-chamber.

VII. Radiation Tolerance

The approach to the development of the system architecture described above is primarily a function of the radiation conditions imposed on the CSC chambers. The worst case radiation conditions are:

ionizing dose of 4.4 krad/yr and neutron flux of $7 \cdot 10^{12} \, n/cm^2/yr$. Development of the system architecture centered on single event effects (SEU's) of CMOS logic elements. The design approach adapted to minimize this problem was to remove as much digital hardware from the chamber as possible, specifically the SCA controller. The trade-off is that an optical receiver is required on-chamber to receive control information. A test set is presently being developed to characterize the optical PIN diode and de-serializer when irradiated. Tests are expected to be completed by 2001.

Multiplexing of ADC data to the G-Link transmitters will be performed by COTS shift registers. This decision was based on the NRE cost to develop a rad-hard ASIC for this simple function. COTS qualification based on the ATLAS policy will be necessary. Other COTS items to qualify include an AD8042 op-amp, AD9042 ADC and MC10H116 ECL differential receivers. These items are common to the LAr FEB, and will be qualified with a joint effort among the two detector groups.

Ionizing radiation studies of the preamp/shaper have been completed. Four samples have been tested at BNL to 1Mrad. Results shown below indicate no significant effects from ionizing dose.
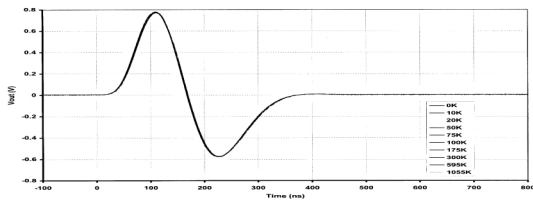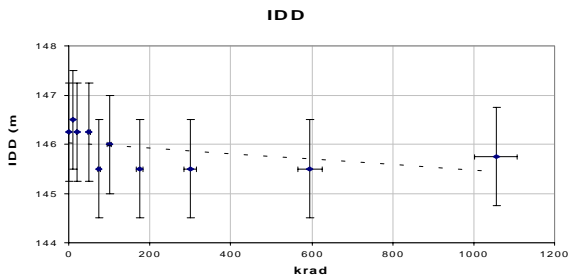

Figure 6. Pulse shape (offset subtracted)
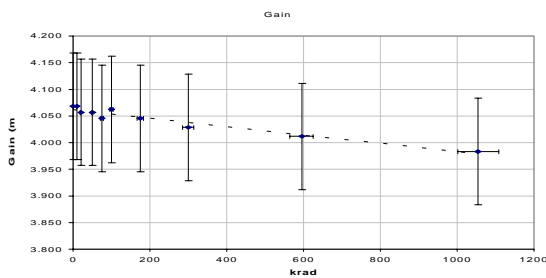

Figure 7. IDD
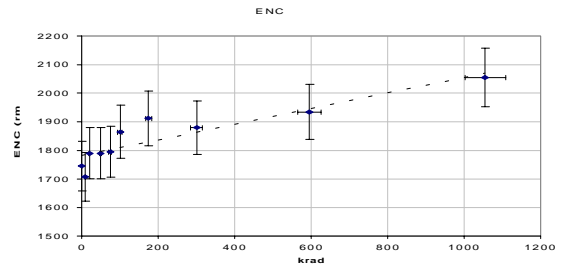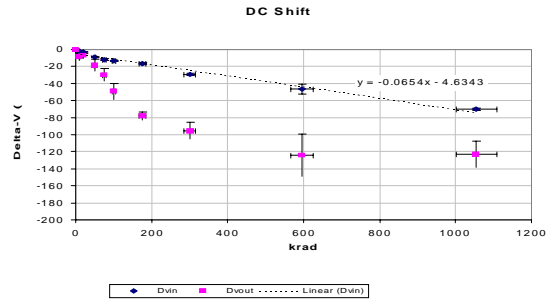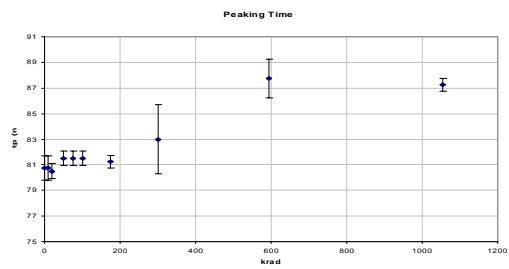

Figure 8. Gain

Figure 9. ENC

Figure. 10 DC Shift

Figure 11. Peaking Time

VIII. REFERENCES

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