An analog front-end in standard 0.25µm CMOS for silicon pixel detectors in ALICE and LHCb

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Abstract

A new front-end has been implemented on a pixel detector readout chip developed in a commercial 0.25µm CMOS technology for the ALICE and LHCb experiments. This technology proves to be radiation tolerant when special layout techniques are used, and provides sufficient density for these applications.

A non-standard topology was used for the front-end, to achieve low noise and fast return to zero of the preamplifier to be immune to pile-up of subsequent input signals.

The chip is a matrix of 32 columns each containing 256 readout cells. Each readout cell comprises this front-end and digital readout circuitry, and has a static power consumption of about 60 µW.

The complete readout cell will be described, but the paper will be mainly focussed on the front-end section.

I. INTRODUCTION

Hybrid pixel detectors offer several advantages over other detectors in the severe environment of the Large Hadron Collider (LHC) at CERN: low noise and low power consumption per channel, high channel densities and radiation tolerance, and low mass.

The ALICE experiment [1] will use pixel detectors in the two layers of the Inner Tracking System (ITS) closest to the interaction point. The baseline photon detector for the LHCb Ring Imaging Detector (RICH) [2] uses pixel detectors and readout chips to detect photoelectrons produced by Cherenkov photons: a pixel sensor and a readout chip are encapsulated in a vacuum tube to form a hybrid photon detector.

The ALICE1LHCB chip is a mixed-mode integrated readout chip for pixel detectors and can satisfy the needs of both systems by means of a selectable mode of operation.

II. RADIATION TOLERANCE

The ALICE experiment will use silicon pixel detectors as a part of the ITS, very close to the interaction point. This requires the chip to be tolerant to a radiation dose of about 500Krad (integrated over 10 years of the LHC operation). Although radiation hard technologies exist, they do not always provide adequate device density, so radiation tolerance is one of the main issues to be addressed during chip design.

Irradiation measurements on MOS capacitors showed a significant decrease of the radiation induced trapped oxide charge and interface states for oxides thinner than about 10 nm [3,4]. Gate oxides in present day submicron CMOS technologies are in this range (t_{ox} ~5.5nm for standard 0.25µm CMOS), and measurements on transistors implemented in these technologies confirm the significant reduction in radiation induced transistor parameter shifts [5].

Ionizing radiation can still lead to source-to-drain and inter-transistor leakage for the N-channel devices. Source-to-drain leakage can be avoided by using enclosed geometry transistors, while the inter-transistor leakage is eliminated by implementing P+ guardrings wherever necessary.

The effectiveness of this layout approach has been extensively proven for transistors in many CMOS technologies [5], and for complete mixed-mode circuits [6,7]. For the 0.25µm technology in which this front-end was designed, a test circuit tolerated a total X-ray dose of 30 Mrad(SiO_2) and subsequent anneal. It remained fully functional with only minor degradation of analog parameters and practically no change in power supply currents [8].

All digital storage elements in the chip have been designed to be immune to Single-Event-Upset (SEU), a

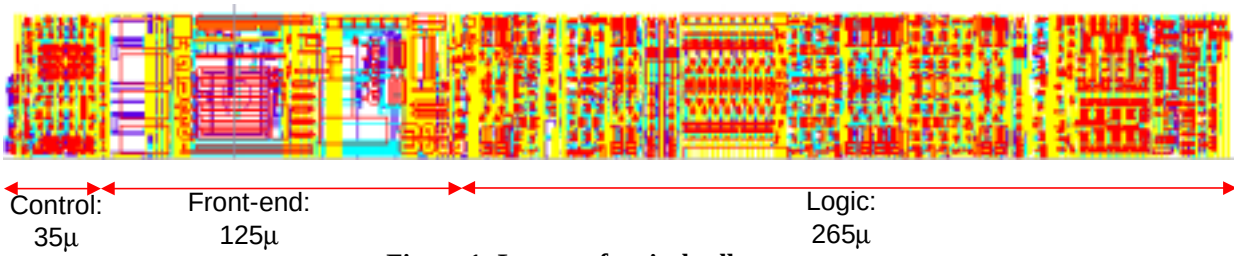

Figure 1: Layout of a pixel cell

phenomenon which can alter the configuration of the chip during operation. They use a special latch design which recovers its original state following an upset [9].

III. THE ANALOG FRONT-END

Figure 1 shows the layout of the 50μm × 425μm pixel cell. The analog front-end of the chip is composed of four main blocks: a charge preamplifier, a first shaping stage, a current feedback stage and a second shaping stage, which feeds a discriminator. A block diagram is shown in Figure 2.

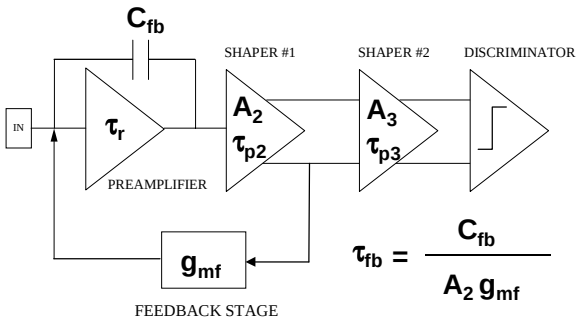

Figure 2: Analog front-end block diagram. Time constants and voltage gains are indicated.

A. The Charge preamplifier and the first shaping stage

The charge preamplifier is a differential pair with a single-ended, cascoded output and a feedback capacitor of 15fF. Incoming signal charge is integrated on this feedback capacitor. For detector readout, standard practise is to use a non-differential input for the preamplifier, as this way only one input transistor contributes to the thermal noise. However, after a first order evaluation of the substrate and supply noise, a differential input amplifier was chosen for better rejection of these noise sources.

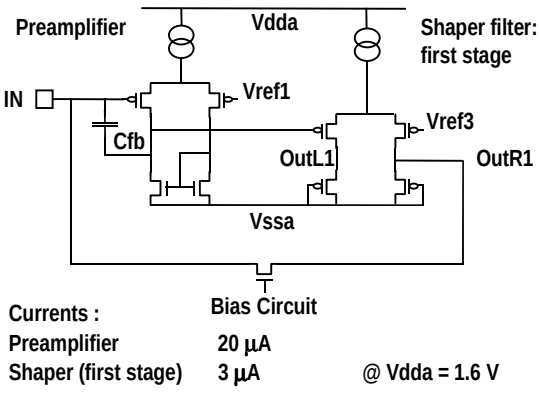

Figure 3: Simplified schematic diagram of the preamp, first shaping stage and high frequency feedback.

The preamplifier output is fed into a first shaping stage and one output of the shaper drives a transconductance feedback stage, as illustrated in Figure 3. This stage is realized using a NMOS transistor operated in the weak inversion region with a dedicated bias scheme.

If we neglect the rise time of the preamplifier, the poles of the closed-loop system are the roots of the second order equation:

$$s^2 \tau_{p2} \tau_{fb} + s \tau_{fb} + 1 = 0 \qquad (1)$$

where the time constants are those defined in Figure 2. For the real design the rise time of the preamplifier had to be taken into account to obtain correct values for the closed-loop system poles, thus leading to a more complex third order equation.

If τ_{fb}=20ns, τ_{p2}=5ns and τ_r=1.5ns, $p_{1\text{-}2}$=80±50j Mrad/s is obtained for the closed loop poles in the Laplace σ-jω domain, as illustrated in Figure 4.

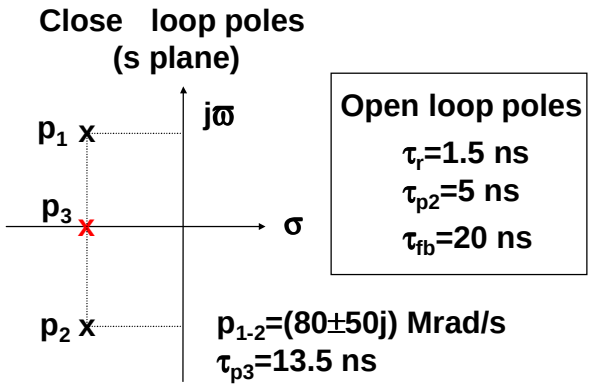

Figure 4: Position of the closed loop poles in the Laplace σ-jω plane.

An important issue to address is the sensitivity of the position of the closed loop poles to the position of the open loop poles. In the ideal case this sensitivity is infinity if the three poles are all real and coincident. A little mismatch in the position of the open-loop poles could then move the closed loop poles far from their ideal position. In particular, it is important to prevent the two complex poles from becoming real because this would degrade the circuit performance. So, although many requirements would call for complex poles closer to the real axis (e.g. noise and return-to-zero time), we decided to push the poles far into the complex plane.

This front-end was chosen instead of a standard charge integration and pole-zero cancellation scheme because of the large occupancy of the LHCb experiment (~8%). This leads to a high hit rate on the individual pixels, and could easily saturate a standard charge integrator with a very slow return to zero (pile-up effect). For this front-end, with the inclusion of the complex

poles, the next hit on the same pixel can be processed after less than 200ns.

B. The second shaping stage

The second shaping stage adds a third pole equal to the real part of the two complex poles τ_{p3}=13.5ns. This tunes the peaking time to 25ns and adds more shaping to further reduce noise.

The total input noise has been estimated to be lower than 200e$^-$, with the contribution of the flicker noise being negligible. In addition, for this pole configuration, the ideal transient response of the front end does not show any undershoot for any value of the imaginary part of the two complex poles.

A low frequency feedback stage compares the differential shaper output to a pre-set imbalance (corresponding to the pixel charge threshold) and injects a feedback current into the preamp input which corrects both for shaper output offset and for detector leakage current. This, together with the second stage of shaping, is shown in Figure 5.

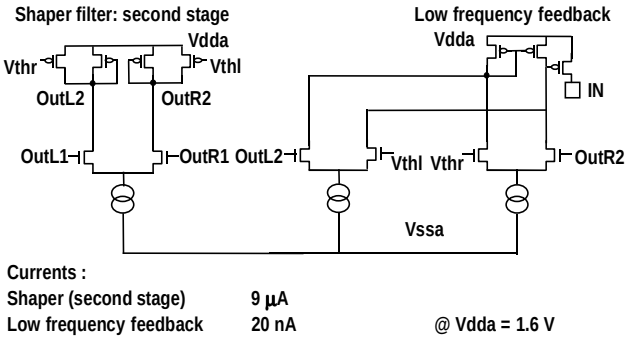

Figure 5: Simplified schematic diagram of the second shaping stage and of the low frequency feedback.

The simulated output waveforms of these three stages of the front-end are shown in Figure 6.

The input signal is 5000e$^-$, which is the typical input signal for LHCb application. The threshold imbalance is set to 20mV, and this is why a differential offset is present at the output of the second shaping stage.

Figure 6 shows that both the preamplifier and shaper have returned to zero ~150ns after the hit and with only a small undershoot.

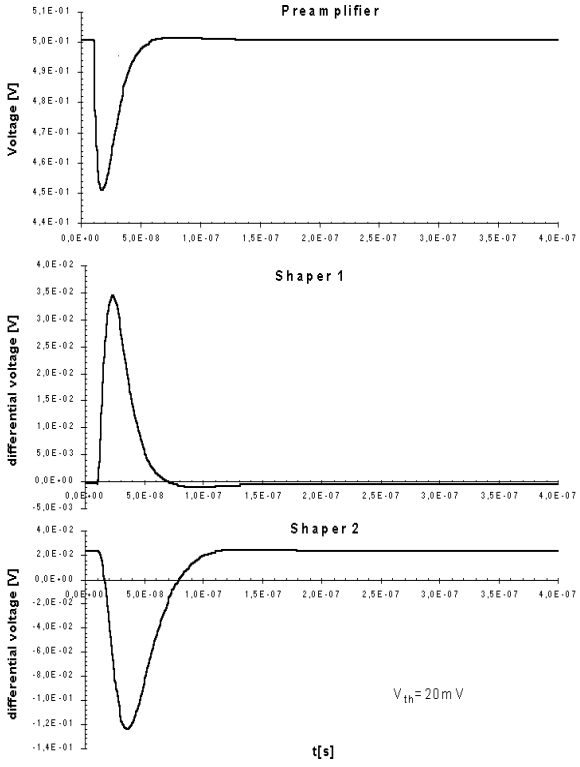

Figure 6: Plots of the simulated output waveforms of the three stages for the typical signal of the LHCb experiment (5000 e$^-$).

C. The discriminator

The shaper differential output feeds into a discriminator, which transforms the analog pulse into a digital signal. A block diagram is shown in Figure 7. The discriminator input stage is an OTA, which makes a voltage-to-current conversion. The discrimination is then performed in current mode by the subsequent non-latching current discriminator. The outgoing voltage pulse is then squared and adapted to the correct digital voltage levels. A NAND gate is used to mask the pixel in case of malfunction or excessive noise.

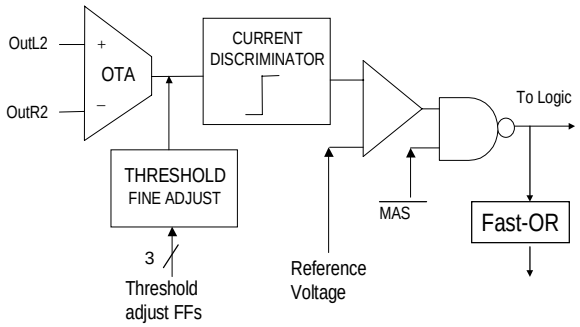

Figure 7: Block diagram of the discriminator with the three bit threshold fine adjust.

The outputs of the discriminators in the pixel matrix provide a fast-OR signal which is foreseen for diagnostic purposes during testing or for self-triggering.

To increase pixel-to-pixel uniformity and decrease threshold dispersion, a 3-bit register and corresponding digital-to-analog convertor (DAC) are used in every pixel to finely adjust the pixel charge threshold. The nominal threshold adjust range is ~960 e^-, but it can be adjusted by means of a DAC.

To avoid hit loss, the effect of time-walk has to be minimized. This is due to the different response times of the discriminator to input signals of different amplitudes. Additionally, consideration has to be given to time-of-flight delays of signals up the pixel columns, which are of the order of a few ns. These must be included in the time-walk optimisation. If we define the time-walk as the charge over threshold needed to trigger the discriminator 20ns after it is triggered by an infinitely large input pulse, the simulations performed indicate a time walk of ~200e^- at a threshold of 1500e^-. This 20ns limit gives a 5ns contingency to accommodate time-of-flight delays given that the required timing resolution is 25ns.

Finally, every pixel can be addressed individually for testing. The content of a test flip-flop in each pixel determines whether or not an analog input signal is applied to the pixel front-end.

The total discriminator power consumption is about 10 μW.

IV. LAYOUT

The size of the front-end is 50 μm × 125μm, as indicated in Figure 1. The circuitry to store the pixel configuration, which is not clocked during data-taking, is placed to the left of the front-end to provide some isolation from the noisy digital circuitry of the neighbouring column. On the right-hand side of the front-end, isolation from the digital circuitry is achieved by the use of guard rings and careful separation of the power supplies. The over-all size of the chip, together with the mechanical constraints imposed by the ALICE ITS, means that all six layers of metal offered by the technology are used. This was necessary to minimise the voltage drops on the power and bias lines. The first two layers are used for local interconnect and the third for bussing, leaving the top-most three layers for power supplies and biasing.

Capacitors made from the polysilicon gate capacitance are used in the pixel cell and also on the periphery of the chip for decoupling purposes.

V. BIAS CIRCUITRY

The biasing of the front-end is carried out by an array of DACs arranged on the periphery of the chip. These provide both voltage and current references across an 8-bit range [10]. They are constructed from a current DAC together with an output stage to tune the range to the requirements of the particular bias or to make a current-to-voltage conversion which is robust against power supply and transistor parameter variations. Those voltage biases which are sensitive to resistive drops across the width of the chip are distributed individually as currents to each column, and the current-to-voltage conversion takes place at the bottom of the column. This avoids any systematic column-to-column variations in biasing.

VI. THE LOGIC

In the digital part of the pixel [11], the discriminator output is firstly synchronized to the clock. The next stage consists of two digital delay units, whose purpose is to store a hit for the duration of the trigger latency. The delay can be set in multiples of the clock period to meet the requirements of the experiments.

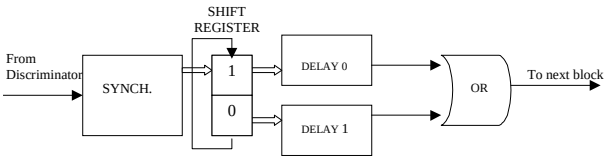

Figure 8: Schematic block diagram of the first logic section (synchronization and delay units).

The result of the trigger coincidence is loaded into the next-available cell of a 4-event FIFO which acts as the multi-event buffer and de-randomizer. This FIFO is read-write addressable by means of two 4-bit busses which carry Gray-encoded patterns. The content of the FIFO cells waiting to be read out are loaded into a flip-flop by the Level-2 Trigger in ALICE or Next-Event-Read in LHCb. The flip-flops of each column form a shift register, and data are shifted out using the system clock.

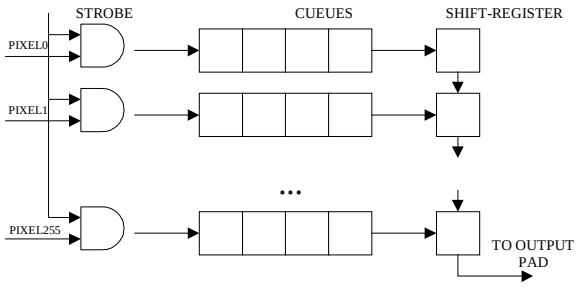

Figure 9: Schematic block diagram of the second logic section (strobe coincidence, FIFO and read-out latches).

Finally, there are five latches inside the cell, whose contents switch on or off the test input to the front-end, mask or activate the pixel, and provide the three bits of threshold adjustment.

Much attention has been paid to reducing the risk of noise injection via the substrate. In addition to the extensive use of Gray encoding and the differential front-end, the logic cells used in the pixels are current starved,

to minimize any bounce in the power supplies during switching. To increase radiation hardness, all the flip-flops that control the state of the chip are SEU hard [12].

VII. Operational modes

With the addition of some extra logic, this architecture can be used for both applications. The mode of operation is selected by an external control signal.

A. ALICE mode

In this mode, each pixel cell acts as an individual channel and the full matrix of 256x32 cells is read out. Using the two delay units, each cell has the capability of simultaneously storing two hits for the trigger latency. The 32 column are read out in parallel using a 10MHz clock.

B. LHCb mode

In LHCb mode, eight pixels in the vertical direction are configured as a "super-pixel" of 425 μm × 400μm, reducing the matrix to 32 × 32 cells. The discriminator outputs of the super-pixel are OR- ed together and the sixteen delay units of these eight cells are configured as an array. Four of the 4-event FIFOs are connected together to form a 16-event FIFO, which can be written to by any of the sixteen delay units. The FIFO output is loaded into the flip-flop of the top pixel in the group, which bypasses the other seven during read-out.

VIII. Conclusions

A new front end for pixel readout has been designed. The closed loop response contains three dominant poles of which two are complex and the third is real. This pole constellation was used to obtain a fast return to zero of the front-end and to avoid pile-up in high occupancy environments. This front end has been implemented on an 8192 channel readout chip designed to serve both the ALICE pixel detector and the LHCb RICH detector where it would be encapsulated inside a hybrid photon detector. This chip was designed in a commercial 0.25μm CMOS technology using special layout techniques to obtain radiation tolerance.

IX. References

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