THE DEVELOPEMENT OF THE CAFE-P/CAFE-M BIPOLAR CHIPS FOR THE ATLAS SEMICONDUCTOR TRACKER

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Abstract

A bipolar chip has been developed to provide the front-end functions of the binary readout architecture used for the silicon strip detectors in the ATLAS Semiconductor Tracker (SCT). This chip consists of 128 channels of low noise amplification and discrimination and provides an interface to a suitable CMOS data processing chip. The chip was successfully fabricated on the Maxim CB-2 process. Preliminary results including channel-to-channel matching, stability, noise, gain, and irradiation tolerence are presented. These results are compared to the previous CAFE-M chip and the ATLAS requirements.

1. INTRODUCTION

One solution for the baseline ATLAS SCT front-end electronics[1] is the bipolar – CMOS combination of the CAFE-P/ABC ASICs [2,3]. The CAFE-P is the most recent in the CAFE (Comparitor Amplifier Front End) series of chips deleveloped at UC Santa Cruz and Lawerence Berkeley National Laboritory. We discuss below the evolution of the CAFE design to meet the challanges of the ATLAS requirements, and the need for radiation tolerence in the hostile LHC environement. Preliminary data from the Cafe-M and Cafe-P are presented.

2. GENERAL CAFE ARCHITECTURE

The chips consists of 128 parallel channels of four stage amplifiers Each channel has a single ended input to a charge sensing pre-amplifier, followed by a shaping stage (15 ns), a second stage amplifier, and finally a differential comparitor. A common threshold is applied to the comparitor of all channels via either a dc current input from the ABC chip, or an externally applied differential voltage pair. Each comparator then yields a current output of aproximately 130uA for all signals above the applied threshold (‘hit’) and 1uA for those below threshold (‘no hit’). Reference currents for the ‘hit’/’no hit’ conditions are output for use by the ABC chip.

To simplify testing, a calibration circuit is provided by which test pulses may be injected into each channel of the pre-amplifiers. Four inputs are available from which these pulses may be provided externally, each to one forth the channels. In addition, an on chip chopper circuit is available which can be strobed from the ABC and will generate an internal test pulse in the CAFE. The magnitude of the internal pulse is set via a dc current from the ABC, and the channel selection by two voltage controlled inputs set by the ABC.

A constant current reference source (IDAR), has been provided to produce a stable current input to the ABC chip. Scaled portions of this current are then fed back to the CAFE chip to provide the threshold, and calibration pulse amplitude as mentioned above, as well as a third current which provides an adjustment for the pre-amplifier bias.

The layout consists of two rows of input pads on a 96um pitch, and three output rows to match the ABC. Power and servicing pads are redundent on both sides of the chip and routed through to the center of the chip before being supplied to the individual channels. This minimizes voltage drops across the chip and adds reliability in the event of bonding failures.

The 23 mm^2 die (Fig 1.) were manufactured with the MAXIM bipolar CB-2 process on 6” wafers. While this process has not been explicitly qualified as radiation resistent, it is inherently tolerent. Care was taken to design and simulate circuits that are tolerent with resistor increases of up to 90%, and β’s down to 20 while still biasing correctly.

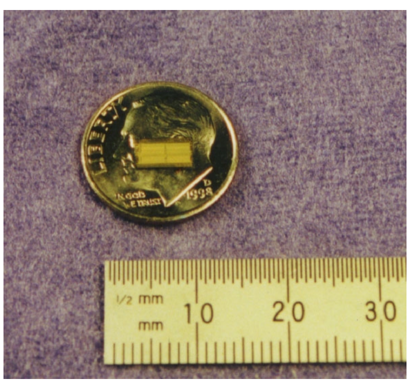

Figure 1, The ATLAS SCT CAFE-P.

The ‘M’/‘P’ versions of the CAFE chip primarily refer to the polarity of the input charge collected from the silicon detectors. The general layout and functionality is the same for both chips. The ‘M’ version was produced one year prior to the ‘P’ variety using the same process. Data presented below includes results from both versions of the CAFE.

3. PERFORMANCE & RESULTS

We have tested a large sample of CAFE-M and CAFE–P chips, both on wafer and mounted on a selection of hybrids and modules, to characterize their performance. Irradiations were performed on chips using the LBL 88” cyclotron providing 55 MeV protons, as well as with γ’s at UC Santa Cruz. Results for an eqiv. 17 Mrad ionizing dose are presented bellow.

3.1 ATLAS Requirements

Specifications have been set on the performance of the ATLAS SCT front end electronics which include:

- Low noise (<1500e with irrad detector)
- Excellent Threshold Uniformity. (<4% at 1fC)
- Low Power (<2mW/ch)
- Radiation Tolerant (10 LHC years)

The radiation hardness requirments of the CAFE chips are set by the levels expected in the SCT after 10 years of LHC operation. The chips are expected to function after levels which are projected to reach 10 Mrad of total ionising dose and $2x10^{14}$ n/cm^2 of 1 MeV equivilent neutron fluence for the displacement damage.

3.2 Support Circuitry Results

- IDAR Stability

The current source IDAR is fundimental to the operation of the CAFE chips, as it provides the scalable current for the threshold, pre-amp bias, and calibration amplitude. We find that IDAR is extreemly stable with respect to bias voltage variation (Fig. 2), supply voltage (< 0.3 %) , temperature and irradiation (Fig.3)

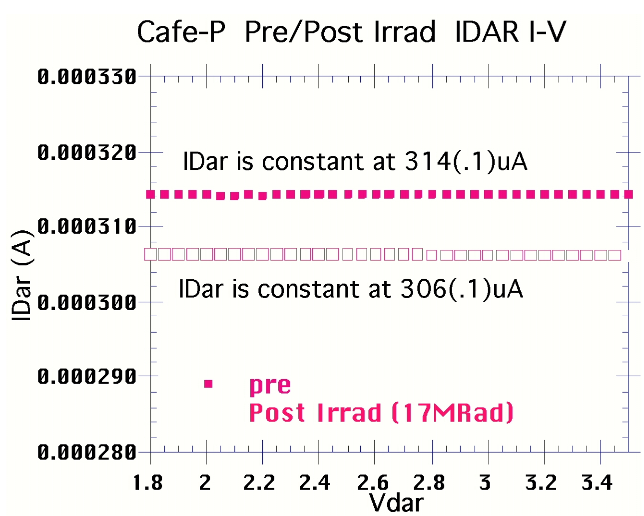

Figure 2, Pre and Post irradiation variation of IDAR current with respect to bias voltage. Showing 3% drop in output current.

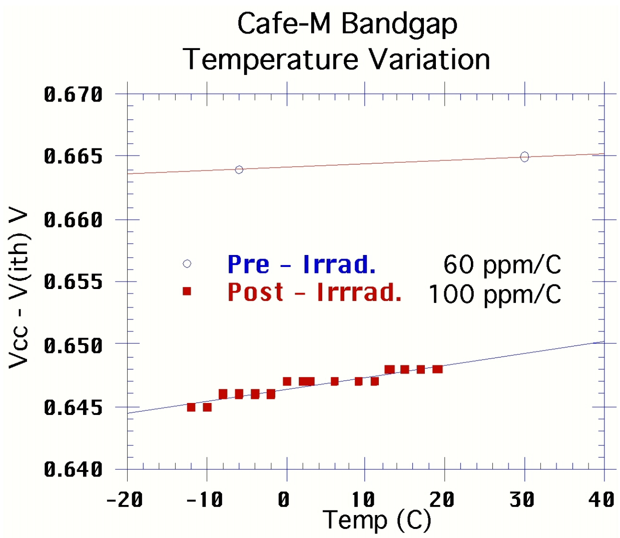

Figure 3, IDAR temperature dependence. IDAR output is coupled directly to Ith input.

- Ith, Cali Linearity

The post irradiation linearity of the Ith generated threshold and Cali generated calibration amplitude are shown below in figures 4 and 5. An allowable threshold range of 0-700 mV is obtained and a maximum deviation of 0.6 mV over the 0.5 – 3.0 fC range of interest. The Cali circuit shows a 0 – 9 fC range and a maximum deviation from linearty of 0.03 fC over the region of 0-3 fC. In both cases we find excellent post irrad. functionality and < 0.5% change from the pre irrad. slopes, and thus the combined IDAR/Ith and IDAR/Cali circuits should prove radiation tolerent.

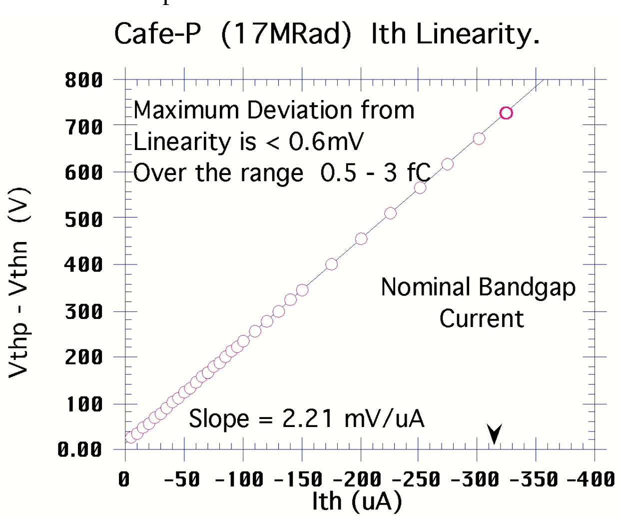

Figure 4. Post Irradiation linearity of Cafe-P Ith linearity. Applied threshold measured as the difference from Vthp and Vthn. Maximum setting is nominal bandgap current of 314 uA

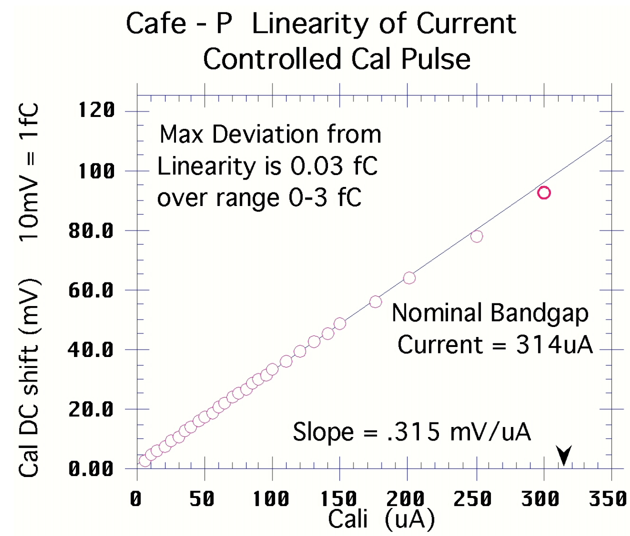

Figure 5, Linearity of the Cali generated calibration pulse amplitude. The DC shift observed on the cal0 bus is a measure of the pulse generated when the Cal strobe is driven by the ABC.

- Other Support Circuitry and Power Draw.

We observe a 15% drop in the output current of the ‘hit’ state of the comparator after irradiation. This should not be a problem as it is within the spec of the ABC input tolerence. No other problems in any of the other support circuitry have been identified, however, many of these functions (such as the internally generated calibration strobe) require the addition of the full ABC to test. This work is in progress.

Figure 6 shows the total current draw on Icc as a function of the supply voltage and the pre-amp bias current. For nominal settings of Vcc=3.5 and Viset = 200uA the total power draw is 1.5 mW/ch which is within the ATLAS specification.

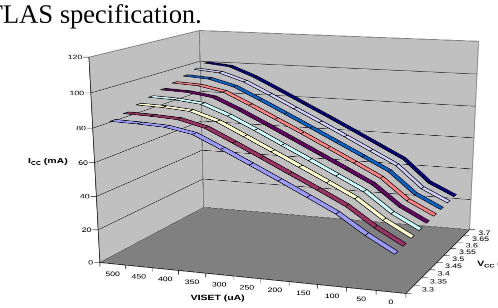

Figure 6. Pre-Irradition Icc current draw for allowable ranges of supply voltage (Vcc) and pre-amp bias current (ViSet).

3.3 Response and Uniformity

The ABC chip was not available at the time of this testing. All the following results were obtained with the CDP chip developed previously for SSC applications, and should not adversly effect the measurements. Calibration pulses and thresholds were set externally.

Prior to irradiation, the CAFE-M exhibited excellent amplifier performance [4]. However after irradiation a dramatic degregation in channel to channel matching, from 4% (1 σ variation across a single chip) to 25% was observed. This unacceptable uniformity was evident in the dispersion of the channel offsets in a typical response curve (Fig. 7), while the differential gain remained uneffected. Further measurements revealed the problem arose from large resistor increases, and decreases in β (> 50%) of the pre-amplifier circuit, which caused the base current to change. This manifested itself in dc voltage variations at the input to the comparator.

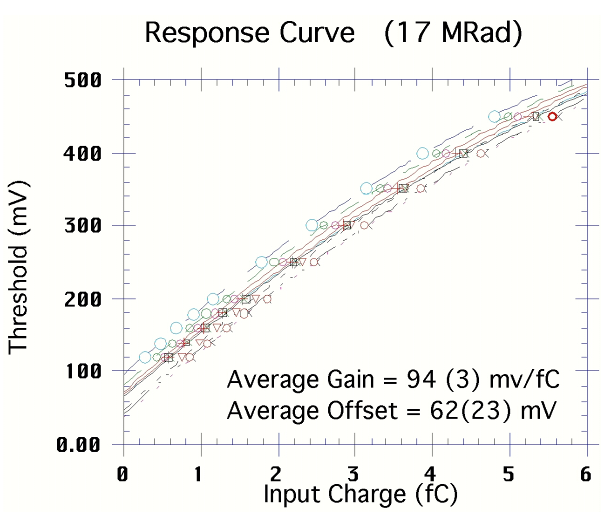

Figure 7, Response curve for post-irradiation CAFE-M showing many channels. Large variation in offset produces 25% uniformity at 1fC. Gain uniformity remains excellent both pre and post irrad.

To improve the post irradiation uniformity, the CAFE-P chip included a compensation circuit which corrected for the large resistor changes. In addition, the dynamic response was increased (~180 mV at 1fC) which gives a greater sensitivity to the threshold setting. The CAFE-P post irradiation response and uniformity are shown in figures 8 and 9. We see better than 4% uniformity at the nominal ATLAS threshold (1fC) after irradiation.

3.4 Noise and Module Stability

There was no observed difference in the noise and stability performance of the CAFE-M and CAFE-P. Figure 9 shows the noise for an irradiated Cafe-P chip with unloaded inputs. We measure ~750e noise, which is only slightly greater than the 700e found pre-irradiation.

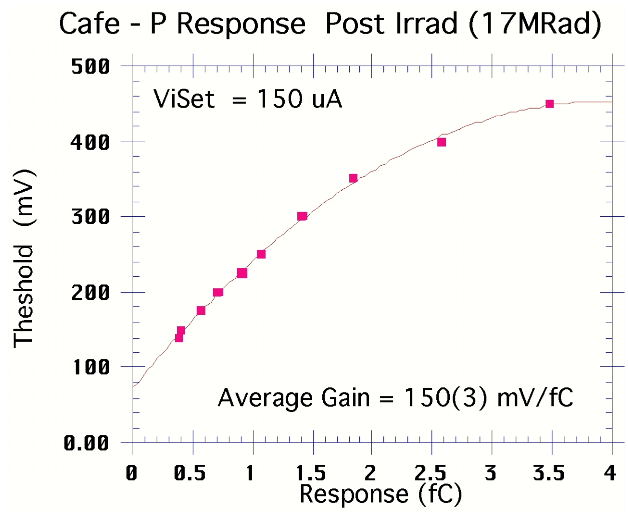

Figure 8, Response curve for post-irradiation CAFE-P averaged over all channels.

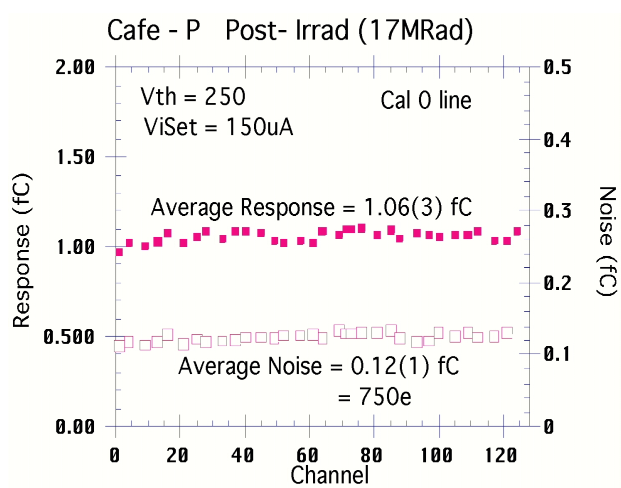

Figure 9, Individual channel response and noise for a 1fC threshold when input charge is sweeped for calibration line 0. We observe better than 4% matching post irradiation, and acceptable noise performance.

With a single die on a hybrid, and no load on the input channel we find that the CAFE-P exhibits no sign of oscillation above a threshold setting of ~0.2 fC. A 6 chip set module (CAFE-P- CDP) with typical ATLAS P-type detectors was then constructed to study the stability and noise performance of a more complex system.

Figures 10 and 11 show the response and noise at 1fC threshold for the module. Chip 6 (channels 640-768) is the same CAFE-P for which the previous irradiated measurements in this paper where obtained. All other CAFE-Ps are not irradiated. Chips 5 and 6 where also connected to the 12cm detector. Again we observe excellent uniformity at 1fC across individual chips, less than 2% for the non-irradiated CAFE-Ps and aproximately 4% for the irradiated chip. We also see good response uniformity across the entire module with the exception of chip 1 which has a small (15mV) threshold offset. For this module, a single threshold was applied for the entire module. With the ABCs we will have individual threshold control for each chip so this threshold shift will not appear

The noise performance for the CAFE-Ps not connected to detector channels is in agreement with previous measurements. The two chips connected to a detector show 1300 and 1400e noise for the unirradiated and irradiated chips respectively. This is well within the ATLAS required noise performance with 12cm detector.

The module was stable down to a threshold of aproximately 0.3 fC which is slightly greater than observed with a single chip, but well within the acceptable performance range.

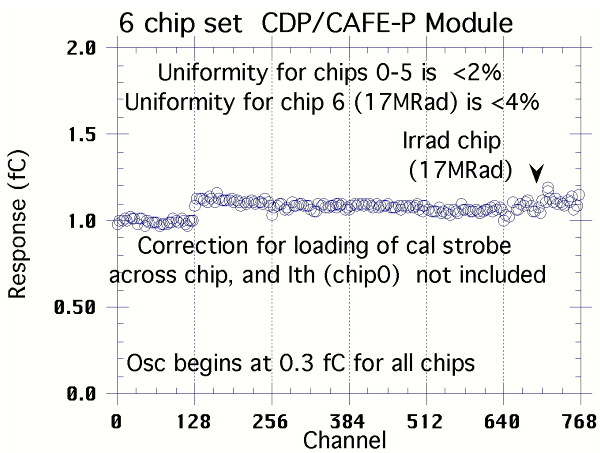

Figure 10, Individual channel response for post-irradiation CAFE-P/CDP 6 chip module. Channels 640-768 are for an irradiated chip. A single threshold was applied to the entire module. Chip 0 shows a small threshold offset.

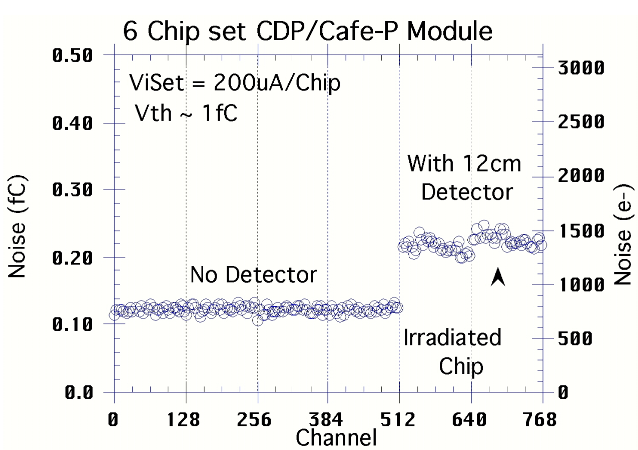

Figure 11, Individual channel noise for post-irradiation CAFE-P/CDP 6 chip module. Channels 512-768 are connected to an ATLAS 12cm p-type detector.

4. CONCLUSIONS

We have presented preliminary results that show the CAFE-M chip functionality meets the major requirements requirements of power, uniformity, noise and stability, but failed to be radiation tolerent. An adjustment to the circuit was made, and the CAFE-P appears more radiation tolerent while preserving excellent functionality within the ATLAS specifications.

Work continues on the same detailed characterization of the CAFE-P which was completed for the CAFE-M and presented at the SCT week. To date, we have found no significant problems. Further studies with the recently completed ABC [4] are underway, and full prototype module construction are planned. Preliminary wafer sorting shows we are obtaining yields of perfect chips near the 75% level.

REFERENCES

1. ATLAS TDR 5, Inner Detector Technical Design Report, Vol. II, CERN/LHCC/97-17, 30 April 1997.

2. N. Spencer et al., Project Specification-CAFE-P V4.01,

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4. M French et al., “Development of a Rad-Hard CMOS Chip for the Binary Readout of the ATLAS Semiconductor Tracker”, this Proceedings.