DETECTOR AND FRONT END ELECTRONICS FOR ALICE AND STAR SILICON STRIP LAYERS

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Abstract

Detector modules consisting of Silicon Strip Detector (SSD) and Front End Electronics (FEE) assembly have been designed in order to provide the two outer layers of the ALICE Inner Tracker System (ITS) [1] as well as the outer layer of the STAR Silicon Vertex Tracker (SVT) [2]. Several prototypes have been produced and tested in the SPS and PS beam at CERN to validate the final design. Double-sided, AC-coupled SSD detectors provided by two different manufacturers and also a pair of single-sided SSD have been associated to new low-power CMOS ALICE128C ASIC chips in a new detector module assembly. The same detectors have also been associated to current Viking electronics for reference purpose. These prototype detector modules are described and some first results are presented.

1. INTRODUCTION

The ITS includes 1706 SSD modules, i.e. about 2.6 Millions analog channels for 5.4 m^2 of surface and the SVT 320 SSD modules, i.e. about 0.5 Million analog channels for 1 m^2. All modules are identical in size and characteristics.

The 75x42 mm double-sided SSD includes 768 AC-coupled strips on each side. Global tests on leakage current and capacitance are performed on a probe station, as well as coupling capacitance measurements for each strip.

The analog readout of the detectors is performed by means of the ALICE 128C readout chips designed by the LEPSI at Strasbourg [3], [4]. The specific characteristics of this chip relate to a very low power consumption, on-chip remote control and tuning facilities. Its specifications have been presented earlier and the measured electrical characteristics are [illegible] [5] in this [illegible] performed at each assembly step. Statistical information is subsequently provided.

The prototype modules used for the tests are equipped with standard hybrids, fan-in on glass, and wire bonding. Signal/Noise ratio (S/N), resolution and charge matching are measured. The proposed final connection and packaging technique using TAB is presented in another paper by S.Bouvier [6].

2. SILICON STRIP DETECTORS

Three supplies of detectors have been tested. They have the same 75x42 mm overall size and the same 300 µm thickness for double-sided SSD or twice 150 µm for a pair of single-sided SSD. They have also the same general geometric layout: 768 strips on each side, no floating strips, 95 µm pitch, 25 µm to 30 µm strip width, stereoscopic angle of ±17.5 mrad, guard ring width ≤ 1 mm, double bonding pads on each strip end. Thus, they can be used with the same fan in, the same hybrids and the same connections (figure 1).

Figure 1: P side of the detector
(simplified layout in full size).

They have also the same biasing technique (punch thru on both sides) and the same electric specifications: depletion voltage ≤ 60 V for 300 µm bulk thickness

5 µA, strip leakage current ≤ 5 nA and guard ring leakage ≤ 5 µA.

Differences between detectors relate to the resistivity of the material (≥ 6 kΩ.cm), the inner design techniques, the manufacturing processes, and the strip width which is defined as to provide a "coupling capacitor / parasistic capacitors" ratio ≥ 20 for each strip in order to limit the crosstalk. Typical coupling capacitor value is 150 - 200 pF as on figure 2. One can notice a shortened capacitor on the left, and a slope on the very right side corresponds to the shorter strip area.

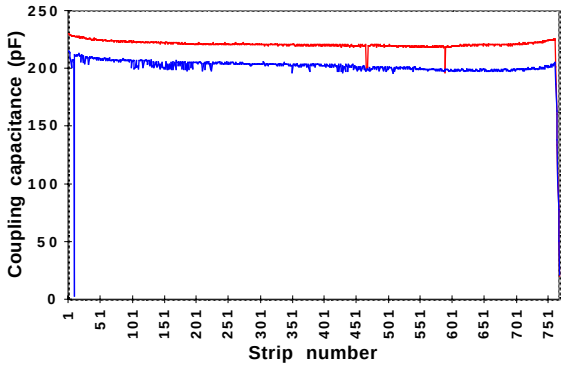

Fig. 2 : Measured strip coupling capacitance side P/N

3. READOUT CHIPS

Reference readout electronics use standard IDEA hybrids equipped with standard VA2 chips. Peaking time is tunable around 1.6 µs, dynamic range is 4 MIPs and nominal ENC is 135 e^- + 12.3 e^-/pF [7].

The new readout electronics uses the ALICE128C 128 channels chip designed with the AMS 1.2µm CMOS technology. The die size is 6 mm x 8.5 mm [3]. Each channel amplifies, shapes and stores as a voltage signal onto the capacitance C_{HOLD}, the charge collected on a strip of the detector. The shaping time (τ_s) is adjustable from 1.4 µs to 2 µs. The dynamic range extends to more than ± 12 MIP. Nominal ENC is 290 e^- + 8 e^-/pF. Power supply is ±2 V. Special attention has been taken to power consumption which is always below 850 µW/channel and drops down to 340 µW/channel for a 1 ms readout cycle. An analog multiplexer allows a sequential readout of the data at a rate of up to 10 MHz through a tristate output buffer shared by the 128 channels. The output buffer has been designed to drive an external link with a 100 Ω characteristic impedance in parallel with a capacitance of up to 20 pF. A slow control mechanism implementing the " JTAG IEEE1149.1 " protocol biases the different analog blocks and tunes the shaping time [8]. It also controls an internal test pulse generator which provides a variable current pulse emulating a deposited charge up to ±11 MIP. The channels, where the pulse has to be injected, are capacitances in a normal readout cycle or select one particular channel through the output shift register to visualize, in "transparent" mode, the shape of the signal at the output of the shaper in order to measure/set the shaping time. Of course, the pulse generators have to be calibrated for characterization use. All the different testing configurations and the pulse level, i.e. all the registers, are addressed by means of the JTAG controller.

4. HYBRID

The prototype hybrid has been made by a set of two thick printed circuit boards (PCB) which provide electrical connections and mechanical support for chips, detector, fan in, external componants and connectors to link it to the outside world for signals and power supply. It is presented in figure 3.

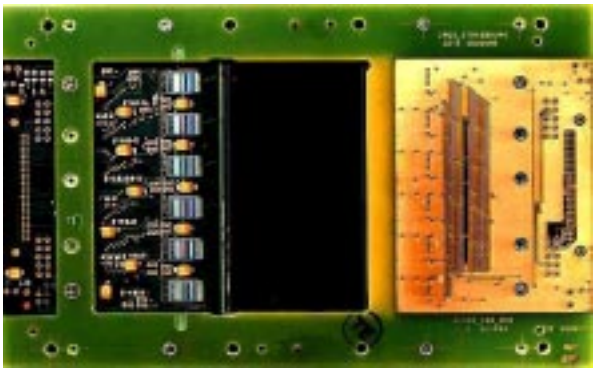

Fig. 3 : Hybrid assembly

All the PCBs are identical. Each PCB holds six ALICE128C chips for the readout of the 768 strips located on each detector side. Each board operates one detector side. Thus, two boards are needed for each double-sided detector or for a pair of single-sided detectors. They face each other in a symetric way but they are completely electrically insulated in order to be floated. Even with the very high coupling capacitor yield of the detectors (≥ 99%), we chose to float one side of the double-sided detectors in order to avoid depletion voltage to be applied across the capacitors. We can float any P or N detector side in order to evaluate the noise added by the opto-insulation (≥ 100 e^-). External components relate mainly to decoupling capacitors and current reference resistors.

5. BEAM TEST SETUP

The beam tests have been performed over three runs in May and June 1998 at CERN on the SPS accelerator with 125 GeV pions, and in August 1998 on the PS accelerator mainly with 10 GeV pions.

Figure 4 presents the detectors under test (DUT)

and timing reference information for charged tracks. The detector frame is equipped with 4 single-sided reference detector pairs having a readout pitch of 50 µm. They provide a spatial resolution of 1.4 µm per detector and a track extrapolation error lower than 1 µm in the center of the telescope.

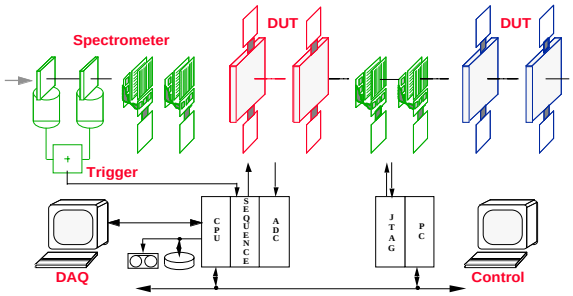

Fig. 4 : Beam test setup

The data acquisition frame located in the control room includes essentially the trigger electronics, a data acquistion VME crate with the Eurocom CPU, VME Sirocco ADC boards, and an acquisition sequencer board. Data are recorded on Exabyte cassettes. The acquisition program OS9DAS which runs under control of a terminal is based on Microdas software [11].

A PC running a LabView control program is interfaced with the DUT by means of a JTAG interface. It performs the detector control, i.e. it stores the operating FEE parameters (biasing, shaping time a.s.o.) and initializes the detector assembly. It is also in charge of hardware tests.

6. TEST RESULTS

For the detectors provided by two manufacturers C and E, the analysis is focused on signal over noise ratio on both sides, on charge matching result for the double-sided detectors and on geometric resolution. The S/N of the detector C with Alice128C readout is shown in figure 5 and the corresponding charge matching in figure 6. The S/N of the detector E with Alice128C readout is represented in figure 7 and the corresponding charge matching in figure 8. The pulse height ratio P/N is displayed in figure 9. For all detectors, the results correspond to side N floating.

6.1 ALICE128C chip on detector C

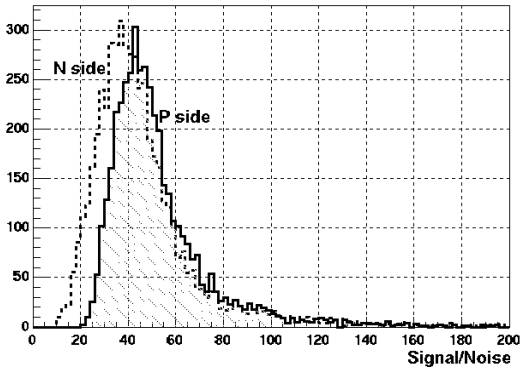

Fig. 5 : S/N detector C

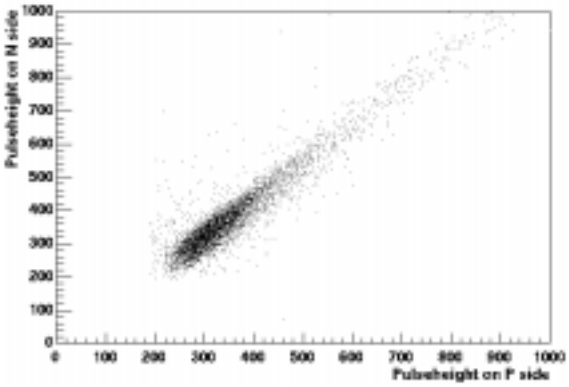

Fig. 6 : Charge matching detector C

6.2 ALICE128C chip on detector E

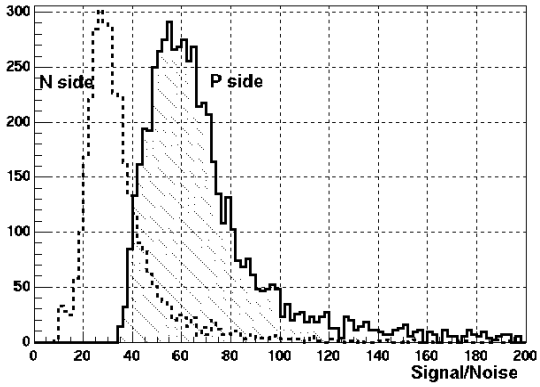

Fig. 7 : S/N detector E

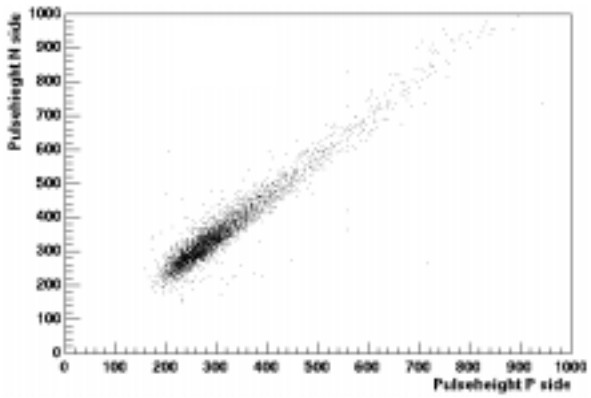

Fig. 8 : Charge matching detector E

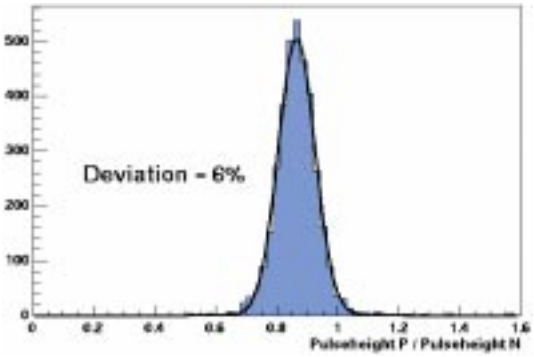

Fig. 9 : Charge ratio detector E

6.3 VA2 chip on detector C

The S/N of the detector C with VA2 readout is shown in figure 10 and the corresponding charge matching in figure 11.

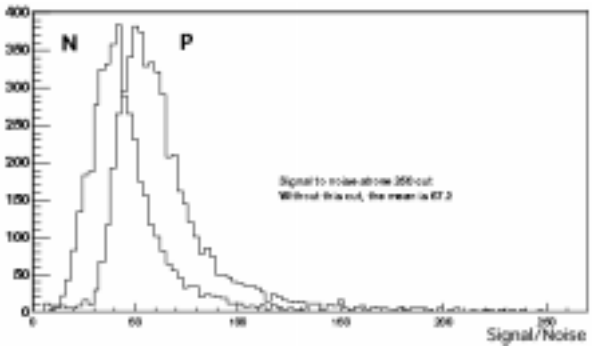

Fig. 10 : S/N detector C

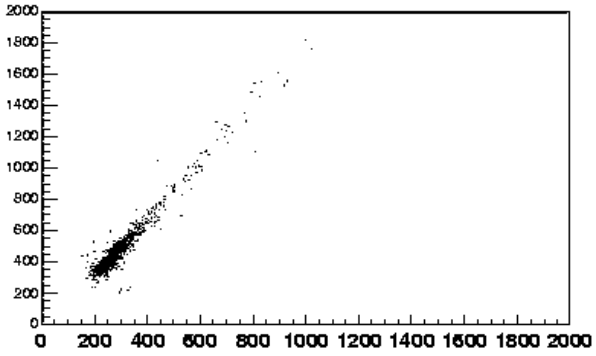

Fig. 11 : Charge matching detector C

The resolution is represented in figure 12 for the P side and in figure 13 for the N side. It is nearly detector and chip independant, only slightly related to the noise level. The nearly rectangular shape can be explained by the geometric characteristics of the detector which has a 95 µm wide pitch and no intermediate floating strips. The number of strips involved in a cluster is below 2. Thus, the distribution of perpendicularly arriving particles provides a resolution of 22 - 25 µm. This is slightly better than the geometric resolution value of the pitch over the square root of 12.

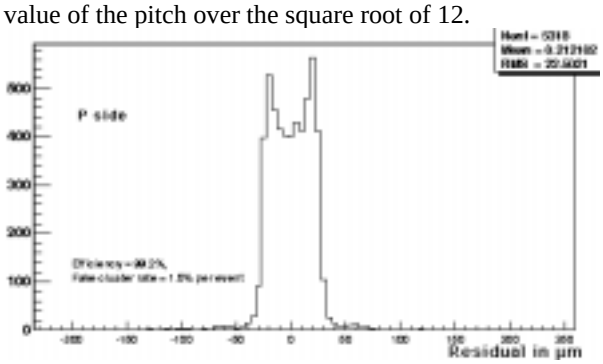

Fig. 12 : Resolution P side detector C

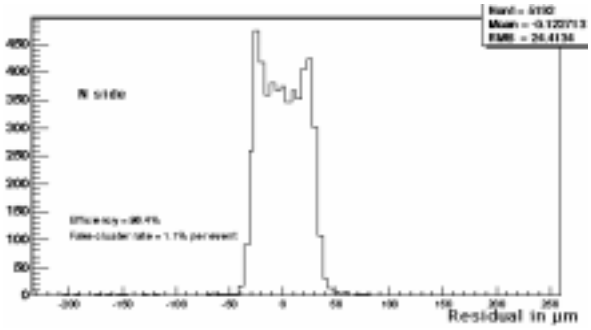

Fig. 13 : Resolution N side detector C

6.4 ALICE128C chip on SS detector

A set of two single-sided 150µm SSD has been glued back to back in order to provide a detector assembly with the same layout, size and total thickness as the double-sided SSDs. The front end electronics is

The main expected difference in characteristics besides the half depletion voltage is the S/N ratio of about 20 shown in figure 14. It is directly related to the thickness of each SSD. This measurement provides a valuable information on the possibility to reduce the thickness of the chosen double-sided SSD for the ALICE and STAR experiments.

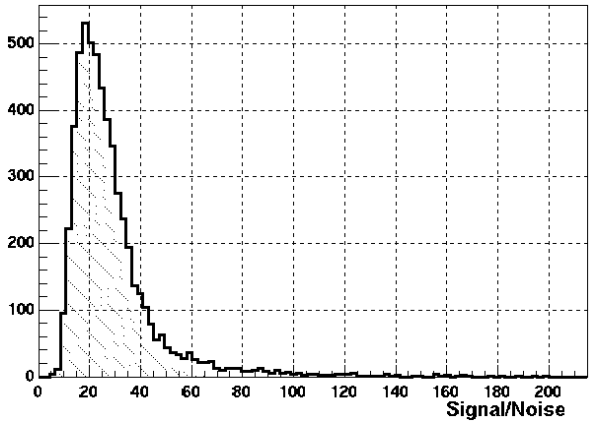

Fig. 14 : S/N single-sided detector 150µm thick

6.5 S/N DATA SUMMARY

The maxima of the S/N ratio distribution for double-sided detectors from the two different manufacturers (C and E) linked to either ALICE128C chips or VA2 chips are summarized in table 1.

Table 1: Signal / Noise summary for double-sided SSD

S/N	P side	N side
Detector C + VA2	55	40
Detector C + ALICE	45	40
Detector E + VA2	65	35
Detector E + ALICE	55	30

The N side S/N ratio is lower than the P side for two main following reasons: the strip insulation technique on the N side of the detector made by P spray and the need for floating electronics on one readout side. This latter request requires opto-insulation of the readout electronics on the chosen N side which adds some noise and thus reduces the S/N ratio.

ALICE128C chips provide S/N ratio lower by 10 units than VA2 chips. This must be related to the 3 time larger dynamic range and to a 4 time lower power consumption.

One can also notice that the detector of the manufacturer C provides a medium S/N, nearly balanced on both sides, whereas the detector of the manufacturer E provides a generally higher S/N ratio on side P and lower on side N.

7. TOTAL DOSE EFFECT AND LATCHUP

The total dose effect has been tested on the detector as well as on the ALICE128C chip on the Vivitron tandem accelerator with 20 MeV protons. These irradiation tests will be pursued soon. Preliminary results reveal an increase of the detector leakage current of about 80 nA/krad in a Alice detector test structure whereas the ALICE128C chip shows a decrease of the pedestal voltage of about 8.4 mV/krad (detector equivalent).

The latchup cross section of the ALICE128C chip has been defined. This cross section has a threshold at 5000 MIP and the overlapping area between the cross section and the expected energy loss spectrum in the chip is about to be evaluated by simulation.

8. CONCLUSION

The present results relate to several detectors of different kinds. All detectors were working. They provide interesting information but the statistics is too low to enable a reliable technical discrimination between the two manufacturers.

The difference between the two readout chips was expected and corresponds to a different design goal. Roughly, compared to the VA2 chip, the ALICE128C chip provides a 3 time expansion of the dynamic range and a much lower power consumption (down to 1/4) for a S/N ratio of less than 20% lower.

One concludes that the chosen detector layout and biasing technique provide a space resolution below the 27 µm recommended in the ALICE technical proposal.

The double-sided technique allows charge matching selction for ambiguous hits.

The ALICE128C chip demonstrates its ability to provide good data with reasonable S/N ratio. It allows drastic reduction in power, in cooling and in material by reducing the external components.

ACKNOWLEDGMENTS

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