

A Fast Pipelined Trigger for the H1 Experiment based on Multiwire Proportional Chamber Signals

*S. Eichenberger, H. P. Beck, S. Egli, K. Müller,
C. A. Meyer, P. Robmann, U. Straumann, P. Truöl*
Physik Institut, Universität Zürich, CH 8001 Zürich
M. Arpagaus, R. Bernet, R. Eichler, C. Grab, J. Riedlberger, T. Wolff
Institut für Mittelenergiephysik, ETH-Zürich, CH 8093 Zürich

Abstract

Based on a total of 1920 pads from two cylindrical and one planar double layer multiwire proportional chamber, the vertex position of ep collisions along the beam axis of the HERA storage ring is reconstructed. This allows discrimination between ep events, originating from the nominal interaction region, and background, introduced mainly by proton beam-pipe and proton rest-gas interactions. The trigger works in a pipelined manner, delivering a delayed decision every 96 ns, corresponding to the accelerator bunch crossing frequency. It employs custom designed gate arrays as well as XILINX logic cell arrays and a 16 MByte static RAM lookup table. Computer controlled debugging procedures take advantage of the reprogrammability of XILINX chips.

1 Introduction

The H1 detector makes use of a four level trigger scheme. The first level (L1) operates dead time free with a decision time of 2.3 μ s. Given the bunch crossing frequency of 10.4 MHz at HERA, this requires a pipelined design: synchronization of all trigger signals is needed every 96 ns along the trigger signal path. At the output, a trigger decision appears every 96 ns, uniquely related to a single bunch crossing 24 clock cycles earlier. A positive L1 decision stops all pipelines and starts higher trigger levels.

The aim of the herein described *z-vertex trigger* is to reconstruct the primary interaction vertex along the beam axis, the *z*-coordinate. It operates on the cathode pad signals of two cylindrical Multiwire Proportional Chambers (MWPCs) [1], situated around the beam axis, as well as one planar chamber, located in the proton direction from the interaction zone. In order to suppress synchrotron radiation influence, each chamber consists of two independent layers. The pad sizes are matched to the anticipated resolution of the vertex determination.

Figure 1 explains the basic principles of the trigger: a *ray* is defined as the coincidence of four MWPC pads, which can be connected by a straight line in the *r-z* plane. The number of such rays, which are active for any given bunch crossing, is entered into a 16 bin wide histogram, each bin being related to the origins of its respective rays along the beam axis. Inevitably, one also finds combinations not originating from a true particle trace. However, these 'wrong' rays generally produce a flat distribution in the histogram, whereas at the true vertex location a peak is found. Background events don't show this typical peak, as they mostly originate from interactions outside the nominal interaction zone (and the histogrammed area).

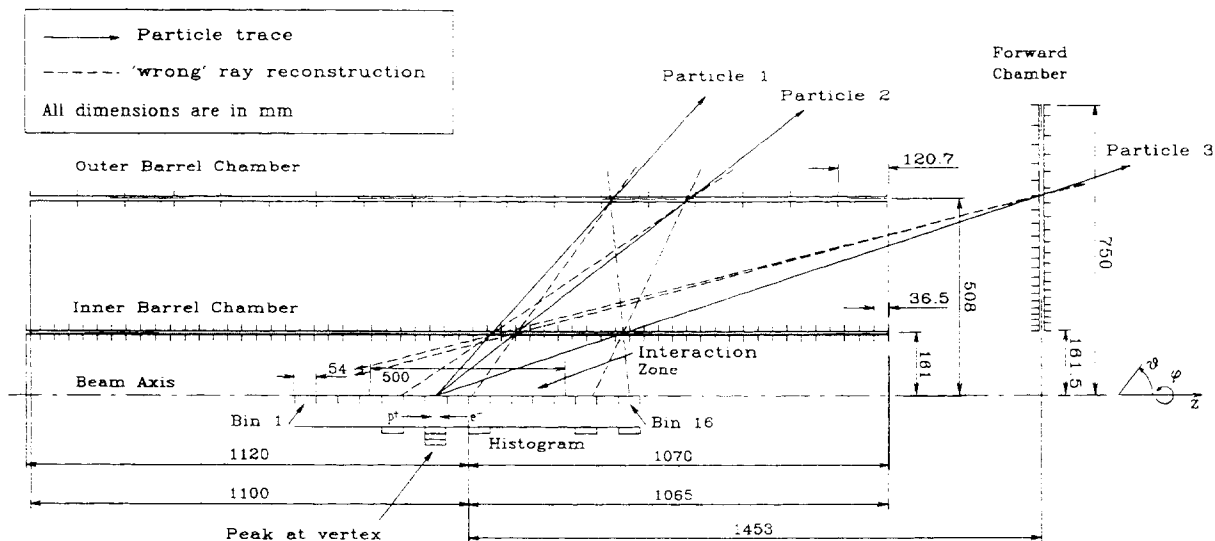


Figure 1 Vertex reconstruction by building a histogram, which displays a peak at the true vertex location.

The 16-fold ϕ -segmentation (around the beam axis) of the chambers corresponds to 16 independently built histograms, one for each segment.

2 Hardware Realisation

The MWPC pad signals are preamplified on the chamber and shaped, digitized and synchronized with the bunch crossing frequency on a *receiver card*. Input to the trigger are 1920 digital pulses of 96 ns duration, resulting in a dataflow of 1.9 GBit/s. The block diagram of the trigger logic operating on these signals is given in figure 2. A more detailed description is given in [2].

In the *rayfinder* electronics[3], the 16 histograms are built for the 16 ϕ -segments respectively. It is distributed over 256 printed circuit boards. Each of them builds one histogram bin for one ϕ -segment. A total of 2112 1.5 μ m CMOS gate arrays with 2200 gates each are used. For each bin some 120 rays are evaluated.

The 16 individual histograms for the 16 ϕ -segments are summed up in the *adder cards* to one 16 bin wide histogram. The *vertex finder* card extracts some significant numbers, including total number of entries and peak size, which are then passed as a 22..24 bit word to a static *RAM card*, which is operated as a lookup table.

Output are eight trigger bits, each programmable to different levels of peak significance. These bits are passed to the L1 central trigger logic, where a global trigger decision is derived, considering all other L1 subtriggers as well. The z-vertex trigger bits are available 15 HERA bunch crossing clock cycles after the initial interaction, marked as 'BC 15' in figure 2.

To maintain flexibility, the *adder* and *vertex finder* cards use reprogrammable XILINX logic cell arrays. They not only allow for future adaptations of the logic to new requirements, but also semi-automated circuit testing. Special programs have been developed, which allow scanning

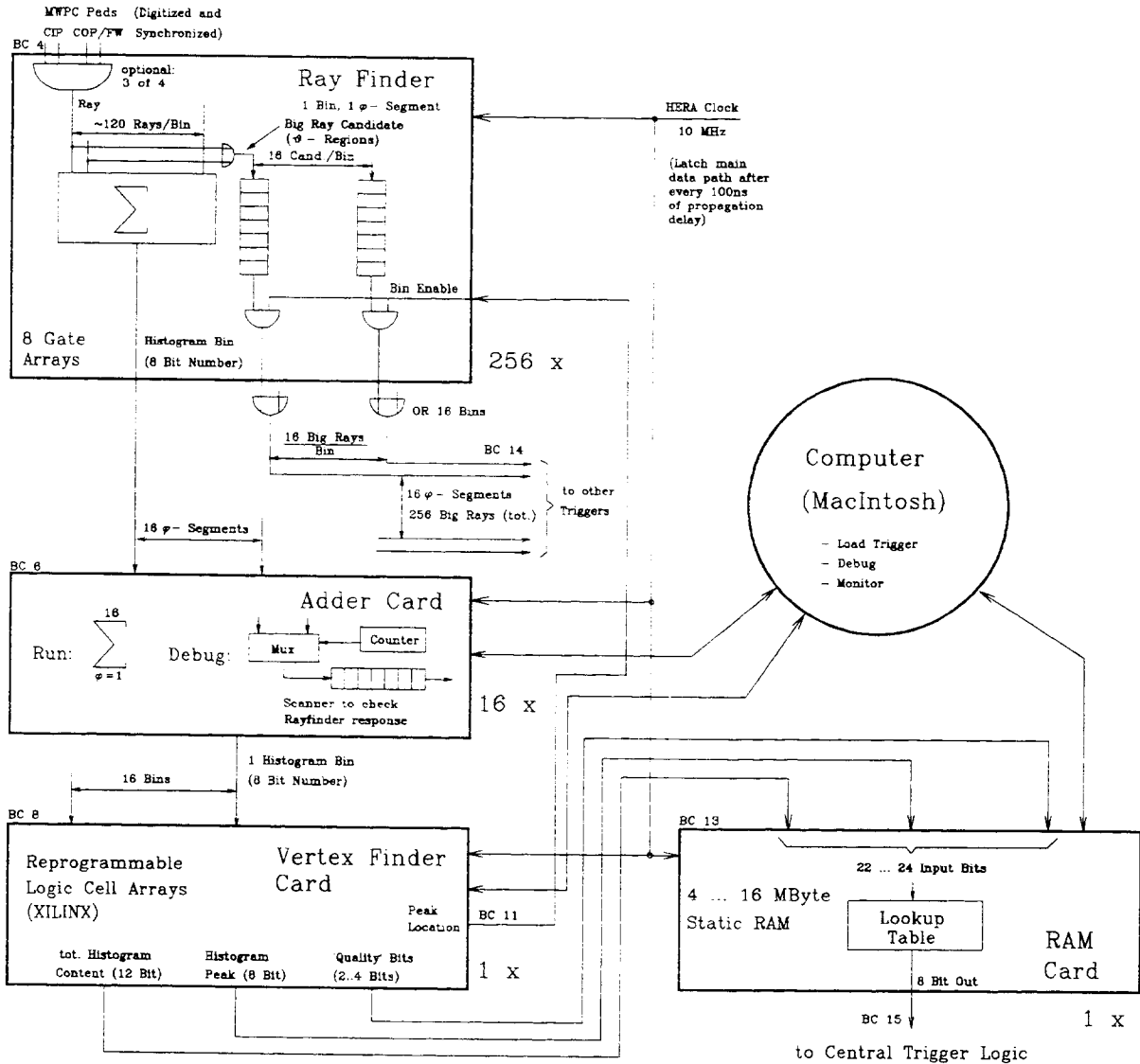


Figure 2 The block diagram of the *z-vertex trigger*

all XILINX input pins and making their signal states available to a computer, which then can deduce detailed bug reports on the *rayfinder* part of the electronics. These tools proved to be very helpful not only during the installation phase but also to monitor correct operation after interruptions such as power failures, etc.

3 First Experiences from HERA Run Periods

The trigger has been operational during all ep collision runs of HERA since startup. The main purpose of this trigger is to flag events, which do not deposit enough energy in the H1 calorimeter to be accepted by those triggers. They are mainly heavy quark events, which are not expected to be produced in great numbers with the presently available luminosity.

However, about half of the currently accepted events have a reconstructed vertex in the acceptance area of the histogram. The others are mostly rejected on the trigger level four filter farm. Figure 3 shows good agreement of the peak location in the *z-vertex histogram* with

the reconstructed vertex location along the beam axis for events accepted for DST tapes.

A driftchamber trigger[4], which is expected to become operational in autumn 1992, will help to restrict the radial distance of the vertex from the beam position as it will reconstruct charged particle traces in the r - ϕ plane. Operated in coincidence with the z -vertex trigger, this becomes a powerful tool to on-line reconstruct the primary event vertex. It will further reduce the trigger rate of currently about 15 Hz. This is necessary as soon as the HERA luminosity of presently some $10^{28} \text{ cm}^{-2}\text{s}^{-1}$ is increased to the design value of $10^{31} \text{ cm}^{-2}\text{s}^{-1}$.

It is also vital to correctly identify the bunch crossing at which a triggered event took place. Since the necessary time resolution of less than 96 ns is not inherent to many of the other L1 subtriggers of H1, a non-empty z -vertex histogram serves for t_0 -validation purposes. The MWPCs used as input to the trigger have an intrinsic time resolution of less than 50 ns. Such a weak trigger condition is close to 100% efficient over a wide range of event classes, but has a rate which is about one order of magnitude higher than if one requires a significant histogram peak.

4 Conclusion

This trigger demonstrates, that complex electronics, which is dominated by a high wiring density, can be built without sacrificing flexibility. We examine as many as 34'400 rays simultaneously and still maintain many programmable options. Testability and performance monitoring becomes a major design concern.

References

- [1] K. Müller et al., Nucl. Instr. and Meth. A 312(1992)457
- [2] S. Eichenberger et al., to be published in Nucl. Instr. and Meth., as part of the Proceedings of the 6th Int. Wirechamber Conference, Vienna 1992.
- [3] S. Eichenberger, Diploma theses, University of Zürich (1988), H1 collaboration internal report H1-11/88-96, unpublished.
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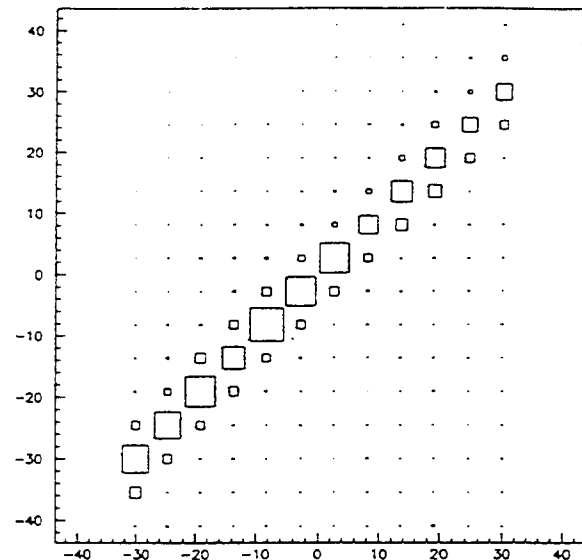


Figure 3 Reconstructed vertex position versus peak location in the histogram.