MICRON SEMICONDUCTOR SILICON DETECTORS OF THE 1990's

MICRON - C.D. Wilburn

SILICON DETECTORS FOR 1990's

with 'TECHNOLOGY DEMANDS'

MICRON SEMICONDUCTOR 1983 INCORPORATED

HEP DOMINATES MICRON BUSINESS

CURRENTLY 9 CONTRACTS CERN 8 CONTRACTS FERMI LAB

PRIVATE COMPANY U.K. BASED

PLUS U.S.A. MARKETING COMPANY

NO GOVERNMENT SUPPORT

TECHNOLOGY:

ION IMPLANTATION STRUCTURE

3" TECHNOLOGY (SILICON)

4" TECHNOLOGY (SILICON)

OTHER BUSINESS

HEAVY ION PHYSICS

SPACE PHYSICS

#### MICRON SEMICONDUCTOR ,

LATEST DEVELOPMENTS IN SILICON DETECTORS

U.K. BASED COMPANY / OPERATES FULLY TRACEABLE MOVITORED QUALITY CONTROL

SUPPLIED APPROXIMATELY 50 DESIGNS TO PHYSICS MARKET

TECHNOLOGY 3" AND 4"

CAPABILITY: DETECTORS Several 100/Month. PHOTODIODES Several 1000/Month

Single Area: 0.1mm<sup>2</sup> - 25cm<sup>2</sup> (3") 0.1mm<sup>2</sup> - 50cm<sup>2</sup> (4")

Ring Counters with central hole to 9.6cm 0

Gamma Transient Detectors Microstrip Detectors

> Pitch 10µ to 1cm Channels 5 to 2000

Thickness 150μ, 300μ\*, 500μ Response Time < 10nS

\* Leakage Current 6nA/cm² Capacitance 40pF/cm²

Single Sided and Double Sided

Integration with VLSI Electronics

Paralleled and Daisy Chained

FAN-OUT ON-CHIP / PCB / CER; MIC

Acceptance Levels: 99% - 100%

PIXEL Detectors Ring Counter Format 384 Pads Ceramic Overlay / Particles through back Charge Injection Devices (Indium Bump) 256 x 256 (30μ PIXELS) and 12 x 66 (75μ PIXELS) Designed to Interface Hughes RAM MICROCHIP with same pixel format

O.lem<sup>2</sup> - SILICON PHOTODIODES 0.lem<sup>2</sup> - 2.5cm<sup>2</sup> Id lnA/cm<sup>2</sup> tc 2nS High Speed | Large Area / Low Series Resistance / Low Cost

#### PACKAGING / ASSEMBLY MATERIALS

FOR

#### SILICON DETECTORS

PCB	MATERIAL	G 10	or	G	30

Minimum Track Width  $40\mu m$  Minimum Pitch  $100\mu m$  Maximum Size  $40\nu m \times 40\nu m$ 

KAPTON

Minimum Track Width  $70\mu m$ Minimum Pitch  $150\mu m$ Maximum Size  $40cm \times 40cm$ 

CERAMIC

KEVLAR

Minimum Track Width 70µm Minimum Pitch 150µm Maximum Size 40cm x 40cm MICRON SEMICONDUCTOR

DETECTORS FOR 1990's

MICROSTRIP DETECTORS

SINGLE SIDED

2048 Ch 25μ PITCH 300μ

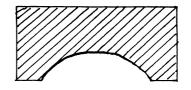
\* 520 Ch 10µ PITCH 150µ

Both Active and Inactive FAN-OUT

PROFILED DETECTORS (ZEUS)

Instead Straight Edge

SINGLE SIDED (HIGH RATE) CLOSE CUT



800Ch 45°

300µ

Edge < 500μ

ELECTRONICS - SANTA CRUZ
(Dielectric Isolated VLSI)

#### DOUBLE SIDED MICROSTRIP DETECTORS

#### for 1990's

#### 5 DESIGNS TO DATE

1988 1. RING COUNTER DESIGN S Heidelberg / CERN

1988 2. MICROSTRIP 40 x 40 x 1mm LEAR / CERN

1988 3. MICROSTRIP 50 x 50 x 3mm Edinburgh / SERC Daresbury

1989 4. MICROSTRIP 50 x 50 x (25μ & 50μ) BCD / FERMI LAB

1989 5. MICROSTRIP 16 x 32 x 2mm (A/c) UA2 / CERN

#### Problems

Yield

Uniformity of Characteristics

Manufacturing Control

Silicon Handling

Interstrip Impedance on Ohmic Side

AC or DC Coupling

Radiation Effects

Testing

#### MICRON SEMICONDUCTOR

#### DOUBLE SIDED DETECTORS

Necessary to bias all strips during testing.

Assembling devices prior to Test too costly.

Micron have developed 'Double Sided' computerised probe station for coarse detectors and will enlarge this for fine strip devices.

Probe station gives rapid control and feedback of processing for these difficult devices.

Double Sided Microstrip Detectors are a Triple Implant Device

- (1) Junction Strips
- (2) Ohmic Strip Isolation
- (3) Ohmic Strips

#### SILICON PIXEL DETECTORS

### During 1988 MICRON built 2 DESIGNS for SLAC for SSC DEVELOPMENT

(1) 10 x 64

120µ PIXELS

(2) 256 X 256

30μ PIXELS

Designed to Interface with HUGHES PIXEL ELECTRONICS built for INFRA-RED SYSTEMS and operate on U.C. Berkeley Test Facility.

#### STATUS

Both devices assembled via INDIUM BUMPING Detectors at Berkeley, Space Science Lab.

 $10 \times 64$  resolving Minimum Ionising Betas (2MeV) with Oscilloscope  $S/N \,>\, 10:1$ 

256 x 256 ready for first Beta Test.

#### Radiation Hardness

10 x 64 Claimed to be RAD HARD (1 M.RAD Co60?)

256 x 256 not RAD HARD, but RAD HARD version is now funded by SLAC to HUGHES (August 1989)

#### MICRON SEMICONDUCTOR

#### PIXEL DETECTORS

Pixel Electronics Studies

EUROPE

CERN

Heinje/ Jarron

200µm

RUTHERFORD Sharp / Seller

200µm

Pixel Collaboration U.S.A.

#### SSC Proposals

D. Nygren / N. Lockyer / G. Trilling / Hughes

Santa Cruz / Berkeley / Cornell

'Architecture for High Speed, High Rate Systems'

#### Limitations

Small Size | lcm² Indium Bump / Pressure Limits

Larger 'In'Solder Pads

#### Advantages

High Radiation Damaging Environments
Individual Pixels Damaged / Knocked out but sufficient
numbers remain to collect and analyse data usefully. If damage
rate high pixel should be small. S/N Min. Ionising needs to be high.

#### Future Physics

If successful EXPERIMENTS will most likely use some PIXELS along with MICROSTRIPS which will still carrry most of the AREA coverage.

#### RADIATION DAMAGE EXPERIENCE

EXPERIMENT CERN UA2
PHYSICIST: CLAUS GOSSLING
HADRONS: PROTONS with 15% NEUTRONS

OUTER DETECTOR

7 PAD ARRAY 6cm x 4cm

300µm

DESIGN I

LEAKAGE CURRENT (FD) 100nA typ.

1 METRE<sup>2</sup>

FULL DEPLETION (FD) 30 VOLTS

INNER DETECTOR

16 Ch. ARRAY 16.4mm x 32mm 300μm

DESIGN DD

OPERATIONAL

l Year with Off-Periods

Damage

lnA/cm<sup>2</sup> / 100 Rads

Total Dose

100K Rads

Some Design I received 30K RAD during beam

alignment

Electronics Inner AMPLEX 16Ch CMOS VLSI IMEC (P. Jarron Design)

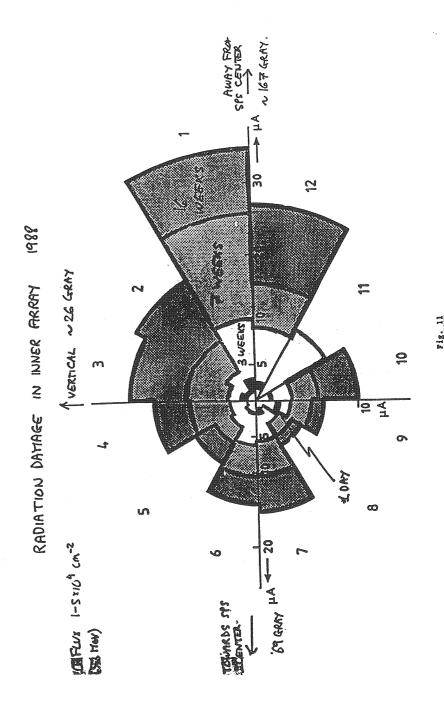
Outer

8 Ch. Hybrid. 0.8 μsec Shaping

EXPERIMENT E653

PHYSICIST BYRON LUNDBERG (Radiation mask

Reported Similar Damage results UA2



#### CURRENT RADIATIION EXPERIENCE

NEUTRONS 10<sup>12</sup>/CM<sup>2</sup>

REACTOR (14 MeV)

3 Test Detectors FD - 50V OP.V. 80V

Exposure  $\simeq 10^{12}$  neutrons/cm<sup>2</sup> ( = 1 Year SSC)

I LEAKAGE (BEFORE)	I (AFTER)	I(AFTER 3 MONTHS)
1.7nA 2.0nA 2.5nA	680nA 690nA 700nA	125nA 120nA 118nA
RISE TIME (B) 2.2nS 2.6 2.5	FALL TIME(B) 3.0nS 4.6 4.0	RISE TIME(A) FALL TIME (A)  2.2nS

RESPONSIVITY (0.85μm) (B)

RESPONSIVITY (0.85μm) (A)

1

0.89

Capacitance and Breakdown Voltage

NO CHANGE

ANNEALING 85°C 80V

I LEAKAGE 🗻 50nA

#### MICRON SEMICONDUCTOR

#### RADIATION DAMAGE EXPERIENCE

EXPERIMENT: FERMI LAB E789

PHYSICIST: JOHN KAPUSTINSKY 'LANL'

#### LANL TEST AUGUST 1989

SILICON MICROSTRIP DESIGN B 5cm x 5cm 1000 Channels 50 Micron Pitch Thickness 300µm Full Depletion 40 Volts Total Current 2µA

#### RADIATION

High Rate bursts of 300nS 800MeV PROTONS Run Times 2 Hours and 12 Hours Total Dose 1 x  $10^{14}$  PROTONS Event Rate: 5 x  $10^{7}$  PROTONS/cm²/sec and  $10^{8}$  PROTONS/Cm²/sec Ambient AIR

#### DETECTOR (20°C)

Leakage Current / Strip increased 8nA - 200nA Optimum Operating Voltage increased 60V to 150V Additional Current only present when Beam on Higher on Outer Strip and level proportion to Beam intensity

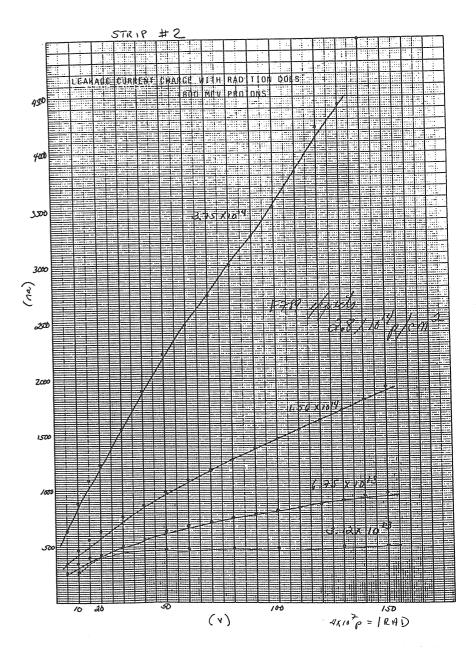
## SILICON STRIP BEAM TESTS AT LOS ALAMOS

(8/1 - 8/13/89)

# MICRON TYPE B W / and Plane 10 HIGH INTENSITY EXPOSURES OF 800 Me V/C PROTONS

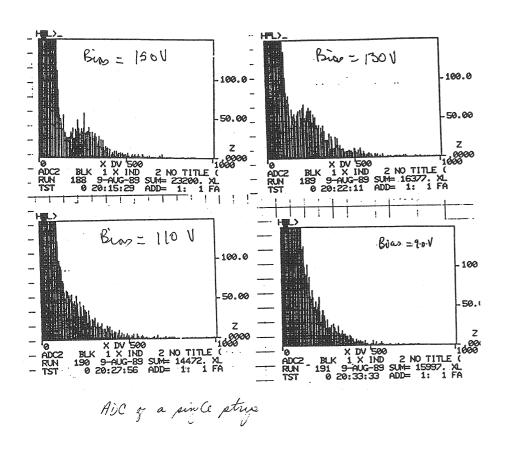
1.	$1.82 \times 10^{12}$	2 Hrs	$2.5 \times 10^{8} \text{ Ptm}^{2}$ .5	ON
	1.86 x 10 <sup>12</sup>	2 Hrs	#	ON
	1.86 x 10 12	2 Hrs	11	OFF
	$8.77 \times 10^{12}$	14 Hrs	$1.7 \times 10^{8}$	ON
	$9.29 \times 10^{12}$	14 Hrs	$1.8 \times 10^{8}$	OFF
	9.29 x 10 <sup>11</sup>	5 Hrs	5.2 x 10 <sup>8</sup>	ON
	9.29 x 10 <sup>11</sup>	5 Hrs	11	OFF
	$2.81 \times 10^{13}$	10 Hrs	$8.0 \times 10^{8}$	OFF
	7.62 x 10 <sup>13</sup>	19 Hrs	$1.0 \times 10^9$	OFF
10	$1.75 \times 10^{14}$	9 Hrs	5.4 x 10 <sup>9</sup>	OFF
	$4 \times 10^{14} \text{ P/cm}^2$			

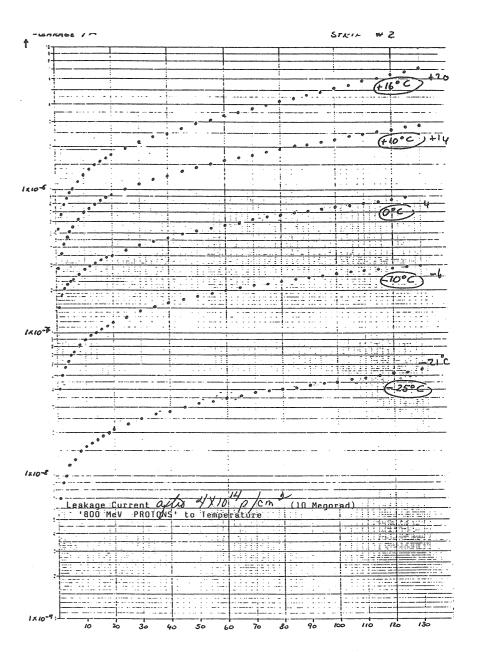
10 Megarad Total Exposure



cytic creation 2 10 13/5/cm2

Minimum Ionising Pulse to Applied Bias Voltage





#### SILICON PHOTODIIODES

Micron Semiconductor is manufacturing a wide range of 'LOW COST' SILICON PHOTODIODES.

Standard and Thin Window Implants are shown.

The Standard Window is - 2 0.5μm

The Thin Window is 🛫 Ο.1μm

Detector / Photodiode all depleted structure also available.

Typical Q.E. characteristic is shown next.

I dark Current - lnA / cm<sup>2</sup>

Capacitance (150μm) -- 70pF

Capacitance (300μm) -240pF

Suitable for (Scintillation Interfacing'.

