The Role of Analogue Circuitry in LHC/SSC Triggering

G. H. Grayer (RAL)

Introduction

For the first generation of collider experiments, the advantages and disadvantages of digital and analogue trigger circuitry were strongly debated. This was epitomized in the differing approaches to triggering of the UA1 and UA2 experiments. I think it is fair to claim that the balance of opinion came out on the side of digital processors, and this has been obvious from the second and third generation of collider experiments (CDF and D0 at the Tevatron collider, and the LEP experiments). However, the next generation of machines (SSC and LHC) will have to operate under very much more arduous conditions in speed and complexity, and this re-opens the question whether analogue circuitry has a major role to play. I will first review the conventional wisdom, and then look how this might differ in the new regime.

Analogue vs. Digital

Here is a brief summary of the general arguments put forward in favour of one technique or the other, though their validity depends greatly on the application:

- **Speed.** Analogue used to be used where speed was a priority. Now however this arguement can hardly be sustained. Digital circuits have become faster and faster, and at the same time power consumption reduced. Although there is always the overhead of digitization, this can be reduced to nanoseconds where necessary by the use of flash ADCs. This of course takes power, but analogue circuitry is also power-hungry when high speeds are required.

- **Power.** The simplest analogue circuitry is passive, but as soon as active circuits are included, analogue circuitry can consume very large amounts of power. This is because most devices have to support a standing current even in the presence of no signal, in order to retain linearity. Large dynamic ranges require high currents to represent them with fixed precision, as do high speed (fast slew rate) amplifier/buffers. Digital circuits, on the other hand, by using their devices as switches which are either off (no current) or turned fully on (low resistance) limit their I^2R dissipation. The final comparison of power budgets for doing the same task with the two kinds of circuitry finally depends largely on the complexity, precision, and speed required, and must be evaluated in individual cases.
- **Accuracy; precision; stability.** For limited precision (as is often sufficient for trigger systems) analogue circuitry can sometimes offer a much simpler solution. As soon as high precision and accuracy is required, circuitry becomes much more complex and power consumption increases. Cost also increases as components must satisfy closer tolerances. Long term stability, due to the hostile environment found in particle physics experiments, is likely to make performance deteriorate. Digital circuitry, on the other hand, has a precision and accuracy which is exactly determinable, and can be expanded to any desired level. Also correctly designed digital circuitry has immunity to quite large changes in environment (temperature and supply voltage) and ageing. In addition, they posses considerable noise immunity, which is also important in the environment of a particle physics experiment.
- **Design; programming.** Digital circuitry is simple to design compared with analogue. Its results are completely predictable and manipulable, using Boolean algebra, as long as the individual elements operate within their performance specification. Control and programming is more natural, since these will involve digital techniques. Digital storage is easy and accurate; indeed, the usual technique for programming analogue circuitry is by a digital register followed by a DAC.

After these very general remarks, I will now go on to consider in detail the possibilities of analogue circuitry in two of the three main divisions of detectors: calorimeters, tracking devices, and particle identification devices (see Fig. 1). I do not know of any suggested applications to particle

identification devices at the LHC or SSC. Furthermore, I consider only its use at the first or quasi-first level, since this is the critical regime where analogue trigger circuitry could play a part.

Calorimeter Triggers

Although later stages of calorimeter trigger processors tend to be digital, many of the schemes for SSC and LHC experiments plan to retain the raw data in analogue form while a first level trigger is being performed, this being more economical in terms of circuitry, an important factor in view of the large number of channels involved. This does not necessarily imply that the trigger itself is using analogue circuitry, however.

Most trigger systems use a reduced number of channels for the first level calorimeter trigger. The simplest way to achieve this would seem to be a simple passive analogue addition of signals, such as has been done in almost all large collider experiments, from UA1 to the ZEUS liquid argon calorimeter. However Goggi and Löfstedt [1] have pointed out that this can conflict with the optimisation of a system. Briefly, the reasoning is that with the high energies involved, a very large dynamic range (typically 15 bits, or 90 dB!) is required for the calorimetry, but the precision can be significantly less (9 to 10 bits, for the trigger even less), because of the intrinsic resolution of the calorimeter. In view of the large number of channels involved, and the need to reduce the electronics to a minimum, it makes sense to compress the dynamic range in some way. They considered the optimum transfer function, which is here irrelevant; what is not, however, is where this compression is applied to the data. There are three ways to apply this:

1) Linear pre-amp and non-linear ADC; this has two difficulties. A non-linear pre-amp with 90 dB dynamic range is extremely difficult to construct, and implies high current consumption. In addition, a non-linear ADC not an obvious device.

2) A non-linear pre-amplifier and a linear ADC; this seems much easier, and accurate logarithmic amplifiers can be constructed which are a good approximation to the optimum.

3) A non-linear pre-amp and non-linear ADC; this approach has some advantages and is favoured by the authors.

Only the first approach results in linear signals at a level suitable for addition, and as pointed out this is a very unattractive solution.

Another problem of an analogue addition of channels for trigger purposes is that of noise. For example, the transverse energy trigger adds calorimeter cells over a large part of the experiment. If these are a simple addition, the

resulting noise is obtained by the usual sum of squares over all these channels. A better solution would be to put a threshold on each channel before they entered the sum. An output gated by a discriminator operating on the signal present would be necessary.

Tracking Triggers

The principle difficulty with first level tracking triggers is the number of interconnections which must be made in all three dimensions in order to reconstruct tracks. Even if this is done with local logic, this can be mechanically very difficult. Therefore some coding of position using analogue signals with a single wire have been proposed. However, the problem is one of occupancy; multiple hits could be difficult to handle.

An example is the trigger proposed by R. Nickerson [2] for the silicon tracker on the SSC experiment on the SSC. each output is weighted by a different value resistor, and the result summed. A linear addition of the outputs is also made, and divided into the other sum. This normalises the result, which is proportional to the centroid of the track in the case of several adjacent hits (see Figs. 2,3,4,5).

Neural Networks etc.

An introduction was given at CERN to the LHC Trigger Group by C. Peterson of Lund University [3]. As background, I refer you to [4]. Since the classic neural network involves feedback or feedforward proportional to some resistance determined by the data, they must be classified as analogue circuits.

Neural networks have the advantage that they are highly parallel analogue computers, and hence fast. They are especially suited to pattern recognition problems, such as track recognition and cluster finding. Their performance in a particular case depends on the number of intermediate levels between input and output and the number of neurons in these levels, as well as the quantity of data used to train the network, and the number of passes made on this set of data. There is still a lot to be done to understand how to optimise these parameters.

Denby et al. at FNAL have made software simulations of track finding using neural network techniques [5]. They have examined the performance for different numbers of training events and different numbers of passes. Most tracks are found successfully, but there is always a residual of tracks not correctly reconstructed. However, this inefficiency may be acceptable for

trigger purposes. It is planned to test its performance under real conditions in a CERN test beam in tests for the SDC experiment (Belletini et al.) [6].

Fast track finding will require special LSICs to implement the neural network calculations. Neural network ASICs can already be purchased commercially, but they are much too slow for this application. However, the problem remains of the number of connections necessary, how these can be brought on-chip, and made in depth on the detector.

A related, but not classical neural network, has been developed by Bonino and Lautrop at CERN [7]. They have built a two-dimensional network which, applied to calorimeter data, finds clusters, gives their energy, and their area. The algorithm which achieves consists of a transfer of energy from cells to the neighbour with higher energy; this process is iterated until all energy is concentrated in isolated cells. Simulation shows that other (software) methods show that resolution of overlapping clusters is not as good as can be obtained by the best methods, but it is sufficient for triggering. The settling time is a few hundred nanoseconds.

Contiguity processors are the extreme case of a "dumb" network. These may be quite general track finders [8], or may have acceptable tracks pre-determined by the wiring [9]. One can argue that these are digital devices, for in their simplest form they just consist of a series of switches. However, one way of dealing with inefficiencies is to have a finite resistance with the switches open, then the inefficiency along a track is proportional to the resistance remaining [10]. This is essentially an analogue summation. An application of this principle to muon chambers was described in this Workshop.

Conclusion

It will be seen from this survey that the days when analogue or digital circuitry was a burning question are long passed. The advantages of digital techniques for most on- and off-line computing are manifest, but specialised techniques, for the most part on a grey area between analogue and digital circuitry, are likely to play an important role. After all, that so-far unequalled computer, the human brain, is a mixture of digital and analogue operations, as the section on neural networks pointed out. As our problems get more complex, we will presumably move towards the way that was pioneered by Nature, which mostly shows us the best way of solving a problem.

References

[1] G. Goggi, B. Löfstedt, "Digital front end for a calorimeter at LHC", talk given in LHC Trigger /DAQ Working Group, CERN, 26 July 1990.

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[3] C. Peterson, talk given in LHC Trigger /DAQ Working Group, CERN.

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[10] G.H. Grayer, "Real Time Track Finding for Future Large Particle Physics Experiments using LSI"; RAL-89-041 (May 1989) available from the author.

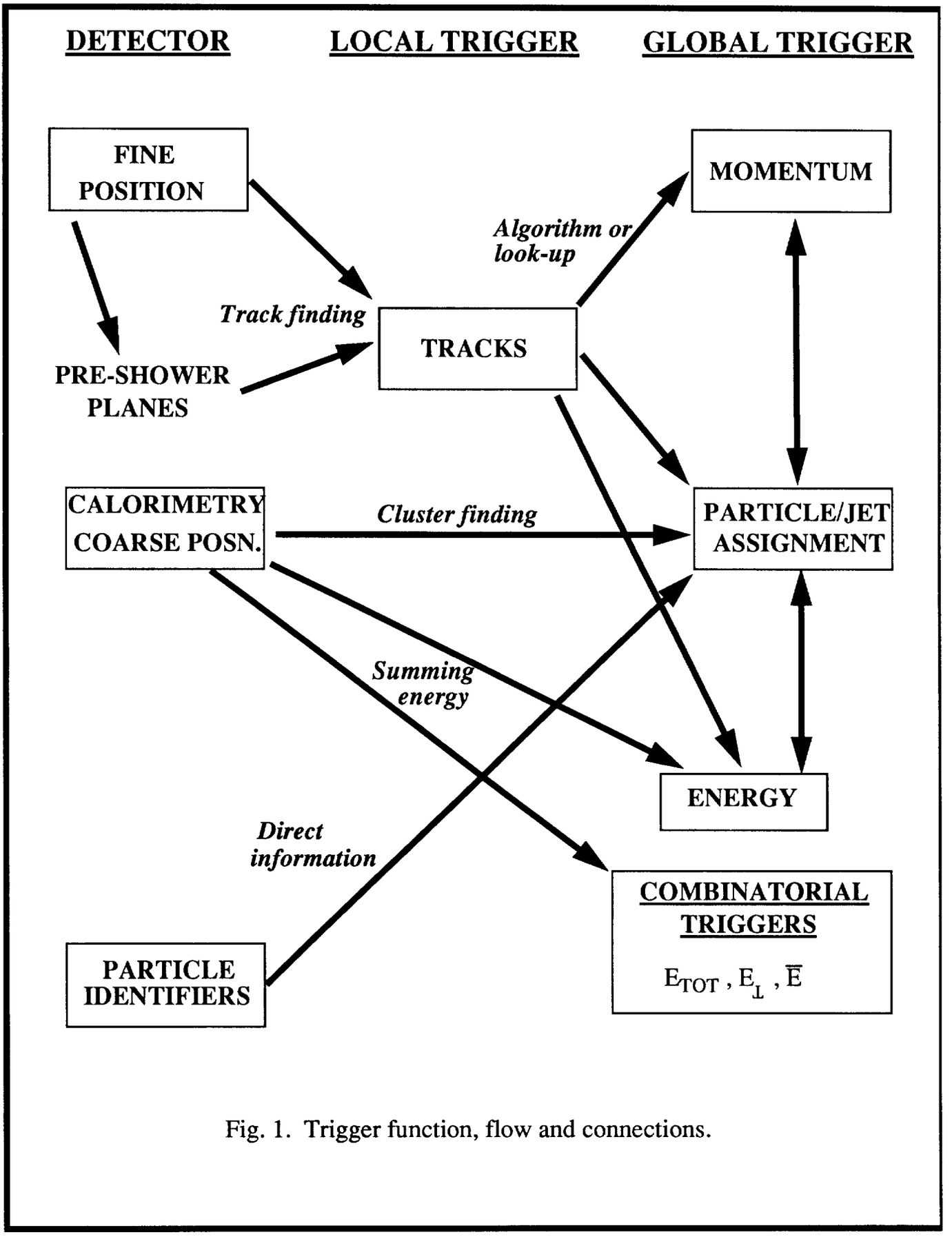


Fig. 1. Trigger function, flow and connections.

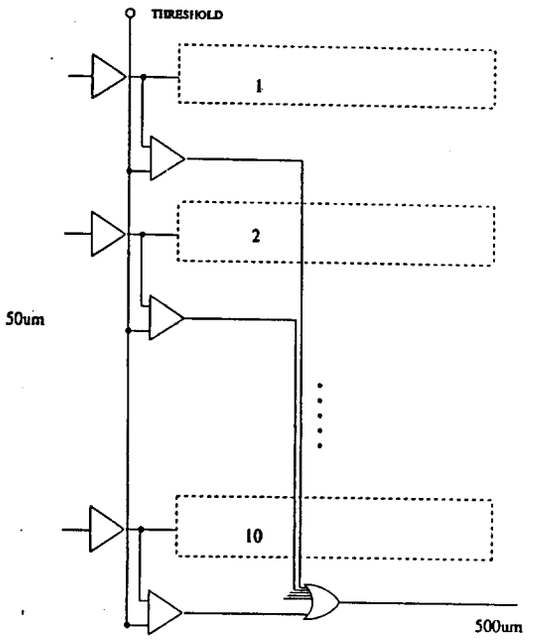
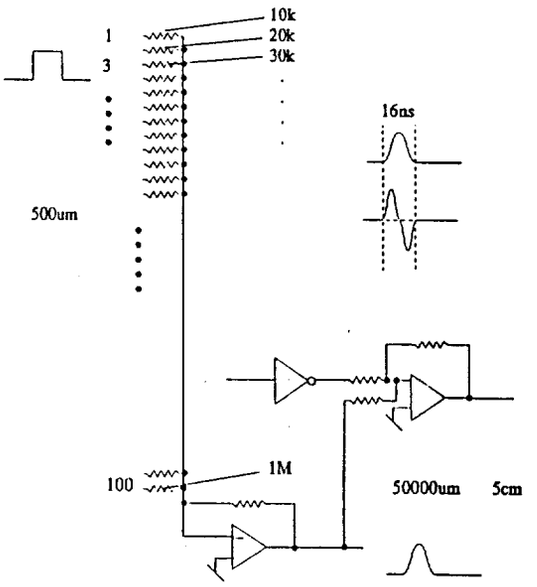


Fig. 2. Momentum trigger for SDC forward silicon strip detectors.
A logical sum is formed over 0.5mm [2].



Figs. 3. Momentum trigger for SDC forward silicon strip detectors.
Analgue signal is produced proportional to position.

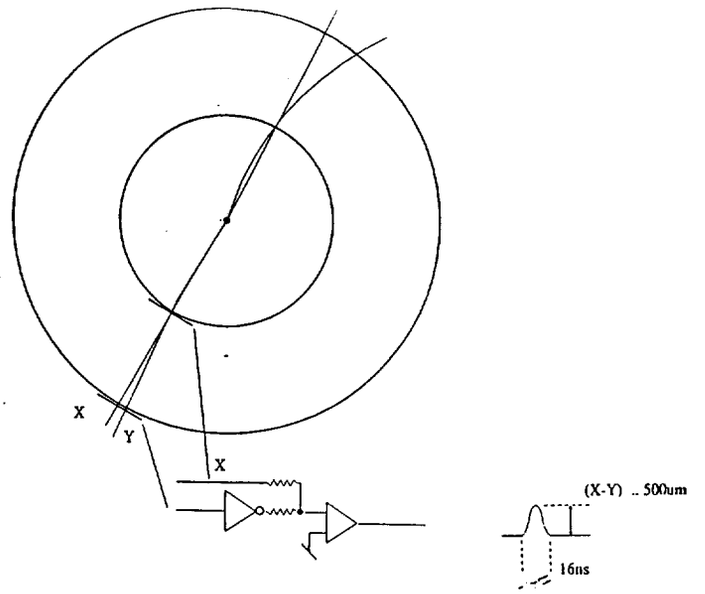
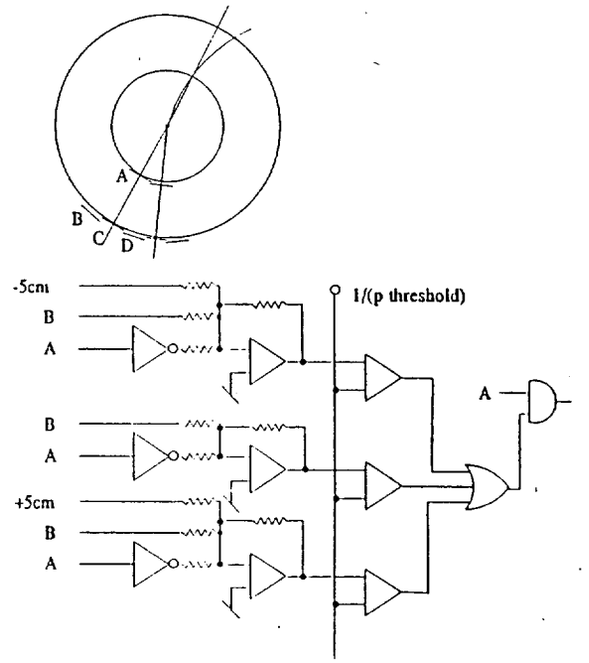


Fig. 4. Momentum trigger for SDC forward silicon strip detectors.A signal is produced proportional to the deviation from a stright line in projection [2].



Figs. 5. Momentum trigger for SDC forward silicon strip detectors. Each sector is tested separately for exceeding the momentum threshold [2]