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A TIMING SYSTEM FOR DIAMOND

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Abstract

This paper describes in some detail the organisation of the timing system for the proposed new electron storage ring DIAMOND and its injectors. In addition to the philosophy of the overall timing scheme details will be given of some of the electronic circuits used, which will realise enhanced stability and flexibility from the timing system. This will include a master oscillator driven by a Direct Digital Synthesizer (DDS). Combined ECL and analogue delay units for precision control of storage ring clocks, and a booster/storage ring coincidence unit for single bunch injection timing, will also be described.

1 INTRODUCTION

The proposed DIAMOND light source includes an electron gun using gated 500MHz pulses in a similar manner to that of the ALS [1]. It is hoped to produce sub-nanosecond electron bunches from the gun directly and so avoid the use of, or curtail the power needed in, a following buncher before entering a linac. In the case of a microtron a buncher will be required to get the electrons to relativistic velocities. The gun will inject into a 50 MeV commercially manufactured linac or microtron, which will provide enough acceleration to the injection energy of a 500MHz booster synchrotron. The booster will give full energy injection to a 3 GeV storage ring. The booster dipole magnet power supply will use resonant drive at 5 Hz or 10 Hz, with a peaking strip and gauss clock [2] tracking the field through the acceleration cycle. The gauss clock will also be used to control the current of quadrupole focusing and defocusing power supplies during acceleration of beam. In addition the extraction system will use programmable delay timers referenced to the gauss clock and interlocked with the booster orbit clock.

The timing system will need to be flexible in terms of storage ring fill patterns in a similar manner to that used on the ALS, with a spreadsheet determining storage ring fill patterns.

2 TIMING SCHEME

The design parameters for booster and storage ring are 211 and 564 buckets respectively at 499.6544 MHz. This gives a Booster Ring Orbit Clock (BROC) of 2.368 MHz and Storage Ring Orbit Clock (SROC) of 855.91 kHz. Coincidence (COIC) between booster and storage ring occurs at 4.198 kHz. Like the ALS an important feature of the timing scheme is the ability to load specific buckets in the storage ring. This can be done by delaying a specific number of BROC pulses {N} after the COIC pulse to target a specific bucket {T} in the storage ring. The number of BROC pulses to be counted is derived from the following expression

$$N = (139\,T) \text{ Modulus } 564$$

The booster extraction kickers are triggered from the N count output via precision delay units. To facilitate this bucket loading scheme the 500 MHz pulses to trigger the electron gun and extraction of beam are interlocked with BROC and COIC respectively. The time between the detection of a certain magnetic field and BROC or COIC will thus be variable meaning slight changes in energy before injection to the booster or extraction. If DC plus sinusoidal drive is to be used for driving the main booster dipole magnets (i.e. a biased excitation), the maximum resonant frequency of this magnet power supply system may be limited by the energy spread acceptable at injection or extraction.

The worst case at extraction for .01% change in energy/position corresponds to two COIC pulse intervals being needed after maximum field to synchronise and then target any storage ring bunch. This sets a maximum frequency of about 10 Hz assuming a trigger can be had .01% before peak field, or only 5 Hz if peak field is used to interlock with COIC.

In the case of injection more spread in energy is probably acceptable but it is only necessary to interlock with BROC. This takes less than 1μs although additional delays of a few BROC periods will be required, but even so the extraction time dominates the situation. This initial work suggests periods of up to 10 Hz are possible within these constraints.

3 THE ELECTRON GUN

A paper presented at this conference [3] describes the proposed DIAMOND low level RF and shows the arrangement of phase shifting between the different accelerating structures. In practice it is likely that the dividers for BROC, SROC and COIC will be located close to the gun and the 500 MHz for these counters will follow the final phase shifter. This enables 2ns logic pulses to be fully synchronously gated at high speed before fibre optic transmission [4] to the gun platform, and then amplified [5] to drive the gun cathode or grid.

The high speed 1062 MBit/s link in reference [4] is actually a transceiver and its input and output interface is differential PECL (positive ECL) although ECL can be

used with capacitive coupling. It is proposed to control and monitor equipment on the gun high voltage platform and drive the gun cathode directly from the same link. This can be achieved as shown in Figure 1, where control information is framed just before the time at which the link is required for direct gun modulation and a time window is then switched in to permit this.

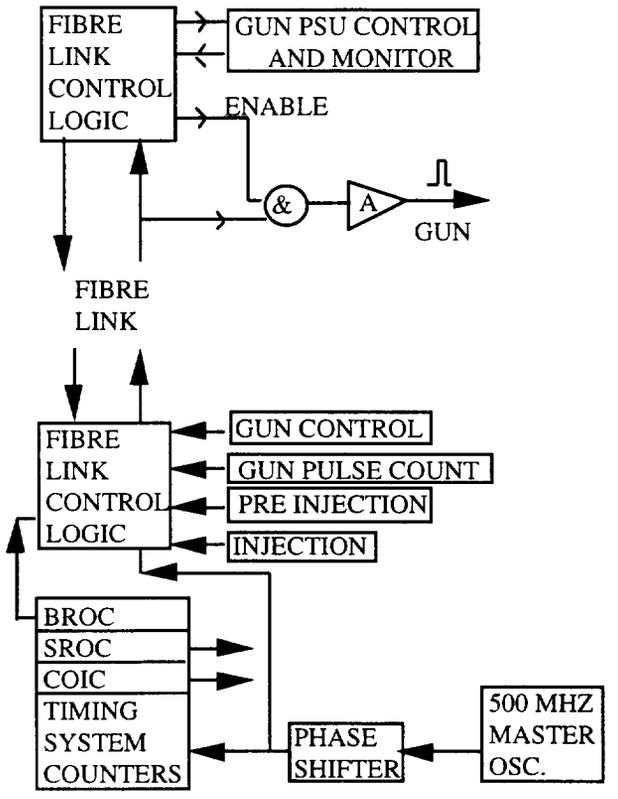

Figure 1. Gun Control and Pulse Drive

The control path on the link will either use double frequency encoding or most likely pulse position, where alternate clock pulses will be used to represent the bit clock. If a pulse occurs between these clock pulses a binary '1' is present, if not a binary '0' is transmitted. This simplifies the recovery of the data. Transmission of normal data will consist of two consecutive serial messages. The first contains the command and address, the second the written data or a frame in which read data must be inserted. Both messages will be error checked. If the gun is to be directly pulsed by the link the correct command is sent up so the link control logic switches the gun modulation gate on for a specific time and any pulses coming up the link in that time interval directly modulate the gun. The start of such a burst of pulses will be interlocked with BROC and injection field.

4 TIMING SYSTEM COUNTERS

It is intended to use Motorola ECLinPS logic to provide the main timing system pulses BROC, SROC and COIC. The ECLinPS 8 bit pre-settable counter (MC10EO16) has already been used in circuits to upgrade the SRS orbit clock counters where all three clocks are generated within one module. In that particular design, for historical reasons, the BROC and SROC pulses are increased in width before ECL to TTL conversion. The use of a clocked ECLinPS JK flip-flop accurately increases the width of the TERMINAL COUNT outputs from the pre-settable counters. The COIC pulse is produced by gating together the terminal count outputs of the BROC and SROC counters, with a JK again being used to accurately widen the pulse before TTL conversion. Although on DIAMOND the fact that the storage ring has more than 256 buckets complicates the detailed design the ECLinPS family of components is capable of doing the job.

There has been an increasing interest in having very accurate storage ring triggers (SROC-A) for both accelerator physics experiments and users. A combined fine analogue delay and counter will give a few picoseconds triggering accuracy on a storage ring bucket. The technique has already been used to produce a 500/16 MHz delay unit. However the design is simplified when going for larger division numbers as more time is available to make the value change to the pre-set count inputs.

The basic technique is to use a 500 MHz analogue phase shifter after the Master Oscillator output followed by a divide by 564. The output pulse from the divider can be moved later in time by causing it to count one extra clock pulse to move the trigger 2 ns later in time. In the opposite direction if the counter counts one less it moves the output pulse forward 2 ns.

The phase shifter is driven by digital to analogue converters and sine-cosine maps from an up-down counter (for manual adjustment) providing fine delay control. The two functions can be integrated by a carry or a borrow on the up down counter causing the 500 MHz counter to add one or subtract one respectively. Delays of a few picoseconds repeatability can be generated by this method.

5 INJECTION AND EXTRACTION

The intention is always to start injection so as to place the first gun electron pulse in booster bucket 1. The pre-injection pulse from the booster magnet timing will be interlocked with BROC and used to produce any delays necessary for injection RF power up and kicker pulse initiation.

As mentioned previously in section 2, extraction triggers will be coincident with the target bucket and precision multi-channel delay units within an EPLD will trigger booster extraction and storage ring injection devices.

6 HARDWARE

The intention is to use 3U x 220mm depth Eurocard modules for all the low level RF and timing system electronics. This is a low cost and flexible system and if necessary tightly screened boxes can be incorporated within these modules near to the front panel.

So far equipment designed as part of SRS upgrades to the timing system has used -5V supplies with single sided -5V and signal tracks against a ground plane. It is anticipated that at least a 4 layer board will be required for most DIAMOND designs. In addition the question of whether to use split supplies +2V and -3V to enable 50 ohm terminations at true DC ground level has still to be decided.

Ordinary quality glass epoxy base, double sided PCB has been used with no problems for the SRS upgrade designs and the same material will be used with multi-layer boards.

ACKNOWLEDGEMENTS

The authors would particularly like to thank C.C.Lo, M.Fahmie and B.Taylor for information on the RF and Timing System used on the ALS. Their elegant design approach to provide the flexibility required in the timing system of a modern storage ring , seems to be one that all should follow.

We would also like to thank our colleagues Peter McIntosh and Andrew Moss for their help in preparing this paper.

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