THE DESIGN, CONSTRUCTION AND PERFORMANCE OF THE ALEPH SILICON VERTEX DETECTOR

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Abstract

The ALEPH Silicon Vertex Detector is the first detector operating in a colliding beam environment that uses silicon strip detectors which provide readout on both sides and hence a three– dimensional point measurement for the trajectory of charged particles.

The detector system was commissioned successfully at the e^+e^- collider LEP at the research centre CERN, Switzerland, during the year 1991 while taking data at the Z^0 resonance. The achieved spatial resolution of the complete 73 728 channel device (intrinsic plus alignment) is 12 μm in the $r \cdot \phi$ view and 12 μm in the z view.

The design and construction of the entire detector system are discussed in detail and the experience gained in running the detector will be described with special emphasis on the uses of this novel tracking device for the physics of short-lived heavy particles produced in the decays of the Z^0 resonance.

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1 Introduction

The ALEPH Silicon Vertex Detector (VDET) was built to provide a high precision measurement of the trajectory of charged particles trajectories nearest to the interaction point, with the goal of reconstructing the decay topologies of short-lived particles. This enables the identification and lifetime measurement of short-lived particles with typical decay lengths down to a few tenths of a millimetre.

In order to achieve these goals, a three-dimensional vertex reconstruction capability was deemed essential, since a single projection of an event into e.g. the $r \cdot \phi$ plane leads to ambiguities in linking tracks to the rest of the spectrometer and occasional misassociation of tracks to wrong vertices.

In order to achieve a reconstruction of the track position in space the ALEPH VDET uses for the first time, double sided silicon strip detectors which give high spatial resolution in both projections, parallel and perpendicular to the beam direction.

This paper describes the design, construction, and running experience of this detector in the years 1991 to 1995. Section 2 describes the overall design of the detector. The basic components like silicon detectors and electronics and the assembly to the basic detector modules are described in section 3. Section 4 describes the mechanics used to hold the detectors in place. The peripheral electronics and the data acquisition system is explained in section 5. The experience during the operation of the detector is summarised in section 6. The reconstruction of the VDET data is described in section 7 and some data on the performance are given in 8.

2 Overall Design Considerations

The purpose of the ALEPH silicon strip vertex detector is the high precision measurement of particle tracks close to the interaction region without causing a deterioration in the performance of the outer tracking detectors.

Since multiple scattering of the charged particle tracks in the beam pipe and in the detector material reduces the accuracy of the track extrapolation to the primary event vertex especially for low momentum tracks, one is forced to make the first precise measurement as close as possible to the primary vertex and the radiation length traversed by the charged particles before the first measurement should be minimised.

The minimum radial position of the detectors is fixed by the size of the beampipe, and the outermost radius by the size of the Inner Tracking Chamber (ITC) support tube [1]. The inner radius of the ITC is 128mm and the outer radius of the beam pipe in the central region of the detector is 55mm. The design should also allow for remote installation and removal of the complete detector system.

Finally, the size of the silicon wafers available for the production of the silicon strip detectors (3" or 4" diameter) as well as the maximum input capacitance allowed for the amplifier to still achieve a reasonable signal to noise lead to a decision to use 50mm square wafers, which determines the overall solid angle coverage in the $r - z$ projection. Since the silicon detector area is larger than the active detector area, adjacent detectors in $r \cdot \phi$ overlap in order to achieve full solid angle coverage in this projection.

The above design criteria have led to the configuration shown in figure 1. Two layers of silicon strip detectors are arranged in two concentric barrels around the beam pipe with an average radius of $r_1 \approx 6.3\ cm$ for the inner layer and $r_2 \approx 10.8\ cm$ for the outer layer. The active detector areas of adjacent wafers are arranged such that they overlap by 2 mm in the $r \cdot \phi$ projection to cover the full solid angle with active detector area. This corresponds to a coverage of the $r \cdot \phi$ solid angle with overlapping wafers of ≈ 5
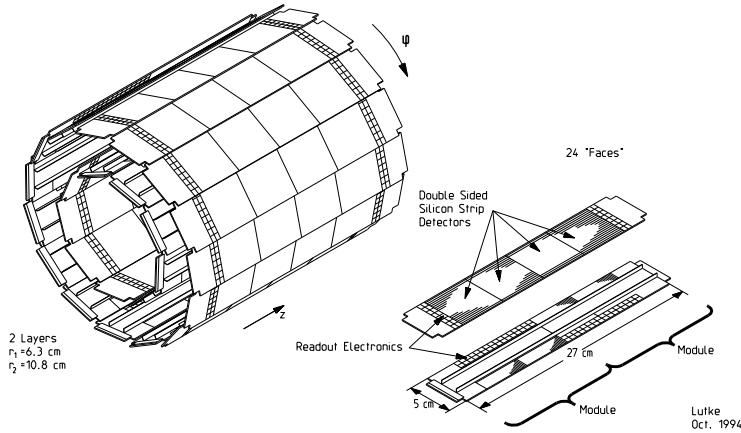
Figure 1: Configuration of the ALEPH silicon vertex detector.

%. Two detectors each are mounted onto one *electrical* building block, the *module* and two modules are again mounted together lengthwise to form the basic *mechanical* building block of the system, the *face*. The inner layer consists of nine mechanically independent faces and the outer layer has fifteen faces resulting in a total of 48 electrically identical and independent modules.

To minimise production effort we chose to employ only one type of wafer, one type of module, and one type of face. Choosing one type of face for both layers means that the fraction of solid angle covered by the active detector is 87% for the inner layer and 75% for the outer layer.

The silicon strip detectors have readout strips on both sides. The strips on one side are parallel to the beam direction and measure the azimuthal angle ϕ and the strips on the other side are perpendicular to the beam and measure the coordinate z. With the radius r of the individual wafers given by the mechanical holding frame, the position of a single particle hit is determined in cylindrical coordinates $r - \phi - z$.

The faces are mounted such that the ϕ sides are facing towards the beam pipe in the inner layer and towards the inner support wall of the ITC for the outer layer.

3   Modules and Faces

3.1   Overview

As mentioned before, the basic electrically independent unit of the VDET is the *module* (see figure 1).

Each module consists of two identical silicon wafers, the hybrids with the readout electronics and two short, flat kapton cables with a 35 pin connector. All components are custom made (except some surface mount resistors and capacitors). Each module is connected to the outside world via a 4 m long 3-4 mm thick multi twisted pair cable, a patch panel and a 32 m long TPC type cable. All modules are mechanically identical.

3.2 The Double-sided Silicon Strip Detectors

3.2.1 The Biasing Principle

The design of the detectors is the result of an intense R&D program that has been carried out over several years [2, 3, 4, 5]. It introduces a novel biasing scheme [3] which makes it possible to deplete the entire detector volume with the help of only two contacts, one for the p^+ side and one for the n^+ side.

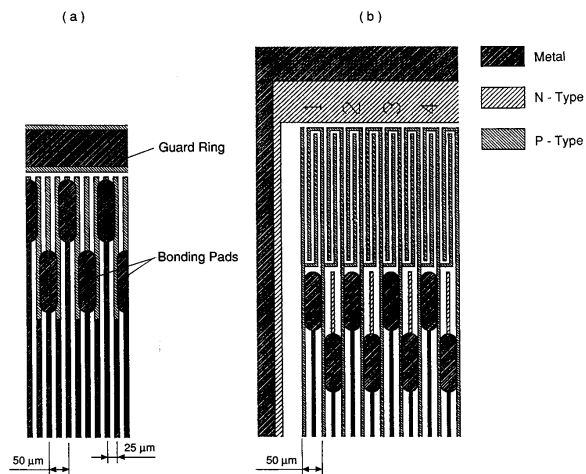Figure 2 shows the strip pattern on the p^+ junction side of the detector [5]. All

Figure 2: (a) The strip pattern of the p^+ junction side of the ALEPH double-sided silicon strip detectors.(b) Similarly for the n^- side.

p^+ implanted strips end a few μm from a p^+ guard-ring surrounding the active detector area. The p^+ strips are biased via the guard-ring structure using the punch through effect between two close p^+ implants. The principle is schematically shown in figure 3 [3] where a cross section of the junction side is shown for three different guard ring voltages.

When no voltage is applied (situation a) both p^+ structures are surrounded by a shallow depletion zone caused by the diffusion of charge carriers. With increasing voltage the depletion zone around the reverse biased contact (the guard-ring) grows. Situation b in figure 3 shows the configuration where the depletion zones touch each other. Further increase of the bias voltage will remove holes from the floating strip. This hole transport is a punch through current [6] which stops as soon as it has charged up the floating strip high enough to change the potential in the n bulk silicon in such a way that a barrier for the holes is created. The voltage difference between the two implants will remain almost constant, therefore allowing depletion around the floating strip (figure 3c). The value of the voltage difference is a function of the resistivity of the silicon and the distance of the p^+ strips to the p^+ guard-ring. The gap between the p-strips and the bias strip was chosen to be 4 μm, resulting in a voltage difference ΔU of about 3-4 V.

On the n^+ side the strips are biased by taking advantage of the electron accumulation layer present at the silicon-silicon oxide interface. Figure 2b) shows the strip pattern at the edge of the n^+ side. The p^+ blocking strip implants between the n^+ strips are formed to end in a channel [3, 5], thereby defining (at full depletion) an ohmic bias resistor, with a value determined by the sheet resistance of $\sim$ 30 $k\Omega$ per square and the length and the width of the channel. In the present design, the bias resistance of a n^+ strip to
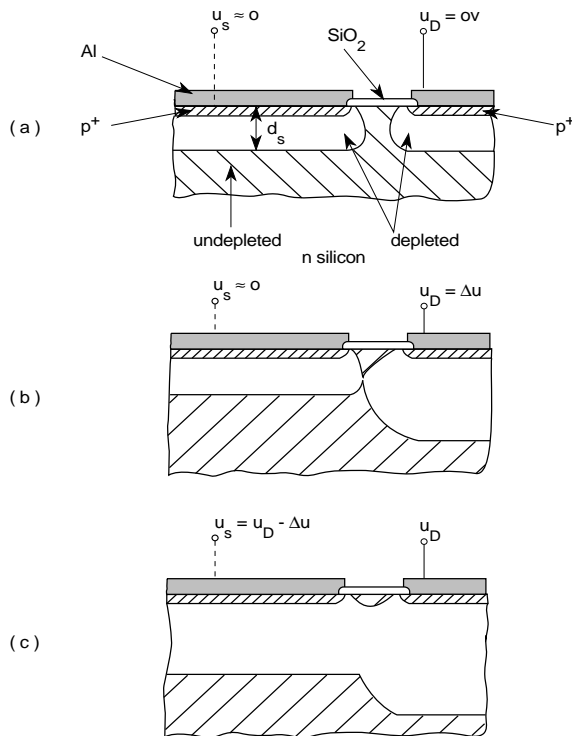
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Figure 3: Biasing principle of the detectors. a) Shows unbiased detector with intrinsic depletion zones around the p^+ strips. b) Shows detector partially biased from the guard ring with the depletion zone extending toward the p^+ strip. c) Shows a fully depleted detector with the depletion zone stretching all the way through.

the guard-ring is $R^{\Omega}_{s-gr} \approx 1 - 5 \ M\Omega$ for a fully depleted detector.

To summarise, even on the ohmic side, one contact to the guard-ring structure surrounding the active strip area is sufficient to bias all strips simultaneously.

3.2.2 Detector Properties

The detectors used in the present system have been designed at the INFN, Pisa and fabricated at CSEM, Neuchatel (Switzerland) [7] on 4 inch n type float zone wafers [8]. Details on the production process can be found elsewhere [5]. Table 1 summarises the basic properties of the detectors.

Applying capacitive charge division every fourth p^+ strip on the junction side and every second n^+ strip on the ohmic side are connected to the readout electronics.

3.2.3 Electrical Tests and Quality Control

The total leakage current for a detector is typically in the range of a few hundred nA. The currents are measured for an over-depleted detector with detector bias voltage $V_{Det} = 1.5 \ V_{Depl}$. Detectors are accepted if the total reverse bias current of the detector is less than 2 μA, no single strip exceeds a current of 500 nA and not more than two strips show a leakage current of more than 100 nA. In addition detectors were rejected with short circuits between strips that affect more than two readout electrodes.

Finally, the inter strip resistance is measured on the n^+ side to check for the proper separation of the n^+ readout strips through the p^+ blocking structures when fully depleted. Figure 4 shows a typical example of the resistance between strips and the resistance

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detector dimensions	51.2 mm × 51.2 mm	
wafer thickness	300 μm	
resistivity	6 - 30 $k\Omega cm$	
depletion voltage	8 - 60 V	
	p-side	n-side
active area	49.8 mm × 49.7 mm	49.7 mm × 49.0 mm
p-strips (diodes)	1994	-
p-blocking strips	-	995
n-strips	-	994
(p/n) pitch	25 μm	50 μm
strip length	49.7 mm	49.0 mm
strip width	12 μm	12 μm
inter strip capacitance	≈ 1 pF/cm	≈ 1 pF/cm
capacitance to backplane	1 pF	1 pF
minimal readout pitch	50 μm	50 μm
bond pad size	200 μm x 50 μm	200 μm x 50 μm

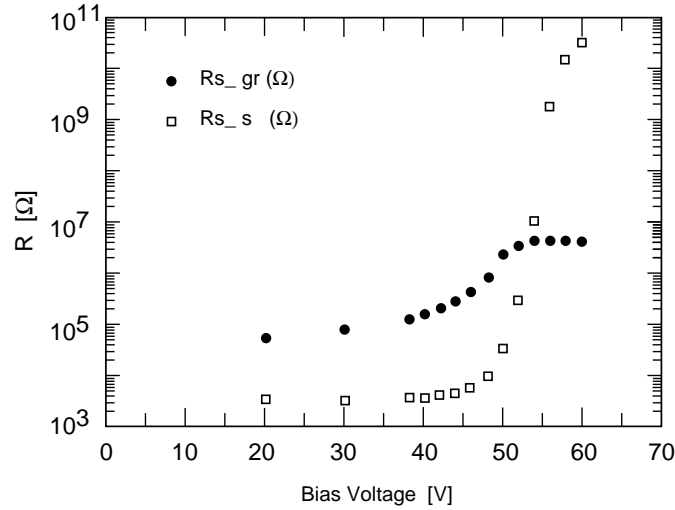Table 1: Properties of the ALEPH silicon detectors

Figure 4: An example of the functional behaviour of the resistance between the guard-ring and a n^+ strip (R_{s-gr}) and one n^+ strip to the next (R_{s-s}) as a function of the detector bias voltage. The voltage corresponding to full depletion of the detector is about 55 volts.
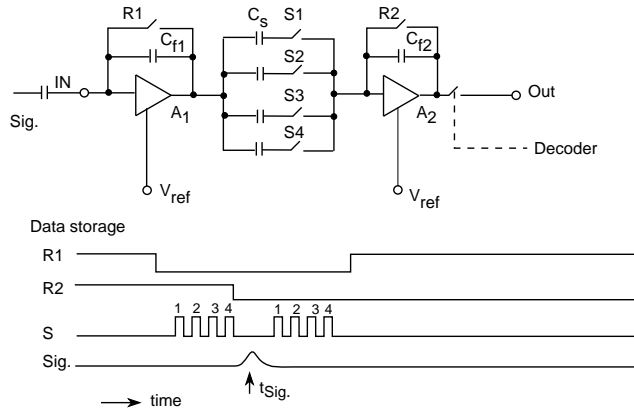
Figure 5: The structure of a single channel of the amplifier section of the CAMEX64 and the timing diagram.

between strip and guard-ring on the ohmic side as a function of the detector bias voltage. Detectors are accepted for $1\ M\Omega \leq R^{\Omega}_{s-g} \leq 10\ M\Omega$.

The fraction of accepted detectors was $\approx 70\ \%$.

3.3   The Readout Chip CAMEX64

The readout chip used for the present detector is the CAMEX64 (Cmos Amplifier with MultiplEXing 64 channels). The chip is a custom designed VLSI silicon chip with 64 parallel channels arranged in a readout pitch of 100 μm. It has been developed in CMOS technology in collaboration between the Max Planck Institut für Physik, München and the Fraunhofer Institut, Duisburg [9].

The chip provides signal amplification, noise filtering, parallel storage and serial readout of the analogue signals and contains digital control for power switching as well as a calibration network.

Figure 5 shows the layout of a single channel of the amplifier section of the CAMEX64 together with a timing diagram [9] of the switching sequence.

The chip is designed in such a way that the currents in all the branches of the circuit can be scaled through a voltage V_{Ref}.

When the switches are closed the inputs of both amplifiers are at virtual ground potential. In opening the switch R_1 charge is injected into the input of the first charge sensitive amplifier (A_1) and creates an offset of its output which charges the four storage capacitors C_{S_i} at the time the switches are closed. Now R_2 is opened. If there is a deposition of signal charge Q_{sig} at the input of the A_1 at the time t_{sig} then the output voltage of A_2 changes by $\Delta U_1 = Q_{sig}/C_{f_1}$ and injects charge $Q_2 = 4\Delta U_1 C_S$ into the amplifier A_1 once the switches S_i are closed again.

The amplifier A_2 in turn changes its output voltage by $\Delta U_{out} = Q_2/C_{f_2}$. Since only the difference between the samples taken before and after the arrival of the detector signal is integrated on the feedback capacitor of the amplifier A_2, the correlated unwanted signal components taken at these instances are removed and the uncorrelated signals are averaged. Hence one has measured four samples of the output of the amplifier A_1 before and four samples after the signal arrives with a corresponding reduction in noise [10] and
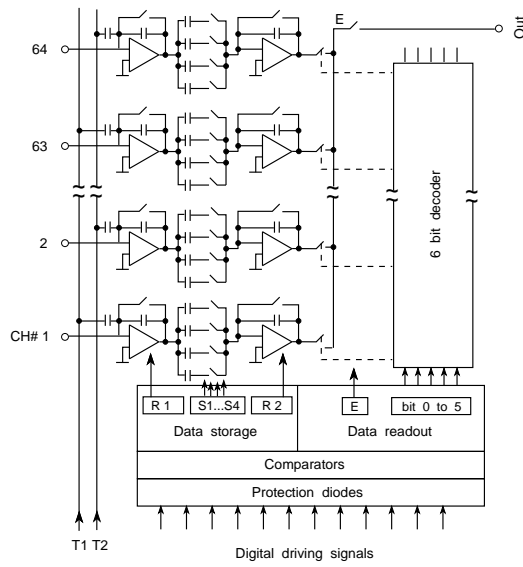
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Figure 6: Schematic block diagram of four CAMEX 64 channels.

an additional fourfold amplification. The output voltage is now

$$U_{out} = \frac{Q_{\text{sig}}}{C_{f_1}} 4 \frac{C_S}{C_{f_2}}$$

The schematics for four channels of the entire chip is shown in figure 6. The reset and sampling signals R_1, R_2, S_1 to S_4 are applied in parallel to all channels during the data storage cycle, while the readout is done serially from channel to channel with the help of a digital decoder which is also implemented on the chip. The output can be switched for the complete 64 channel chip (with the "Enable" signal E) to allow daisy chaining several chips together.

Each signal input is equipped with a test capacitor used for simultaneously testing all even or all odd numbered channels through two test inputs. These test inputs prove very useful also for adjusting the overall output offset level of a given chip.

The surface has been passivated with phosphorus glass.

Table 2 summarises the main characteristics of the CAMEX64 chip.

Type	$3.5\mu m$ CMOS
number of channels	64
Area	$6.35 \times 4.95\ mm^2$
Thickness	$0.5\ mm$
Bond pitch	$100\ \mu m$
Power/channel	$\approx 1\ mW$
Equivalent Noise Charge (ENC) $[e^-]$	$335 + 35 \times C_{in}[pF]$
Radiation hardness	$25 - 30\ krad$

Table 2: Properties of the CAMEX64 readout chip

3.4 The Hybrid Circuitry

The readout electronics for the ϕ and z strips of each module consists of two different ceramic printed circuits equipped with their ASICS (CAMEX64, AC-chips, steering chip,

line-driver) and SMD components. They are called ϕ and z hybrid and described in the following.
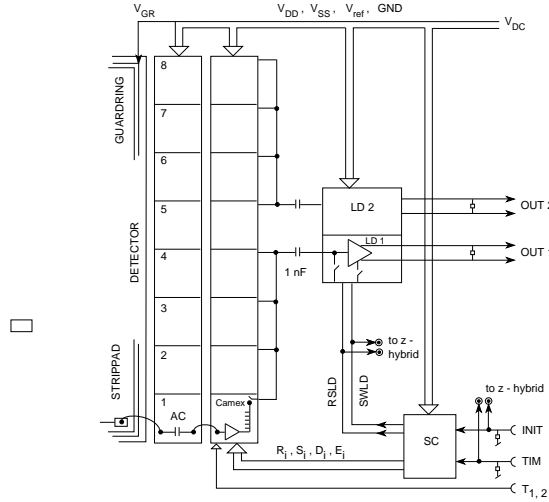

Figure 7: Electrical block-diagram for the ϕ side hybrid. The corresponding diagram for the z side looks very similar.For simplicity the signal path for only one strip is shown. SC is the steering chip, LD the line driver, and AC the AC capacitor chip.

An electrical block-diagram of the ϕ hybrid is shown in figure 7. As seen in figure 1, one module has two detectors. On the ϕ side the strips of the two detectors are daisy chained with wire-bonds. On the z side each strip of the detectors is bonded to an electronics channel. There are 497 readout strips (with pitch of 100 μm) per detector on each side which need 8 CAMEX64 chips on the ϕ side and 16 CAMEX64 chips on the z side.

3.4.1 The AC chip

Since the input voltages of the individual channels of the CAMEX readout chip may vary by as much as 100 mV from channel to channel, currents can flow through the detector network into the amplifiers and saturate them. Hence AC coupling of the strips to the electronics with coupling capacitors on the n^+ side is necessary.

Therefor a special AC chip is used to connect the detector strips to the inputs of the CAMEX amplifiers. Both chips match in width and pitch. Double polysilicon capacitors ($C \approx 210pF$) are produced with a $100\mu m$ pitch on a quartz substrate to minimise the stray capacitance ($\approx 0.3pF$).

The average breakdown voltage of the capacitor is above $24V$.

The chip has been designed at the INFN, Pisa [5] and produced by CSEM, Neuchatel, Switzerland [7].

3.4.2 The Steering Chip

The digital steering signals, the supply voltages and the test pulses are common to all 8 (16) chips on the ϕ (z) side hybrid. In order to minimise the number of input lines and hence cable space, all these signals are distributed on the hybrid to the individual CAMEX64 chips using a common fanout bus structure. For this purpose a special demultiplexing chip, the so-called "steering chip" has been developed in CMOS technology which uses an incoming pulse-train (TIM) and an initialise signal ($INIT$) to generate all

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the 15 digital control signals that are needed to operate the amplifier chip. CMOS TTL levels are used both for the input and the output of the steering chip. The chip has been custom designed at the Max Planck Institute für Physik, Munich and produced by ES2, Munich.

The "Enable" signals (E 7) switch all individual amplifier outputs of each of the four CAMEX chips sequentially to allow the serial readout of the 4×64 channels onto one output line.

3.4.3 The Line-driver Chip

The output line is routed to one common line-driver chip. Hence there are two output lines on the ϕ side hybrid (for 8 CAMEX64) and 4 output lines on the z side hybrid (for 16 CAMEX64) resulting in a total of $6 \times 256 = 1536$ analogue channels for one module.

The line-driver chip has been developed in collaboration between the Fraunhofer Institut in Duisburg and the Max Planck Institut für Physik in Munich and manufactured at the Fraunhofer Institut. It is a current source that is able to drive ± 1.2 V into a 100 Ω twisted pair cable that is terminated at both ends with 100 Ω. The gain of the circuit is adjustable with values between 1 and 4 with an external resistor. The line-driver is resetable (the reset signal is called $RSLD$) and the power consumption can be minimised with the help of an external bias voltage that controls the current consumption and/or by switching the chip on only when readout of the CAMEX64 is requested (with the signal $SWLD$). These two digital control signals are also provided by the steering chip described above.

The line-driver, like the CAMEX64, has been provided with externally adjustable comparators at the inputs.

3.4.4 The z Hybrid and the Detector Voltage

The electrical block-diagram of the ϕ hybrid in figure 7 applies in general also for the z side hybrid. However, there are some differences which will be described in the following.

The number of CAMEX64 chips on the z hybrid is 16 instead of 8 and the number of twisted pair output lines is 4 instead of 2 corresponding to 2 physical line-driver chips. These line-driver chips have to be able to drive negative signals (opposite to the situation on the ϕ side).

For voltages greater than ≈ 24, the AC coupling capacitors between the silicon strip and the CAMEX64 amplifier can break down. But the depletion voltages of most of the detectors can be up to 60 V (see Section 3.2); for this reason the supply voltages of the CAMEX64 electronics and the steering chip on the z side hybrid are referenced to "High Ground" which is essentially equal to the depletion voltage. Because all signals coming to and from the outside world are referenced to low ground, the input of the steering chip and the test input and output of the CAMEX are AC coupled (1 nF, 200V). In order not to duplicate input lines, the voltages and clocking signals needed to operate the line-driver chips on the z side are provided from the ϕ side via contact holes in the hybrid ceramics.

3.4.5 Production and testing of the hybrids

The ceramic printed circuits, produced using thick film technology, and developed and produced at CERN and at MPI Munich, are not standard technology with respect to

trace parameters and substrate. Very thin traces of 90 μm width with 100 μm separation had to be printed on rather long (14 cm) pieces of 250 μm thin ceramics.

By careful inspection of each printing step and correction of faults which arose, a high yield was finally achieved. This is especially important for the z-ceramics which serve also as support for the silicon detectors.

Once equipped with all their components, the hybrids were tested under conditions similar to those in the experiment. For each hybrid bad missing or noisy channels were marked. This information was used during the bonding of the detectors to the electronics.

3.4.6 Radiation tests

To study the radiation hardness of the CMOS electronics the components were irradiated using Gamma rays from a ^{60}Co source and X-ray machines (between 40 and 200 keV) [11].

The CAMEX64 has been irradiated both with power off and with power on and the clocking signals operating. The former condition corresponds to a situation where the radiation dose accumulates during periods when the LEP machine is being tuned and when the detector is turned off completely. The latter condition corresponds to the normal running in collider and data taking mode where the detector is turned on. With power off the chip continues to function, though with increased noise, up to about 440 $krad$, where it ceases to function. With the chip powered and running, the permissible dose is lower, and the chip will die when the dose reaches $25 - 30$ $krad$.

The steering chip has been irradiated with power on and clocking at the input. The chip remains fully operational up to an integrated dose of ≈ 650 $krad$ at which point some of the output lines do not function anymore.

The line-driver chips, both the version for the ϕ side (positive going signals) and the z side (negative going signals), have been irradiated with power on and clocking signals operating. The negative line-driver does not change until the integrated dose reaches $\approx 25 krad$ at which point the output voltage offset begins to increase until the chip becomes useless at $\approx 50 krad$. The positive line- driver shows no change up to a dose of 50 $krad$. After this dose the output offset voltage rises until it reaches an intolerable level at a radiation dose of 85 $krad$. Power consumption, rise-time and the closed loop amplification remain unchanged during the irradiation.

The results of the irradiation tests show that the CAMEX64 chip is the least resistant of the three CMOS chips that are used in the hybrid assembly. Since a reduction of the signal to noise ratio below 10:1 renders the CAMEX64 chips essentially useless, one can conclude that the hybrids are safe up to an integrated irradiation dose of at least 25 $krad$.

3.5 Module Assembly

Figure 8 gives a schematic overview of the basic components that are needed to produce a module: one ϕ and one z hybrid, two matching (with respect to the depletion voltage) detectors, two high precision brass inserts, and two 10 cm long Kapton cables with a 35 pin connector.

The assembly is done in the following steps:

– The ϕ and z hybrids are glued back to back and the through contacts are made with thin wire and conducting epoxy. Then the Kapton foils are glued to the hybrids and wire bonded.
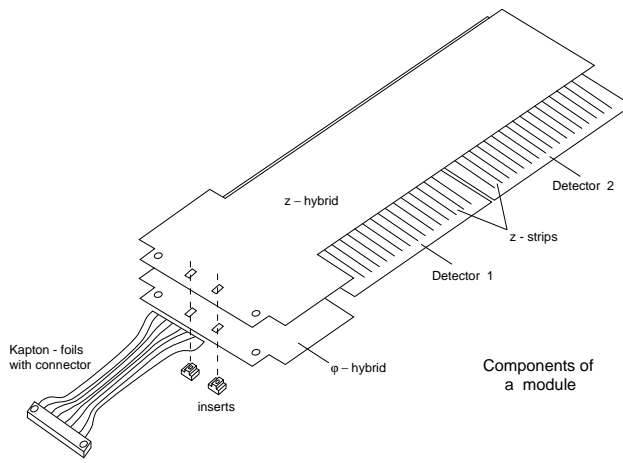
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Figure 8: A schematic overview of the components needed to assemble a complete silicon detector module

- The selected detectors are aligned on $x - z - \phi$ tables (held by vacuum) with respect to each other and to the reference pins for the brass inserts. These brass inserts are machined to very high precision and define the internal geometry of each module. Their installation is performed under a microscope with positioning accuracy of $\approx 5 \ \mu m$.
- The hybrids are placed onto the detectors and glued under slight pressure with three beads of glue along the z-hybrid. At the same time the two brass inserts are glued into oversized holes in the hybrids. One of the inserts has a round positioning hole, and the other an elongated one. To avoid thermal stress the gluing is done at constant temperature.
- The connection of the silicon strip detector with the AC chip is done via ultrasonic wedge wire bonding using 25 μm thick Aluminum-Silicon wire. Known noisy or saturated amplifier channels are skipped. The two detectors on the ϕ side are daisy-chained to each other and the guard-rings of the two detectors are connected on both sides to each other and to the supply lines on the hybrids. The resulting bonding pattern (the correspondence between readout channel and silicon strip) is recorded in a bond-map for later use in the analysis software.

3.6   The Assembly of the Faces

Two tested modules were positioned on a highly polished stainless steel vacuum chuck and aligned under a microscope using two precision pins which facilitate the alignment and guarantee identical length of all faces.

Two ceramic ribs of 5 $\times$ 0.62 mm^2 are glued along the whole length of the face. They join the two modules mechanically and are strong enough to reduce sagging to less than 5 μm. They can be broken, if necessary, for the replacement of a bad module. To achieve a precise radial position of the faces, ceramic spacers are glued at both ends of each face in such a way that the surface of the spacer has a well defined distance to the surface of the silicon wafers. All the gluing was done at constant room temperature to avoid any thermal stress.

After a face is glued, the overall precision of the final assembly is checked by measuring the distances between the precision brass inlets and the silicon strips with an optical measuring machine.

The planarity of a subsample of the detectors has been measured before the assembly with a high resolution microscope. The detectors are found to show a slight bowing with an average sagitta of $\leq 20 \mu m$ and thickness variations of up to 20 μm.

The orientation of the z–strips to the ϕ–strips is given by the accuracy of the mask alignment during the production of the detectors. The misalignment has been measured to be $\leq 0.06 \; mrad$.

4 The Mechanical Frame
4.1 The Overall Design

The mechanical frame is the device that defines the positions of the VDET faces at the centre of the ALEPH experiment. The radial size of the detector was determined by the available space, the thickness of the electrical and mechanical shielding, and a safety margin for installation of the detector. This together with the other constraints led to the placement of 9 faces at an average radial position of 6.3 cm in the inner layer and 15 faces at an average radial position of 10.8 cm in the outer layer.

Figure9 shows a three dimensional view of the mechanical frame consisting of two rings for mounting the faces (referred to hereafter as *face rings*), a cylindrical shell that holds these together and two rings for attaching the cables (referred to as *cable rings*). Since the detector had to be installed around the beam-pipe which was already in place, the whole structure consists of two half-sectors; one with 4 (7) faces in the inner (outer) layer and the other with 5 (8) faces in the inner (outer) layer.

The two face rings are attached to a cylindrical shell consisting of a hollow carbon fibre sandwich structure, which forms a rigid cylindrical frame around the beam pipe. The frame has a total thickness of about 0.1% of a radiation length for a particle traversing at $\theta = 90^0$; the total radiation length traversed is 4.2 % averaged over ϕ, mainly due to the readout electronics on the z- side.

4.2 Face Rings

The face rings are made of 4.5 mm-thick slabs of carbon fibre material. The position of a given face is determined by three brass studs that were glued in holes in the face rings and subsequently machined to a final accuracy of 15 μm. The radial position of the face is fixed by the surface of the two outer studs on each side and the ϕ position by precision steel pins in the centre stud on each side. The pins have spherical heads to facilitate the mounting of the faces and mate to precision holes in the brass inserts in the face (see section 3.5). To allow for thermal expansion of the face one of the positioning holes is elongated, and the faces are restrained by small springs. The face is mounted on these studs with the z side facing the carbon fibre inner shell.

After the face rings had been equipped with the aluminum studs and machined, the two halves of the cylindrical carbon fibre shell were glued to the rings with a precision jig that aligned the two rings relative to one another to about 10μm. Finally, the face rings were cut to make the two half cylinders.

4.3 Cable Rings

In order to decouple the face from the forces exerted by the cables and the shields, the connectors on the Kapton foils were mounted on the cable ring, which is mechanically detached from the rest of the mechanical structure. The cable rings are made of 3 mm thick carbon fibre plates and are attached to each other via carbon fibre tubes that pass through spaces in the sandwich-structure shell that connects the face rings. The electrical
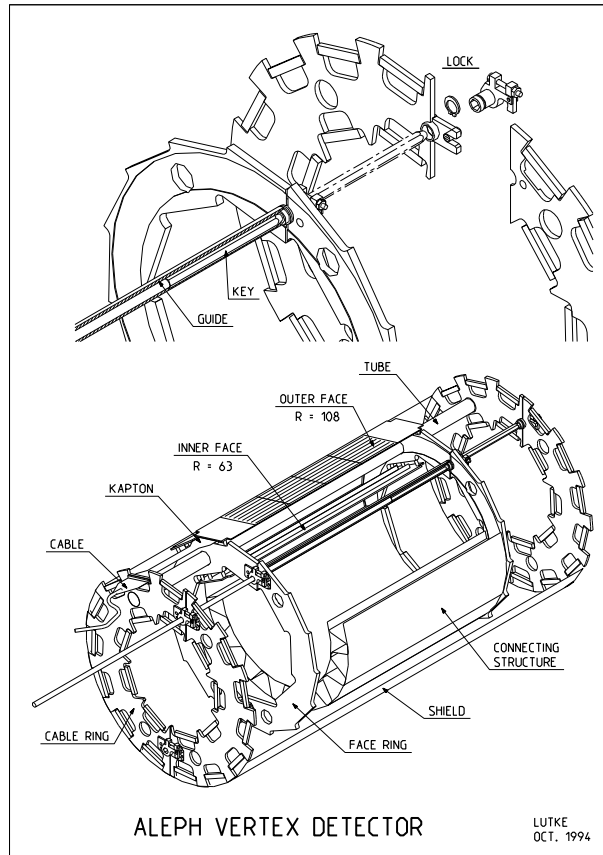
Figure 9: The mechanical holding frame for the vertex detector showing the face and cable rings, the shield and one face mounted. The upper picture shows the detail of the locking mechanism that holds both parts together after assembly.

connectors are fixed to the cable ring using small aluminum stud bolts that are glued in the carbon fibre material. The openings in the face and cable rings allow airflow to the two sides of the faces.

4.4   Shielding

The outer surfaces (in z) of the cable rings were covered with aluminum foil to provide electrical shielding. The mechanical frame is covered with a shielding that encloses the faces to the outside and inside (in $r \cdot \phi$). It consists of a 125 μm carbon fibre foil laminated to a 25 μm aluminum foil. The shielding is fixed with the help of metal brackets that are screwed to the cable rings. It is electrically connected to the common ground of the detectors.

4.5   Installation

In order to be able to mount the detector inside ALEPH, the cable rings and the face rings have skids made out of glass fibre on the top and the bottom. These are used during installation to slide the whole cylindrical structure on rails, on the top and the bottom of the ITC inner cylinder, to the centre of ALEPH.

The two halves of the detector are fixed to each other with two sets of locks made of aluminum which are located on the cable and face rings. These are designed such that they can be closed and opened with a long key from one side of the detector during installation (see figure 9).

For the installation procedure, the two halves of the vertex detector are equipped with faces and cables and tested separately. The two halves are then inserted into the opening of the ITC on side A of ALEPH using a special installation jig. The installation jig consist of mechanics which guide the two halves together around the beam-pipe such that two halves cannot touch each other in the overlap region of the faces or the beam-pipe in an undefined way as to damage the detector. The two halves are guided together and the locks are closed with the long key, at which point the cylindrical structure is sitting on an extension of the ITC rails in the installation jig.

Finally, the detector is drawn by a thin kevlar string from the rails on the installation jig onto the rails inside the ITC and moved into its final position defined by a stop near the centre of ALEPH.

4.6   The Cooling System

The distributed heat dissipation of the readout chips on the z side led to the choice of cooling the face electronics with air flowing through the detector. The air flow is generated by a pair of compressors (150 m^3/h at 25 mb overpressure) outside the ALEPH detector. It is dehumidified and filter-cleaned and then routed via $8cm$-diameter corrugated aluminum-tubing to side B of the ITC support flange. To force the air into the ITC inner bore, a thin membrane is introduced to seal the inner region. As described above, the cable and face rings have been designed to minimise the obstacles to the air flow for the VLSI electronics on the ϕ and on the z side.

Twelve temperature sensors glued to the carbon fibre shell between the two layers monitor the effect of the cooling system. Tests with mock-up faces showed that for a dissipated power of 80 W and a cooling air velocity of $v_{air} \approx 1.5 \ m/sec$ the maximum temperature gradient on the ceramics is $\Delta T_{max} \approx 6 \ K$ and the air heats up by $\Delta T_{air} \approx 3 \ K$. These values are approximately the same as the ones achieved during operation. For

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the gradient of $\Delta T_{max}(ceramics) \approx 6\ K$ the mock-up detectors were radially distorted by $\Delta r \approx \pm 5\ \mu m$ which is within the tolerance.

5   The Electronics and Data Acquisition

5.1   The Data Acquisition System

Each silicon detector module of the ALEPH detector delivers 6 pulse trains of 256 analogue pulses each, which correspond to the pulse heights measured by the CAMEX64 chip for the ϕ side (two trains) and the z side (4 trains). These 6 pulse trains are multiplexed into one pulse train by a custom-designed multiplexer unit. This pulse train is then digitised pulse by pulse using a SIROCCO IV module [14]. The SIROCCO also performs zero suppression and event formating. All the SIROCCOS are then readout by an ALEPH event builder and the digitised data are sent upstream in the standard way as described in [1].

The synchronisation of analogue sampling, CAMEX readout, multiplexing and digitisation is done with a specially designed, programmable pulse generator.

5.1.1 Multiplexer

The six pulse trains with 256 pulses each from one module have to be multiplexed into one SIROCCO input. This is to make efficient use of the SIROCCO memory range which can store up to 2048 pulses per event. Each multiplexer channel has eight analogue switches. Six are used for the module outputs, two are calibration inputs. The pulses from the six module outputs arrive all synchronously. The multiplexer switches through all the eight channels, thus converting the eight parallel pulses (including two calibration pulses) into eight short consecutive pulses. In addition the input amplifiers of the multiplexer permit adjustments of voltage offsets of the different line-drivers. This is important in order to make optimal use of the dynamic range of the ADC and in order to minimise cross talk between different channels.

5.1.2 Digitisation and Event Processing

The SIROCCO IV has a 10 bit ADC which digitises the incoming data and stores them strip by strip in its memory. Since it has 4 input buffers, it is ready to take a new event immediately after the digitisation is completed (if there is at least one empty buffer). The data are then processed by a Motorola DSP 56000 processor which performs the following tasks:

- The signals are de-multiplexed and stored in the original order as they correspond to strips on the detector.
- The signal of each strip is pedestal subtracted. Strips which are known as 'noisy' or 'not connected' are flagged.
- For each series of 256 strips (corresponding to one line driver) the common mode noise, a coherent movement of the baseline of a whole group of channels, is calculated and subtracted.
- A clustering algorithm searches for strips above a certain threshold. A cluster is defined as at least one strip above threshold plus seven strips before and after. The thresholds are defined for each line driver in order to allow for gain variations between different line-drivers. The cluster algorithm searches across boundaries defined by a line driver and ignores strips which are flagged as "noisy" or "not connected".

- The final function of the data-taking program is to follow pedestal shifts. After an event has been processed, the program loops through all channels in the event. It calculates the difference between the pedestal and the current ADC content of the channel. It then subtracts a fraction (10 %) of this difference from the pedestal. This leads to an exponential convergence of the stored pedestal to its real value.
- In special calibration runs the pedestal values of all the strips are measured and the information is stored. These pedestals are then used for the first data run after the calibration run. Periodically the updated pedestals are also stored to be used in the future runs and for monitoring.

The SIROCCOS are themselves read out and controlled by two ALEPH event-builders which provide the link to the general readout structure.

5.1.3 Performance

The CAMEX is activated 3.5 μs before the actual beam crossing in order to start the pre-sampling. The gap between the pre- and post-sampling, during which the beam crossing occurs, is about $2\mu s$ long. The readout starts after the second level trigger of ALEPH, about 60 μs after the beam crossing. At any time before the VDET can be reset and is sensitive to the next event. The readout time of the analogue information is 0.7 ms. Processing time in the DSP is less than 30 ms. The VDET data acquisition saturates at rates above 20 Hz, during practical LEP data taking no excessive dead-time is produced.

5.2 Peripheral Electronics

5.2.1 Power Supplies

The silicon detectors and their ASIC electronics are biased by a modular programmable power supply system developed by a collaboration of LABEN [15] and INFN Firenze.

The system is composed of 24 independent modules plugged in four 19" Eurocard crates. One module has two independent programmable sets of voltages, each of them is able to supply one VDET detector module.

Each Eurocard crate is equipped with a digital bus backplane, 8 transformers and one +5V power supply. The last are connected to the 220V network via a safe power device which protects the system from main voltage drops.

The Controller is programmed to execute commands received from a master computer and to monitor continuously the status of the power supply channels in the crate. If the bias current reaches the programmed current limit, the corresponding voltage is lowered.

The link between the controller and the master is of the RS232 type and realized by a duplex fibre optic cable. The four controllers are daisy chained to the master of the system.

The nine independent voltages are connected to the external loads by relays. The voltages have tow different reference grounds. One (low ground) is connected to the common bus ground and the other (high ground) to the bias voltage terminal. The voltage regulators referred to high ground are optocoupled to the bus and they are used to bias the z-side of the detector module. The voltage regulators referred to low ground are used to bias the $r - \phi$ side of a module.

The bias voltage regulator can be programmed up to 200 V and its current limit is either 200 μA or 2 mA. Two voltages, one referred to high ground, one to low ground, are used to bias the guard rings of the detectors. The CAMEX64 and line drivers are

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supplied by two tracking regulators and one positive regulator per side. The resolution of the programmed values is 1/240 of the full range. The ramping of the voltages to their final values is done by the controller.

5.2.2 Active Fanout for Analogue and Clock Signals (AFAC)

The signals (INIT, TIME, TEST) necessary for the operation of a VDET module are generated by a timing unit, and fanned out by the AFAC's. Each module has its own AFAC card, which provides the digital (TTL level), signals for the sampling and the readout cycles. Furthermore the unit generates signals, adjustable via DIP switches, to the CAMEX test inputs. Separate test signals for z and ϕ sides, and for even an odd channels are generated. This allows the output levels of the line driver chips to be adjusted to be within the correct dynamic range.

6   Running Experience

During the ALEPH data taking the VDET worked as expected. Nevertheless were had several failures of components (coupling capacitors, CAMEX chips, and line-drivers) either due to aging or malfunctioning or due to beam induced damage. During the winter shutdown periods the VDET was therefore removed and damaged modules replaced (9 in 1991/1992, 7 in 1992/1993 7 in 1993/1994 and none in 1994/1995).

Of particular concern in the operation of VDET was damage from radiation, either from total dose effects, from transient effects due to rapid beam losses, or from localised radiation damage incidents. The operational experience obtained, and the steps taken to minimise damage to the detector, are detailed in the next three sections.

6.1   Total Dose Radiation Monitoring and Warning System

As described in section 3.4.6, deterioration of the performance of VDET was expected when the total radiation dose exceeded 25 krad. To monitor the dose received in real-time, a set of four silicon photo diodes was mounted on the holding frame of the detector. This system provided a series of warnings to the ALEPH and LEP control rooms whenever the radiation level exceeded predefined thresholds. As most of the radiation is produced during injection, this system could also inhibit beam injection.

As a result of these efforts, and the improved operation of LEP, the total dose decreased from 1330 rads in 1992 to 300 rads in 1993, with 360 rads measured in 1994 and 320 rads in 1995. The total dose of 2300 rads in the four years of operation was therefore well below the danger level for the detector as a whole. However, this system could not prevent damage due to very rapid and/or very localised beam losses.

6.2   Rapid Beam Losses

A major problem area that was encountered was associated with accidental beam losses of the LEP collider. During a beam loss near the ALEPH detector the ionization of the bulk silicon can become so high that the material becomes essentially conducting. In this case the biasing potential between the ϕ and z-sides of the detector breaks down and the z-side potential approaches 0. This results in the entire bias voltage being placed across the decoupling capacitors, as the potential on the readout electronics is kept high by the power supplies. As the breakdown voltage of those capacitors is sometimes smaller than the depletion voltage, the capacitors are subject to being destroyed. This happened in several instances, with the result that the strips became DC coupled.

With the adjustment of the voltage difference between the low and high ground and the corresponding guard-ring voltages the effect of the shorted capacitors of the AC chips on the z side could be reduced to a level of $\approx$ 1%.

In order to avoid such accidents a rapid beam loss interlock system (ARBLIS) [16] was installed. A beam loss announces itself by a very fast increase of the radiation. A system of fast PIN diodes detects such radiation spikes and triggers a controlled beam dump. The beam is then ejected from LEP with fast kicker magnets in a controlled way without producing further damage. Since the installation of this system only one instance of pinhole damages has occurred. It is believed that this incident happened too quickly for the interlock system to react in time.

6.3 Localised Beam Losses

Two radiation incidents demonstrated the possibility of localised damage to the front-end electronics:

- In 1993, during an attempt to inject beam into LEP, the z readout of a module was destroyed by a highly localised "pencil" beam. The cause of the beam loss was the failure of a quadrapole located just nine meters from the ALEPH interaction point.
- In 1994, during the adjustment of stored beams in LEP, a single line-driver was destroyed as a result of a few minutes of high radiation (but well below the dose rate necessary to trigger ARBLIS).

In both incidents, the detector depletion voltage was off, but the low voltage for the front-end electronics was on. Although the exact damage mechanism is not understood, it is suspected that the front-end chips are vulnerable during these transient radiation incidents due to the presence of the low voltage. With all voltages off, there has never been damage observed, even during accelerator development periods when many severe radiation incidents were recorded. Therefore, the rule was made to leave off *ALL* detector voltages, except when taking data.

7 Offline Reconstruction

Offline reconstruction of the VDET data is organised into two steps; first reconstructing hit positions from the strip data, and then adding those hits to improve the tracks already reconstructed in the outer tracking of ALEPH. This section briefly describes the relevant features of the algorithms used. The determination of the alignment constants, whose accuracy are crucial for exploiting the VDET point resolution in the track fit, is also briefly described.

7.1 Hit Reconstruction

Because the number of electronics channels on a wafer (512) exceeds the number of strips (497), the bonding of strips onto channels is not completely constrained. In order to increase the efficiency of the detectors, dead or noisy single CAMEX channels were skipped in the bonding process. Thus, each module has its own individual bonding map relating channels to strips.

Bonding maps were recorded during the bonding process. These maps were applied to the raw VDET data as the first step in hit reconstruction, converting channel addresses into strip addresses. Raw data coming from electronics channels not connected to any strips, or from strips identified as noisy during online operation, were suppressed.

Once unbonded and noisy channels are eliminated from the data, a final common mode subtraction is performed. The final common mode is calculated using the seven

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strips read out on either side of the strips which triggered the readout of a cluster, using an iterative trimmed mean algorithm.

A final cluster search is then performed on the cleaned strip pulse height data. The offline search algorithm looks for contiguous strips with individual signals at least three times as large as the average strip noise. The sum of the pulse heights over the contiguous strips is required to be at least one quarter of the average minimum ionising signal expected for perpendicular particles. Double hits with two statistically distinct pulse height maxima are separated at this step.

Positions are then calculated from the final clusters. In the local wafer frame, the positions are calculated as the pulse height-weighted mean of all strips. These local positions are converted to global positions in the frame of the ALEPH tracking system, using alignment constants. Derivation of the alignment constants is described in section 7.3.

7.2 Track Fit

A preliminary association of reconstructed VDET hits with tracks already reconstructed in the outer detectors is done in the local wafer plane. Outer tracks are extrapolated onto the VDET wafers, using the alignment constants to precisely define the wafer positions relative to the outer tracking. All hits within a five sigma road of the extrapolated track are collected as potential matches, independently in the two readout views of the VDET. For tracks going through both VDET layers, the angle measured in the VDET is required to match within five sigma that measured by the outer tracking detectors.

The tracks are then ordered according to their transverse momentum, with the tracks having the highest value, and therefore the smallest multiple scattering errors attempted first. For each track, a precise χ^2 for the association of the track with each combination of the potential hit matches (both views and layers simultaneously) is calculated, and the association with the smallest χ^2 is taken. VDET inefficiencies are allowed with a penalty of 15 units of χ^2. Hits already associated to one track are not allowed to be associated to a subsequent track *unless* the pulse height of the hit corresponds to at least two minimum ionising particles in one view only (large pulse heights in both views come mostly from Landau fluctuations). A final calculation of the track parameters and errors including the associated VDET hits is then performed.

7.3 Alignment

To maintain the intrinsic point resolution of the VDET for use in track fitting, the positions of the wafers relative to the outer tracking chambers must be known to a few microns. ALEPH tracking data from Z^0 decays are used to determine these positions, being the most accurate and relevant information. Because the VDET hit resolution is a factor of ten better than that of the outer tracking, this alignment cannot rely solely on the outer tracking. The alignment procedure used by ALEPH therefore makes extensive use of self consistency constraints, most notably using the overlaps between wafers adjacent in ϕ. The procedure is also iterative, such that the VDET is used to improve the alignment of the outer detectors. This ensures that the relative positions of the detectors are consistent, which is essential for accurate determination of the track parameters.

The VDET alignment procedure assumes a reasonable outer tracking alignment and VDET initial position as starting conditions. Initial values for the relative positions of VDET wafers were taken from an optical microscope survey of the detector in 1991 and 1992. In subsequent years, the previous year's final alignment was used as a starting position with no loss of precision.

The alignment procedure uses both isolated tracks in hadronic Z^0 decays, and $Z^0 \to \mu^+\mu^-$ events. To improve the precision of the tracking in the $Z^0 \to \mu^+\mu^-$ events, both tracks are fit to a single helix, the total trajectory being constrained to have the momentum expected for a μ pair, by the known beam energy.

Tracks which go through the $\sim 5\%$ overlapping active area between wafers adjacent in ϕ are used to constrain the relative positions of those wafers, without any reference to the outer tracking. Used together, the overlaps also constrain the average radial position of both layers of wafers. Single-fit $Z^0 \to \mu^+\mu^-$ tracks constrain the relative positions of the two layers with each other, again with no reference to the outer tracking.

Using only the angle measurement from the outer tracking, the relative positions of the $z > 0$ and $z < 0$ halves of the detector are constrained. This constraint uses both the single-fit $Z^0 \to \mu^+\mu^-$ events and tracks which, because of a primary vertex displaced from $z = 0$, pass through the different layers of the VDET in opposite halves. These constraints also control possible shear and twist distortions in the VDET internal alignment. Finally, to determine the position of the VDET as a rigid body relative to the outer tracking, constraints from normal hit-track residuals are also included.

All of the different constraints on the wafer positions are applied simultaneously in the alignment fit. The fit is iterative, adjusting each wafer one at a time while its neighbours and the outer tracking are kept fixed. Convergence is defined when, after looping through all the wafers, none have changed position relative to the previous iteration by more than a few microns. By construction, this fit defines simultaneously the local and global VDET wafer positions. From reasonable starting values, the alignment fit typically converges in under 20 iterations. To achieve a statistical accuracy below the estimated systematic limit of the method (a few microns), the alignment is performed using $\sim 20{,}000$ $Z^0 \to q\bar{q}$ events and ~ 4000 $Z^0 \to \mu^+\mu^-$ events.

When the VDET has been aligned, it is then used to improve the alignment of the outer tracking detectors. The four hits from both tracks in $Z^0 \to \mu^+\mu^-$ events are fit to a single helix, constrained to the known beam energy, extrapolated to the outer tracking detectors, and used to constrain their position and internal parameters. After adjusting the outer tracking, a final iteration of the VDET alignment is made using the improved outer tracks. This iterative method insures consistency between the detectors, and thereby good track fits.

8   VDET Performance

This section presents some results on the performance of the VDET in its operation see also [13] for the VDET performance in the context of the rest of ALEPH. The measurement of basic parameters such as the efficiency, signal to noise ratio, and resolution are first described. Then a brief description of some of the physics results in which the VDET has played an important role are described.

8.1   Detector Parameters and Precision

The VDET single-track efficiency by module for the two views, measured in $Z^0 \to q\bar{q}$ events taken during the 1994 ALEPH run is shown in figure 10. To make this plot, tracks fit using only the outer tracking are selected. The tracks are required to have at least 1 GeV/c momentum, to extrapolate inside a five sigma (outer tracking error) fiducial area inside the wafer active area, and to have no other tracks within a five sigma square around their extrapolation point. The track is considered to match a VDET hit if the hit is within three sigma of the track extrapolation point. Using this definition, the average module
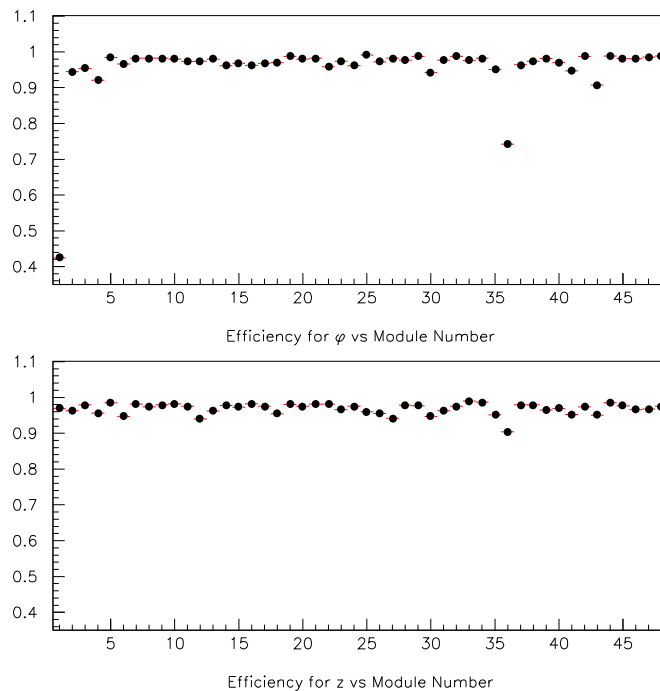
Figure 10: Efficiencies for modules in $r - \phi$ and $r - z$ views for data from 1994. Mean $r - \phi$ efficiency is 95.9 %, mean $r - z$ efficiency is 97.3 %. The low efficiency of module ϕ–1 is due to a radiation damaged line driver chip (see 6.3), and that of ϕ–36 due to the low gain of one half of the line driver. These two low efficiency modules are responsible for the efficiency difference between the ϕ and z sides.

efficiency is 95.9 % for the $r - \phi$ view, and 97.3 % for the $r - z$ view (these means include the two highly inefficient modules on the ϕ side, hence the lower ϕ efficiency).

The signal to noise ratio can be inferred from figure 11, which shows the pulse height distribution for the clusters associated to the matched hits. This plot can be used to calculate the signal/noise in two ways; first, by dividing the most probable pulse height sum value by the per-channel noise measured online, and second by comparing the $r - \phi$ view pulse height with the $r - z$ view pulse height. Both methods give compatible answers of $\mathcal{S}/\mathcal{N} \cong 15$.

Figure 12 shows the estimated amount of material encountered by tracks in $Z^0 \to q\bar{q}$ events as they go through the VDET, expressed in radiation lengths. The plot uses the measured trajectories of all reconstructed tracks together with a detailed model of the location and amount of material present in the VDET wafers and all their support structures to predict the amount of material seen by each track. The most likely amount of material is ~ 2 % of a radiation length, whereas the tails pull the average up to ~ 3 %. The tails come from tracks which hit support ribs or dense electronics elements (tantalum capacitors). The estimate of the absolute amount of material in the VDET used above was verified by comparing the number of photons which convert in the VDET to the number which convert in other, simpler, regions of ALEPH (i.e. in the TPC field cage).

Figure 13 shows the residual distribution for VDET hits generated by tracks going through the overlap region. These tracks were selected to have close to normal incidence on the wafers in the plane of the residual measurement, but otherwise are the same isolated $Z^0 \to q\bar{q}$ tracks used in the above efficiency and $\mathcal{S}/\mathcal{N}$ measurements. A Gaussian fit to
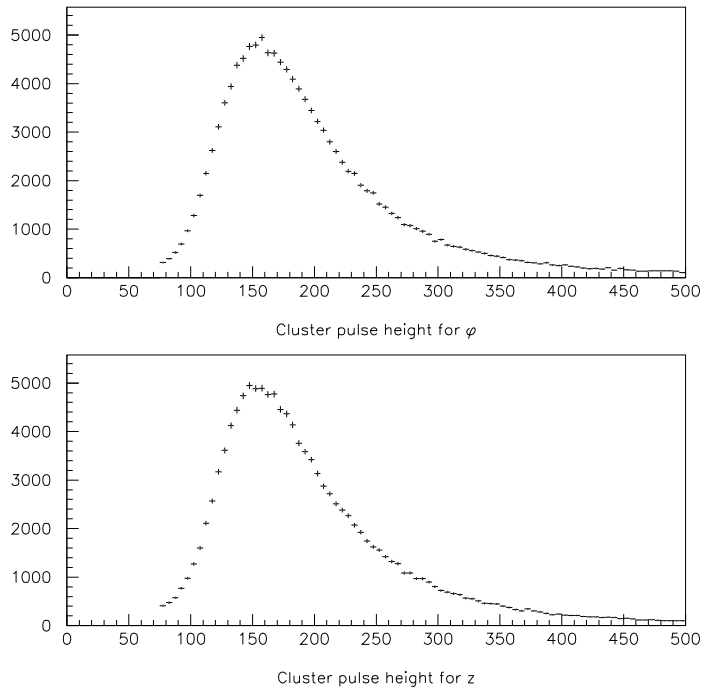
21

Figure 11: Pulse heights (ADC counts) for hits matched to tracks in $r - \phi$ and $r - z$ views. $\mathcal{S}/\mathcal{N}$ can be inferred by comparing to known values of the noise (about ten ADC counts).
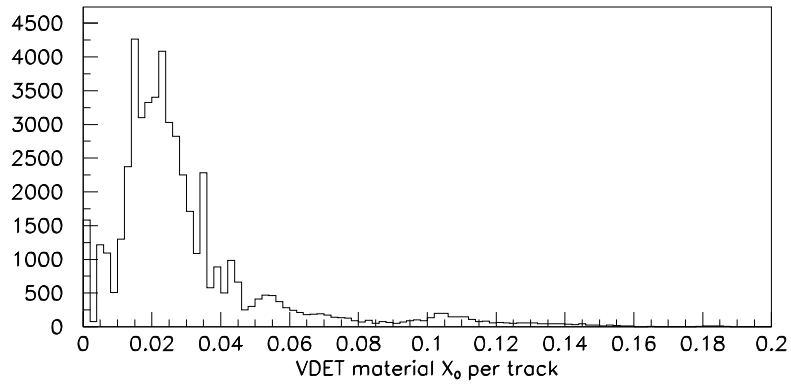

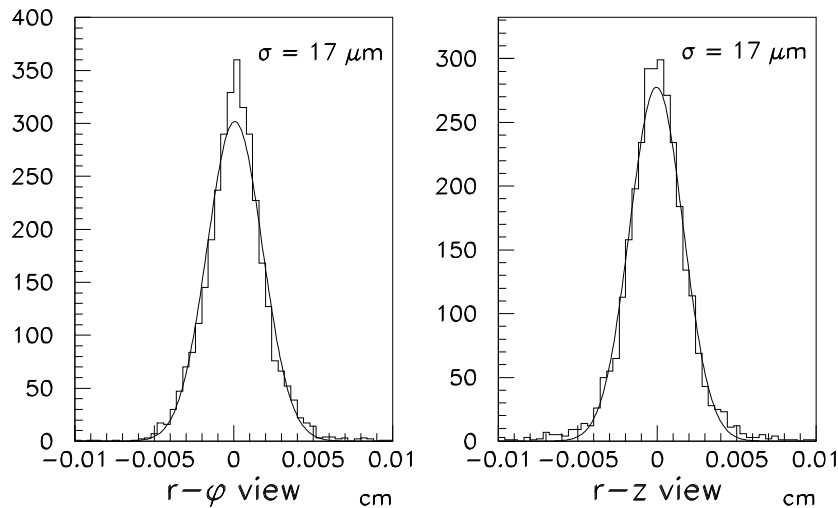Figure 12: Estimated radiation length in the VDET traversed by tracks in $Z^0 \rightarrow q\bar{q}$ events.

Figure 13: The VDET hit separation for tracks passing through overlapping wafers in the (a) $r - \phi$ and (b) $r - z$ views.

the distributions implies an average VDET point resolution of ~ 12 μm, in both views at normal incidence including all intrinsic and alignment effects.

Figure 14 shows the distance between the two tracks in $Z^0 \rightarrow \mu^+\mu^-$ events, measured near the Z^0 decay point, for tracks with VDET hits in both layers. A Gaussian fit to the distributions implies an impact parameter resolution, in the plane transverse to the tracks, of 23 μm in the $r - \phi$ view, and 28 μm in the $r - z$ view, for high momentum tracks. Comparing the measured momentum of these tracks with the known beam momentum gives a momentum resolution of $\sigma(p_\perp)/p_\perp = 0.6 \times 10^{-3}(\text{GeV/c})^{-1}$.

Figure 15 shows the measured impact parameter resolution of tracks in $Z^0 \rightarrow q\bar{q}$ events with VDET hits in both layers as a function of their momentum. The impact parameter is measured relative to an event-by-event reconstructed Z^0 decay vertex. The resolution may be considered as the standard deviation given from a Gaussian fit to the impact parameter distribution for tracks with no apparent lifetime (i.e. tracks which cross the thrust axis behind the primary vertex), subtracting the estimated primary vertex resolution in quadrature. The resolutions can be parameterised as;

$$\sigma \;\; = \;\; 25\mu m + \frac{95\mu m}{P(\text{ GeV/c})^{-1}} \tag{1}$$

in each of the two views. The resolution is of course also heavily dependent on the polar angle of the track, remaining about constant in the region of $\sin \lambda < 0.4$ with a value of about $14\mu m$ and then rising to a value of $50\mu m$ for $\sin \lambda = 0.8$.

8.2 Contributions to Physics

The vertex detector has made a number of significant contributions to physics results of the ALEPH experiment.

The measurement of the $Z^0 \rightarrow b\bar{b}$ width ($\Gamma_{b\bar{b}}$), was made by identifying b events using an impact parameter lifetime tag. The VDET was essential to the precise measurement of the impact parameters of the tracks in these events. The results are discussed in [17].
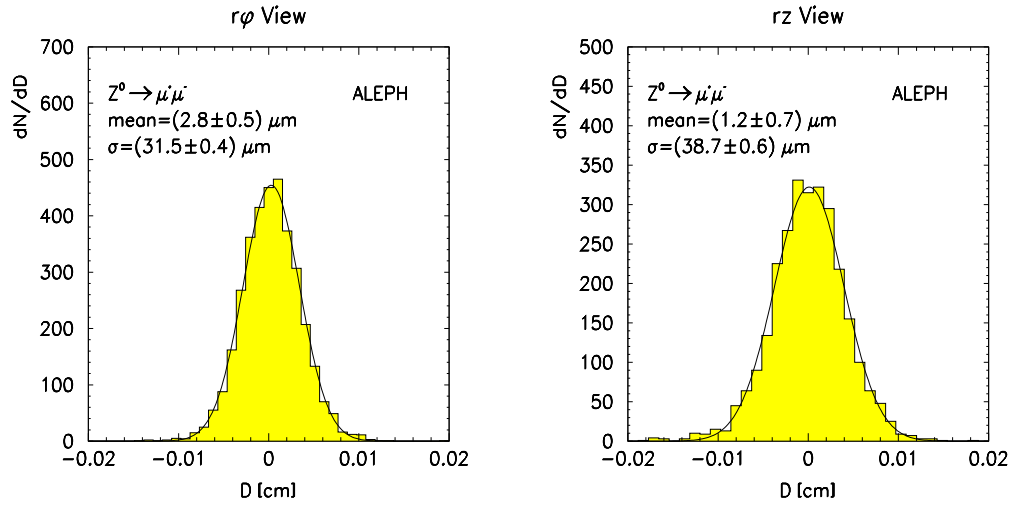
Figure 14: Miss distance for the two tracks of $Z^0 \rightarrow \mu^+\mu^-$ perpendicular to the track direction in the (a) $r - \phi$ and (b) $r - z$ views.
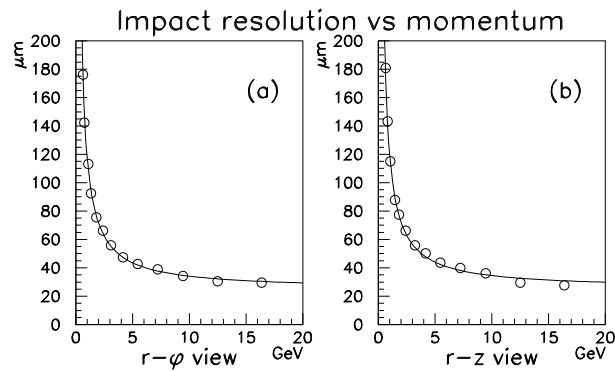

Figure 15: The impact parameter resolution for tracks with VDET hits in two layers as a function of their momentum.

The forward backward asymmetry for $Z^0 \to b\bar{b}$ was measured [24] by tagging $b\bar{b}$ events using their lifetimes, and using the hemisphere charge.

ALEPH was the first experiment to observe B_d^0 mixing directly, by looking at the final charge-conjugation state of B^0 mesons as a function of decay length. In addition, using similar methods, limits have been placed on the strength of B_s^0 mixing. Several papers have been produced on the subject, see [18].

Precision measurements of the inclusive lifetime of b- hadrons [19], and of the lifetimes of B^0, B^- [20], B_s [21], and b-baryons [22], have been made using the VDET to make the decay length measurement. The lifetime of the τ lepton has also been measured [23]

In all of these measurements the VDET has allowed the precision of these measurements to be increased, or in some cases been instrumental in allowing the measurement to be made at all.

9   Conclusions

The detector described in this paper was successfully used in the ALEPH experiment between 1991 and 1995. The operation of the detector demonstrated the principle, and advantages of the use of double sided wafers in a silicon vertex detector, giving very good spatial resolution in two coordinates. Since then double sided detectors have been applied in other experiments as well, and have become a standard technology.

Running experience has been generally good, with few fundamental difficulties occurring in the design. Only the sensitivity to large transient radiation exposure proved to cause problems, and this was avoided by changes to running philosophy and operation.

In ALEPH the vertex detector has played a vital role in the measurement of B-hadron and τ lifetimes, of direct B_d^0 mixing and limits on B_s^0 mixing, of the value $\Gamma_{b\bar{b}}$, and of limits on the existence of new particles.

In November the detector came to the end of its service. At this time it was replaced with an upgraded detector, operating on the same principles. The new detector has larger solid angle coverage, less material in the fiducial region, and better radiation resistance.

The good operation of the first ALEPH silicon detector has successfully demonstrated the principle of double sided detectors, and provided essential to a number of physics results at precisions that would otherwise not have been possible.

Acknowledgements

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