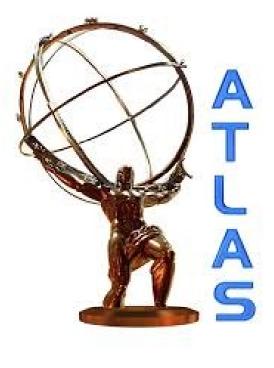
An introduction to ATLAS trigger

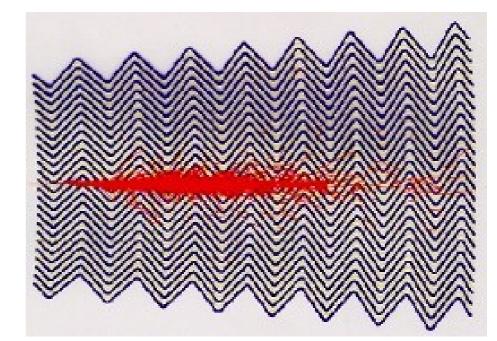
Juraj Bracinik (University of Birmingham)



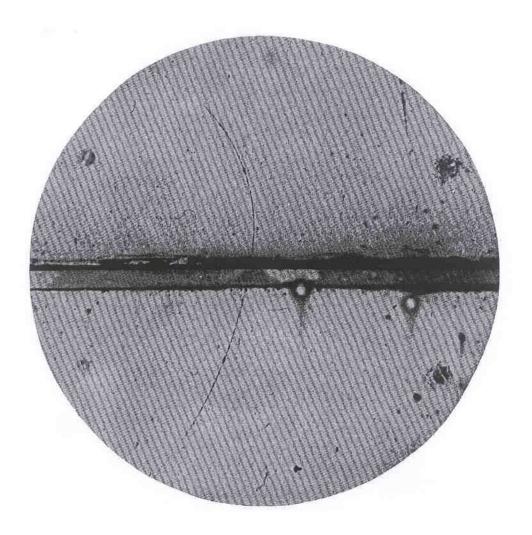
Triggering Discoveries in High Energy Physics III, Nový Smogovec, Slovenská Republika, 11/12/2024



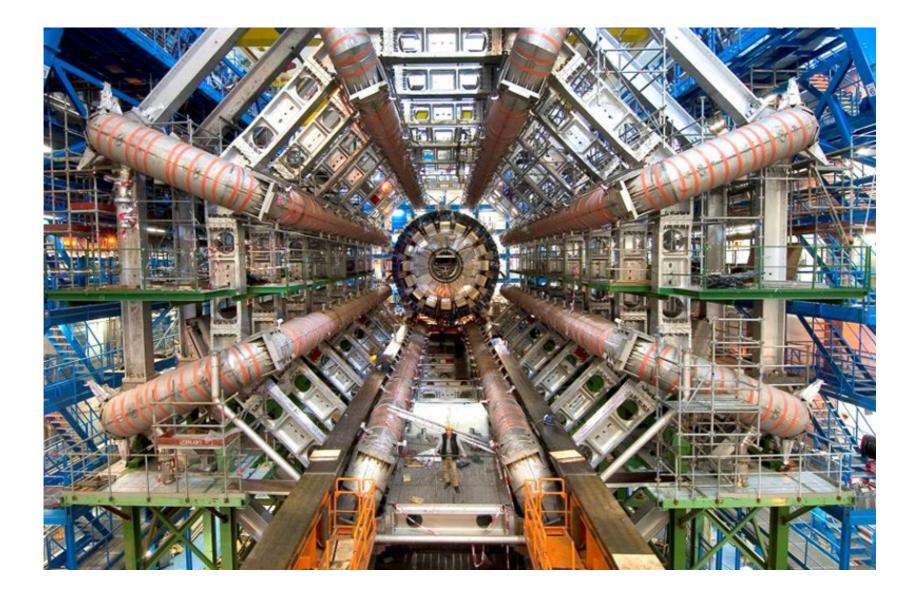




Introduction



Discovery of positron



<u>What are these lectures going to be?</u> (maybe ...)

- Structure of the talk:
 - An introduction to the LHC and ATLAS detector
 emphasis on triggering
 - ATLAS trigger, architecture and performance
 - More detailed look at L1 Calorimeter Trigger, its evolution and recent upgrades
 - This is what I work on, sorry...

LHC and ATLAS

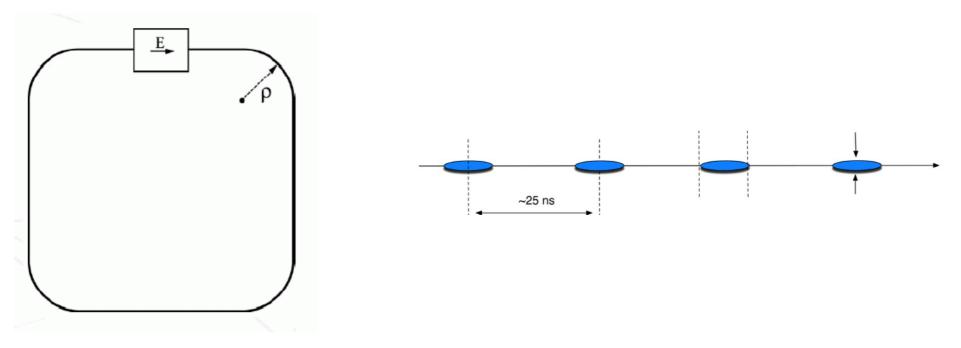
Large Hadron Collider, design parameters



LHC nominal parameters

at collision energy p, Pb Particle type Proton energy E_p at collision 7000 GeV 1 x 10³⁴ cm⁻²s⁻¹ Peak luminosity (ATLAS, CMS) Circumference C 26 658.9 m Bending radius p 2804.0 m RF frequency f_{RF} 400.8 MHz # particles per bunch n_n 1.15 x 10¹¹ 2808 # bunches n_b

LHC beam, bunch structure



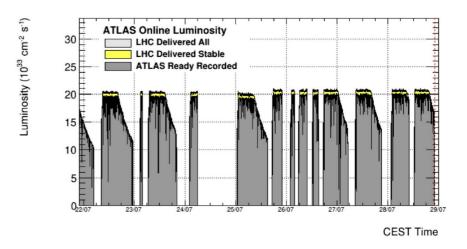
LHC is a synchrotron, acceleration power provided by RF cavities

- Beam need to be organised into bunches
- Bunch length ~10cm
- Transversal dimensions much smaller (~100 µm at collision points)
- time between bunches (1/ LHC clock frequency) is 25 ns

LHC beam, bunch trains and levelling

- Complicated structure of bunches:
 - 3564 full number
 - Around 2800 filled
 - Reflecting pecularities of beam injection and dumping
- Data taking revolves around
 LHC fills:
 - Injection, acceleration, bring beams to collision
 - Flat (levelled) part of the fill, constant luminosity
 - Using both separation and
 β* levelling
 - Then exponential decay





Phases of ATLAS data taking ...

- Run 1 (2009-2013):
 - ✓ S up to 8 TeV, L up to 0.77×10³⁴ cm⁻²s⁻¹, <µ> ~ 21 BC⁻¹ (peak <µ> ~ 40 BC⁻¹)
- Phase 0 upgrade (LS1, 2013-2015)
- Run 2 (2015-2018):

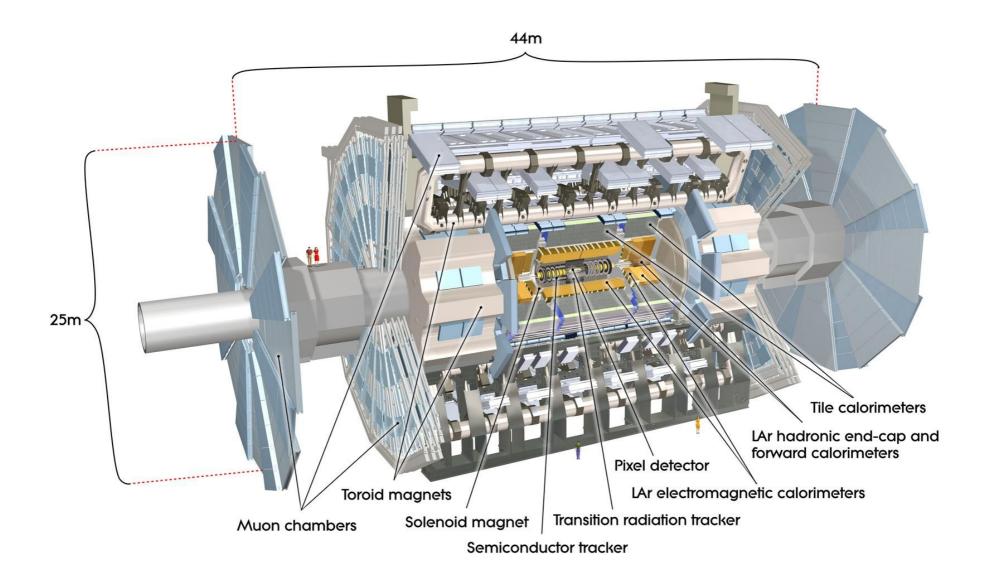
→ $\int s = 13$ TeV, L ~ 2x10³⁴ cm⁻²s⁻¹, <µ> ~ 60 BC⁻¹ (levelled)

- Phase 1 upgrade (LS2, 2018-2022)
- Run 3(2022-2026):
 - L ~ 2-3 x10³⁴ cm⁻²s⁻¹, <µ> ~ 60-70 BC⁻¹ (levelled)
- Phase 2 upgrade (2026-2030)
- Run 4 (2030-2033)

<u>م</u>

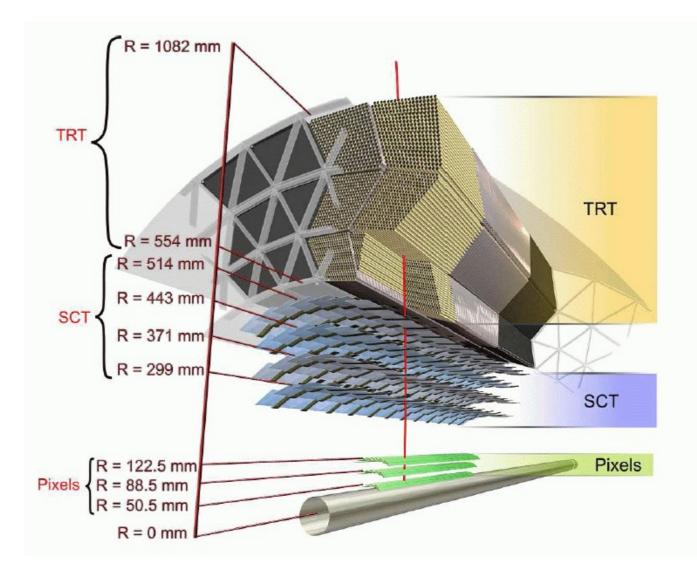
- L up to 7.5×10^{34} cm⁻²s⁻¹, <µ> up to 200 BC⁻¹

ATLAS detector

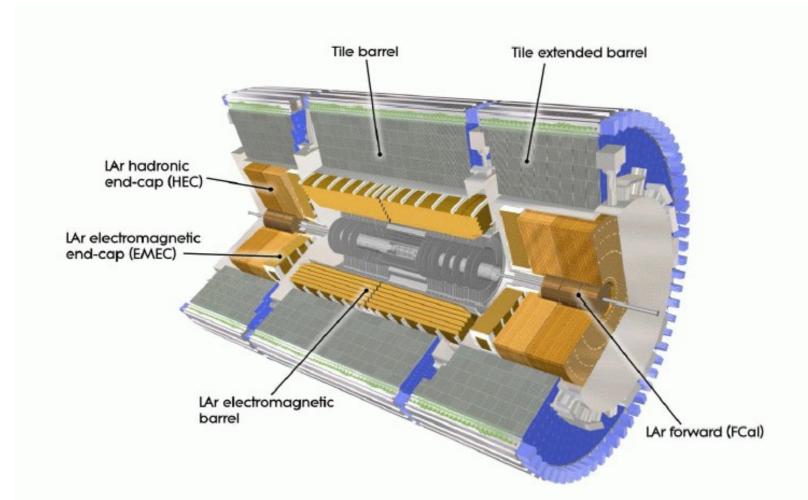


ATLAS tracking (Run 1)

- Low radius pixels (3 layers in Run 1, another layer inserted in 2015)
- Then strips (SCT)
- At larger radius, additional detector - TRT (transition radiation tracker)

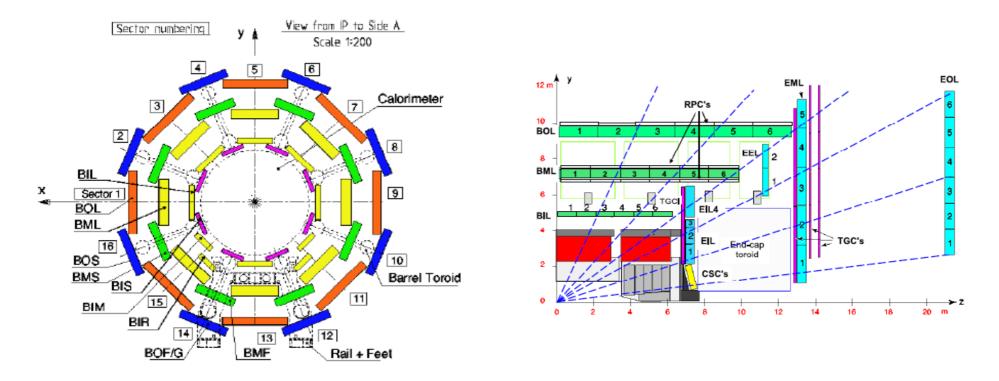


ATLAS calorimetry



- Located outside of solenoidal magnet
 - Mostly based on LAr technology
 - In hadronic barrel Iron+Scintilation tiles (TileCal)

<u>ATLAS muon system (Run 1)</u>



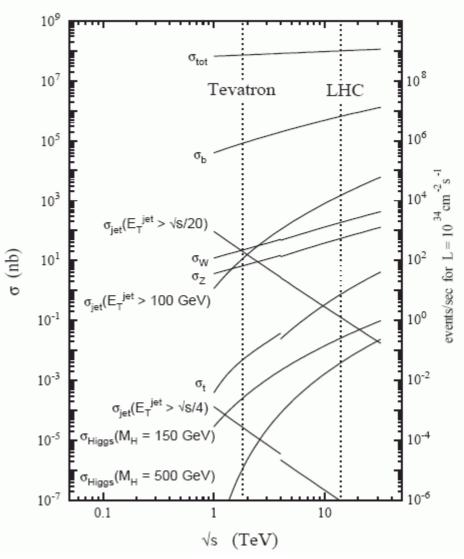
- Reasonable quality of tracking over huge volume of non-uniform magnetic field:
 - Gas drift chambers for precision position measurement (MDT's and CSC's in forward region)
 - Dedicated fast chambers for triggering (RPC's and TGC's in forward region)

ATLAS trigger, design and performance

Triggering ...

- At full LHC luminosity, huge event rate
 - Each bunch crossing at 40 MHz results in many (reaching ~65 in 2024) inelastic collisions
- ATLAS has around 100 Million electronics channels to be read out
 - Event size typically 1-2 MB
- Possible data recording rates are of the order of 1kHz
 - Need on-line filter (trigger) deciding which events should be saved on disk

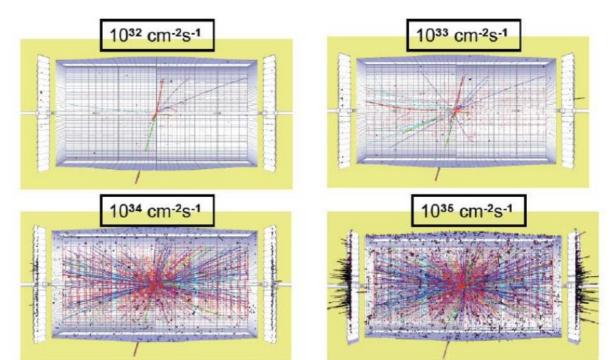
proton - (anti)proton cross sections



Trigger signatures

Typically search for signatures like:

- high-p⊤ muons
- high-p_T electrons and photons
- → High-p_T taus and jets
- → Large missing E_T



Want to retain as many as possible events for:

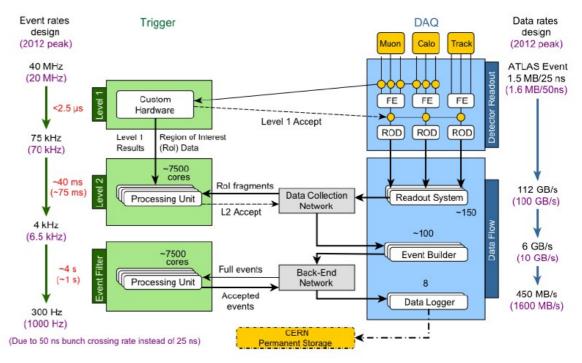
- Higgs physics
- SUSY searches
- Searches for any new physics
- Precision physics studies

<u>Multi-level trigger</u>

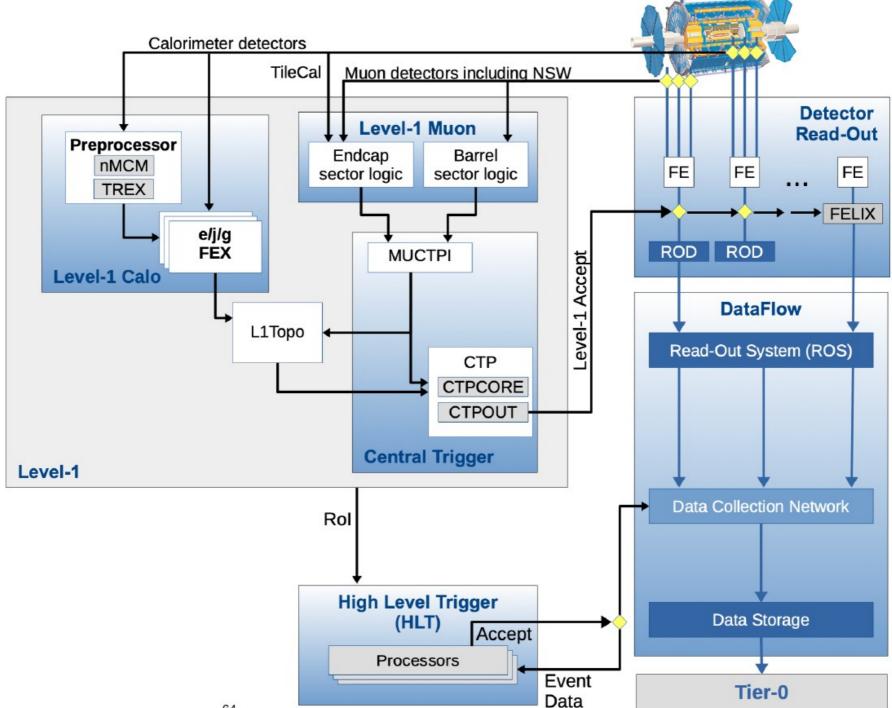
ATLAS trigger during Run1

Multilevel triggers are used everywhere!

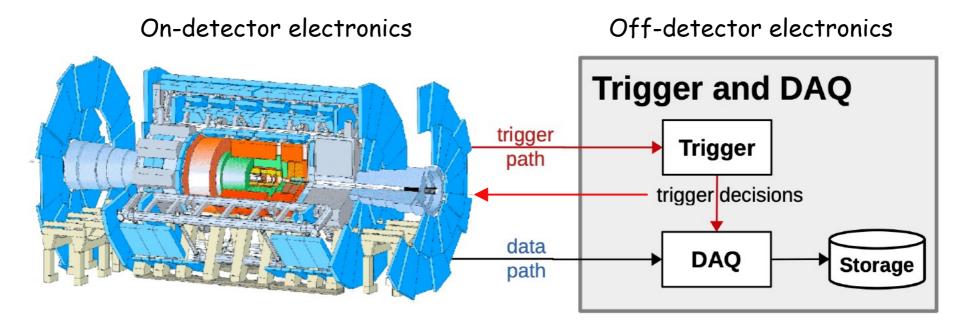
- Rapid rejection of high-rate backgrounds without too much of a dead time
- High overall rejection power



- First-level trigger custom electronics
- Level-2 and Event Filter (L3) built using computers (Linux PCs) and networks
- In Run 1 L2 and L3 were separate objects, now logic separation only



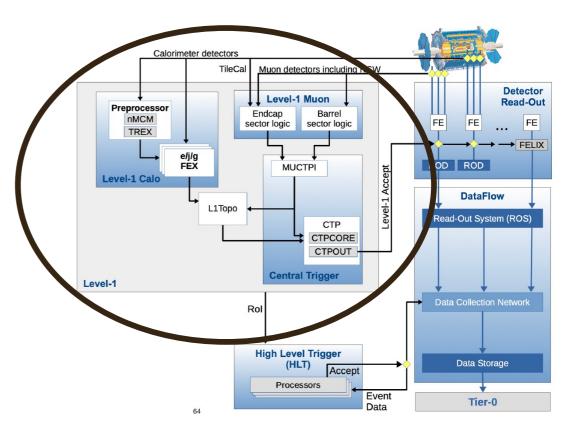
Trigger and Data Acquisition



- Two data paths
 - Low latency: Trigger path
 - Dedicated detectors or reduced granularity information
 - Mainly used by L1 trigger and seeding of High Level Trigger
 - Slower, large latency, precise: Data path
 - Used by High Level Trigger and for precision analysis

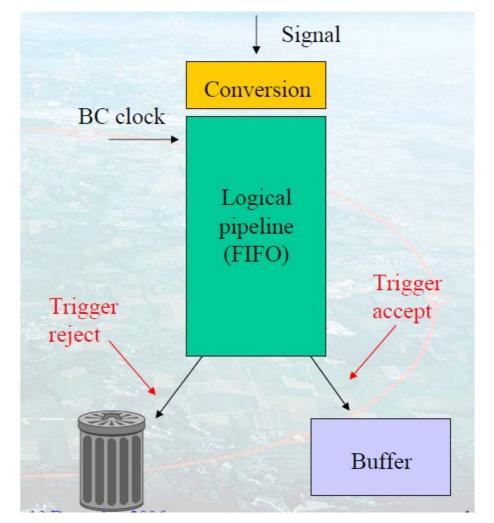
Level 1 trigger I

- Dedicated hardware
- Inputs from:
 - Dedicated detectors (RPCs and TGCs) for muons
 - reduced granularity calorimeter information
 - No tracking information used
- Main components:
 - L1Muon system (muons)
 - L1Calo (EM, TAU, Jets, E_{Tmiss})
 - L1Topo (multiplicities cuts and topological conditions)
 - Central Trigger (clock distribution, prescales, combination of triggers, busy logic, ...



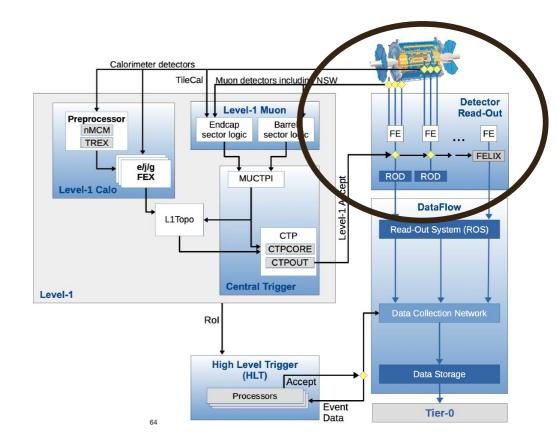
<u>Level 1 trigger II</u>

- Fixed latency, pipelined system:
 Processes each bunch-crossing
 - During fixed latency time (2.5 μs)
 detector data stored in 'pipeline memories' on detector itself
 - The triggered data is taken out from pipeline at a fixed time
 - When L1 trigger accepts an event, data is sent to derandomiser buffers off detector
 - Selects about 1 in 500 events
 - Also flags Regions-of-Interest (RoIs)



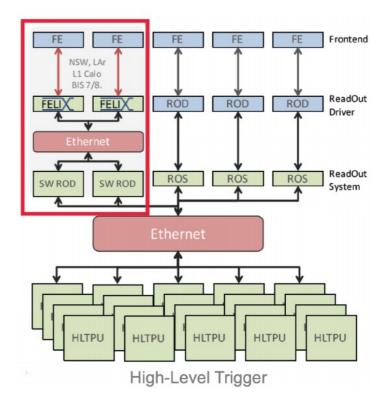
When L1 accepts ...

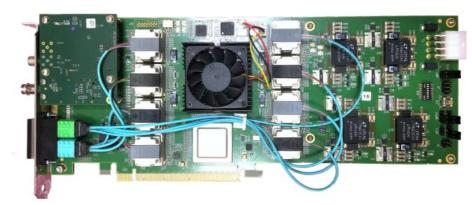
- In case of positive decision by L1 trigger:
 - Central Trigger (CT) sends signal (L1A) to all detector front-ends
 - This initiates read-out
 - Data from all pipe-lines are copied into Read-Out Buffers
- In the case of negative decision:
 - No dedicated signal
 - Pipe-lines are eventually overwritten with new data



ATLAS readout system

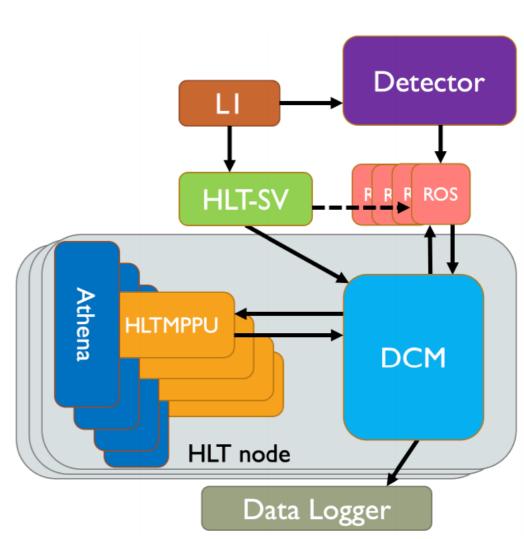
- Original architecture:
 - ≁ RoD
 - System specific card, usually VME
 - About dozen types
 - Connected to RoS
 - Commodity computers hosting ROBin cards
 - Storing data fragments and transfering them to HLT
 - About 100 servers in USA15 cavern
- Upgraded architecture:
 - FELIX
 - Custom PCIe card hosted in commercial servers
 - Currently ~100 cards in ~60 servers in USA15
 - Software RoD
 - Software running on a PC
 - Currently 33 servers in USA15





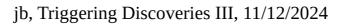
<u>High Level Trigger – infrastructure I</u>

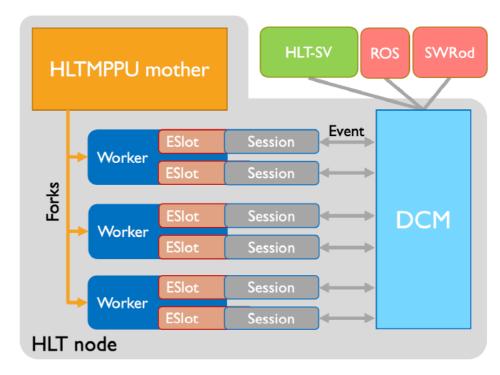
- Highly parallel multi-core architecture:
 - HLT_SV (High-Level Trigger Supervisor):
 - One unique application
 - Assigns event to HLT nodes
 - Responsible for distributing L1 RoI information
 - DCM (Data Collection Manager)
 - Interface between HLT processing units and the rest of DAQ
 - Retrieves RoIs from HLTSV and event fragments from readout system, provides them to Processing Units (PUs)
 - Performs event building for selected events
 - Sends full event to the Data Logging System
 - One application running on each HLT processing note
 - Single thread
 - Communication with PU through shared memory



<u>High Level Trigger – infrastructure II</u>

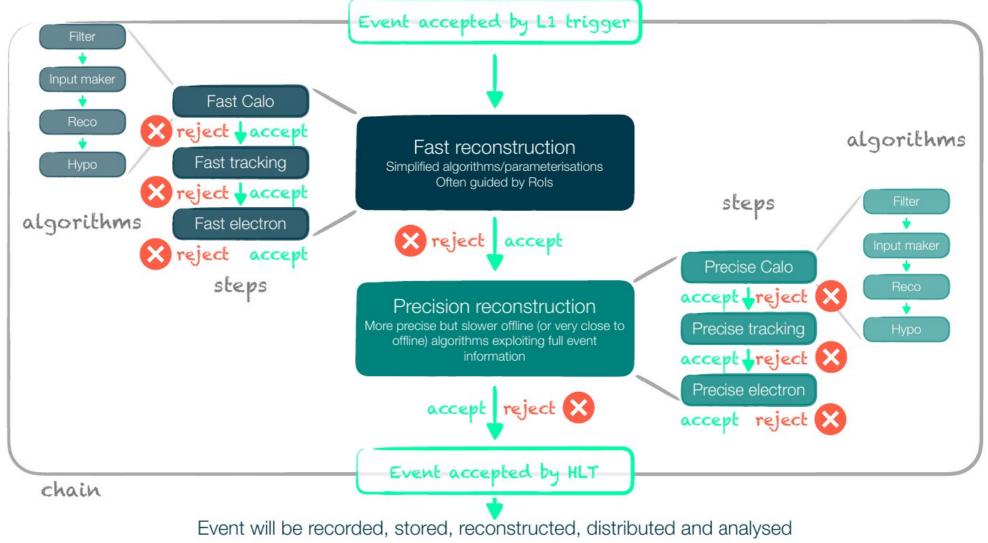
- One mother process per HLT node (HLTMPPMU mother)
 - Forks n child processes (workers) and monitors them
- Workers:
 - Are in charge of event processing
 - Each of them can run multiple threads typical setup in 2024:
 - Processing slot == core on computer
 - 32 slots/node each running 2 threads
- Minimal nr. of nodes determined by event rate and processing time:
 - Input rate> * <processing time> = <min nr of nodes>
 - 100 kHz input rate, 500 ms average processing time (to be compared with 2.5 µs fixed L1 latency)
 - >50 000 HLT processing nodes





HLT: CHAINS, STEPS & ALGORITHMS

example: simple electron trigger chain



jb, Triggering Discoveries III, 11/12/2024

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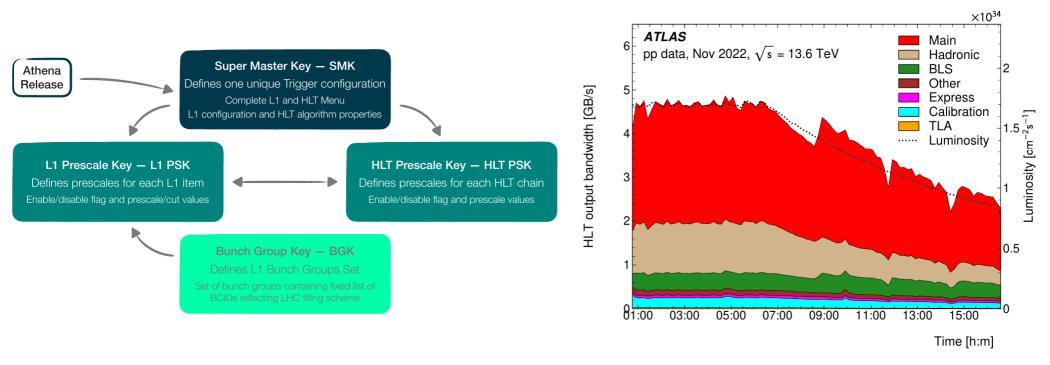


Data Logging System

- Stores events accepted by HLT and transfers data files to Offline Storage Systems
 - Decouples ATLAS data-taking from offline world
 - 48 hours of storage in case of connection problems
 - Implemented in 10 servers (SFOs) with directly attached storage systems (240 hard drives)
 - 8 GB/s writing (O(1) kHz of events)
 - Fully redundant system for high reliability
 - No data loss in more than 10 years!



Trigger settings adjustment during fill



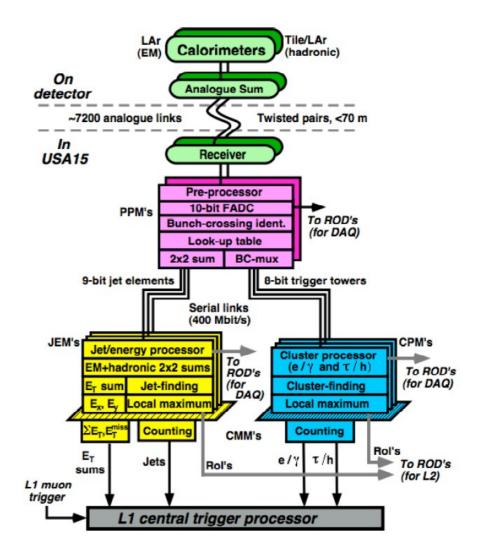
More details here

- For each fill fix basic trigger configuration (SMK)
 - Stay with the same L1 and HLT prescale keys during levelling stage
 - Update prescale keys at predefined points during exponential luminosity decay phase

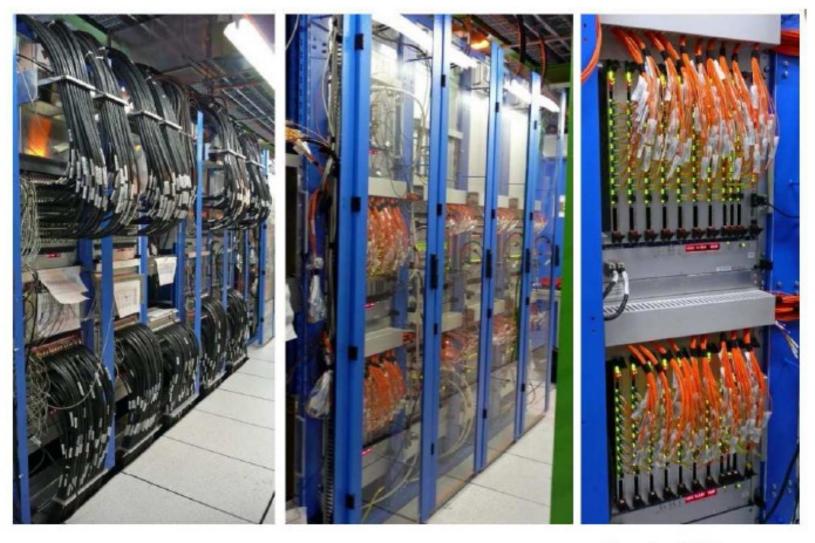
More detailed look at L1Calo and its evolution

<u>Level 1 Calorimeter Trigger (L1Calo during</u> <u>Run1)</u>

- Synchroneous pipelined hardware trigger with fixed latency
 - Implemented as custom electronics (mainly VME, FPGAs, few ASICs)
 - Input are pre-summed analogue signals from all ATLAS calorimeters
 - Pre-processor:
 - Digitization and conditioning of input signals
 - Cluster processor:
 - looks for isolated energy maxima corresponding to electrons and taus
 - Counts their multiplicities
 - Jet processor:
 - Finds Energy maxima jets, count multiplicity
 - Calculates Global sums ETmiss, ETtot
 - Compares with loaded thresholds
 - Processors send their outputs to Central Trigger



L1Calo trigger during Run 1



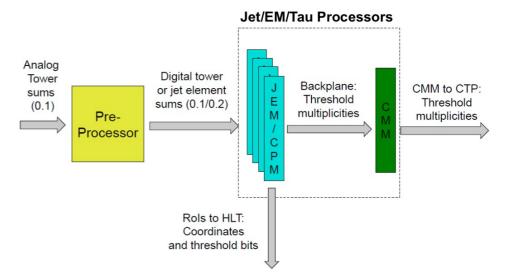
(Half of) Receivers and PreProceccors Processors

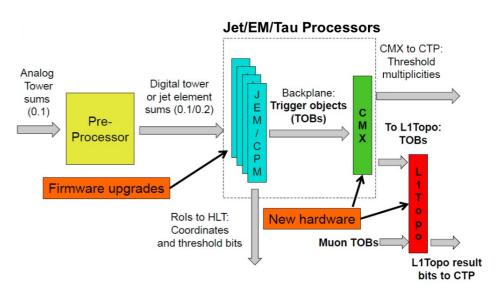
Readout Drivers

~300 VME modules of 10 types housed in 17 VME crates

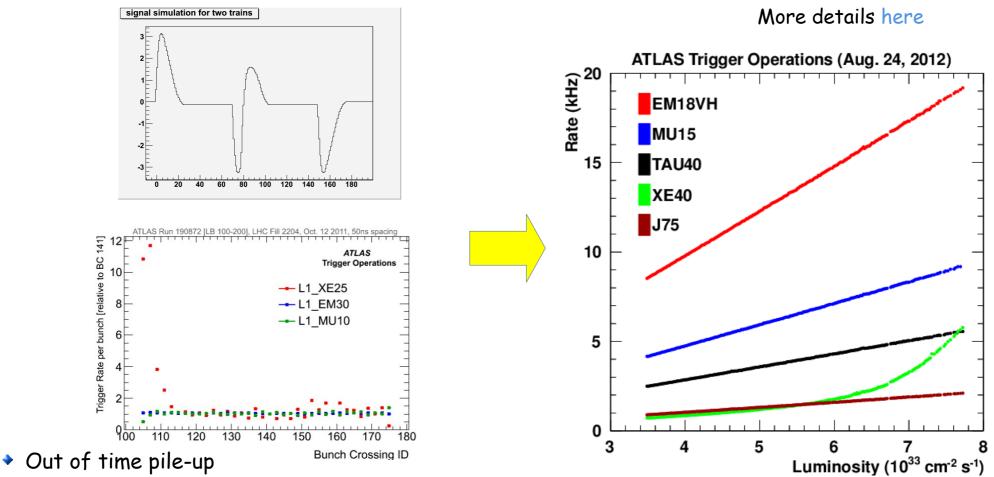
Phase 0 upgrades of L1 trigger

- Major upgrade of L1 Calorimeter trigger:
 - Improved treatment of input analogue pulses
 - nMCM (Multi Chip Module) upgrade in Preprocessors
 - Different definition of trigger objects:
 - Firmware update of processors and new merger (CMX) boards
 - Improvements to trigger algorithms
 - For example new calculation of electron isolation
 - New topological trigger (L1Topo)



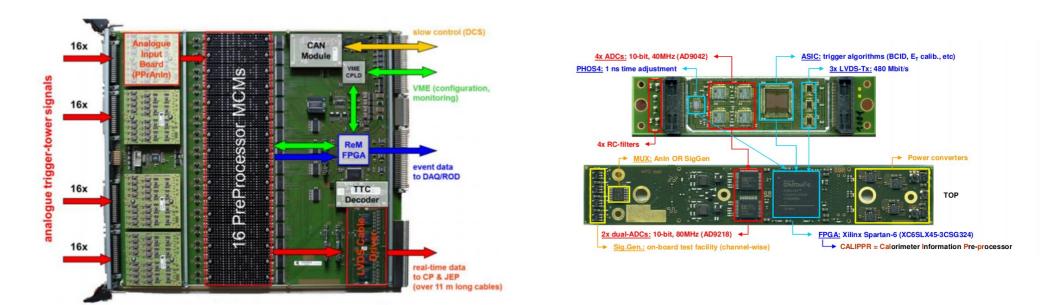


Out of time pileup and effect on baseline



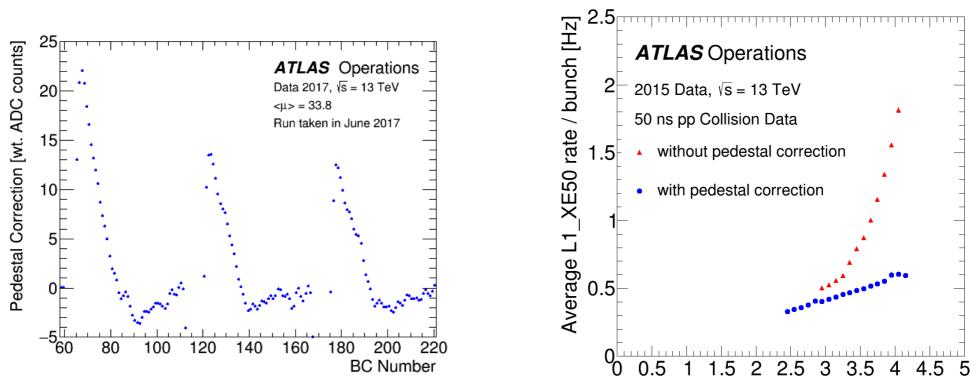
- Signals from LAr are bi-polar and extend over several bunch crossings
- In combination with LHC bunch train structure leads to shifts of base-line at the beginning and end of bunch trains
 - Seen as non-linear component of trigger rates

Upgrade of PP Multi Chip Modules



- Input signal conditioning, digitization and filtering done in PreProcessor daughterboards - Multi-chip-modules (MCMs)
- All being replaced by new FPGA oriented design (nMCM):
 - Better signal conditioning
 - Better pile-up filtering, taking into account pileup autocorrelation matrix
 - Better BC identification for saturated pulses
 - Dynamic baseline correction!!!

Overall improvement in L1 triggering

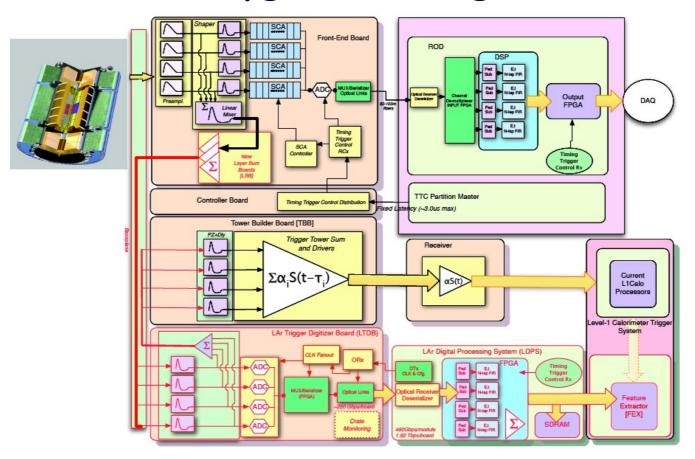


Instantaneous luminosity / bunch [10³⁰ cm⁻² s⁻¹]

More details here

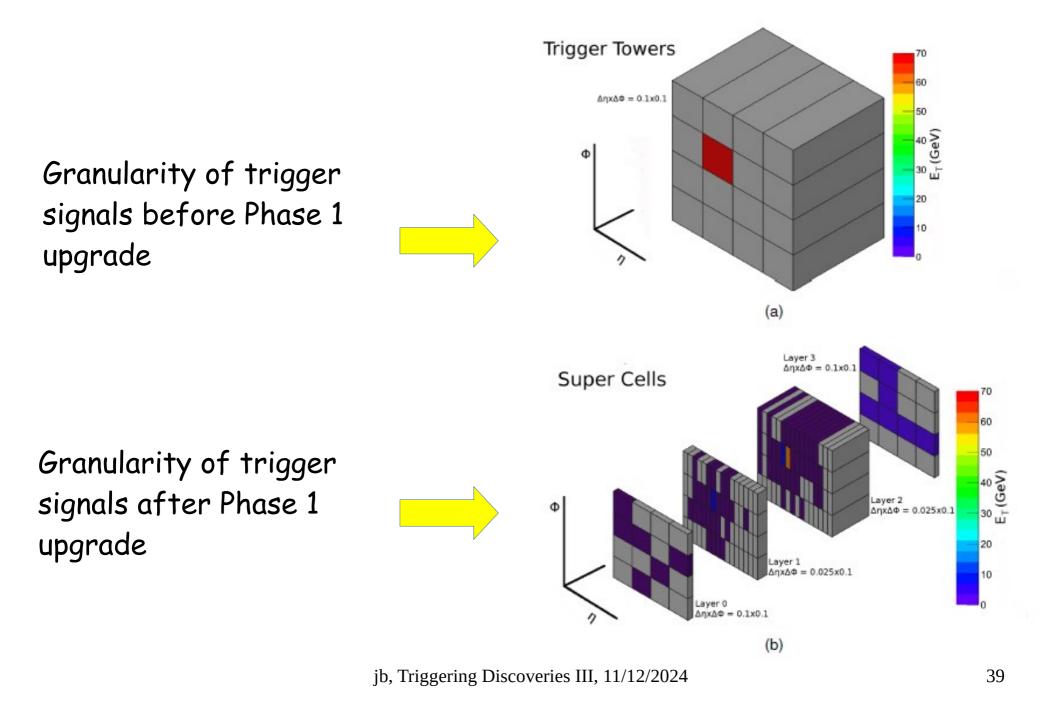
- Baseline (pedestal) correction calculated for each BC
- Average correction calculated over history of 65536 LHC orbits (~6s)
 - Subtracted from FADC counts before the tower energy is sent to digital processors
- Major improvements of global and multi-object rates!

<u>Phase I upgrade – Long Shutdown 2</u>



- Major upgrade of LAr front-end electronics during LS2 (2018-2022)
 - Keeping old (legacy) analogue path untouched (almost)
 - New digital path
 - Digitisation of trigger signals on detector, improved granularity
 - Trigger Towers to SuperCells
 - Same latency of 2.5 µs as before Phase I upgrade

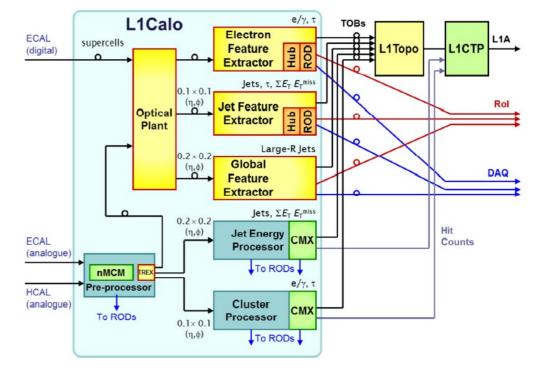
Phase I, changes to input signal granularity



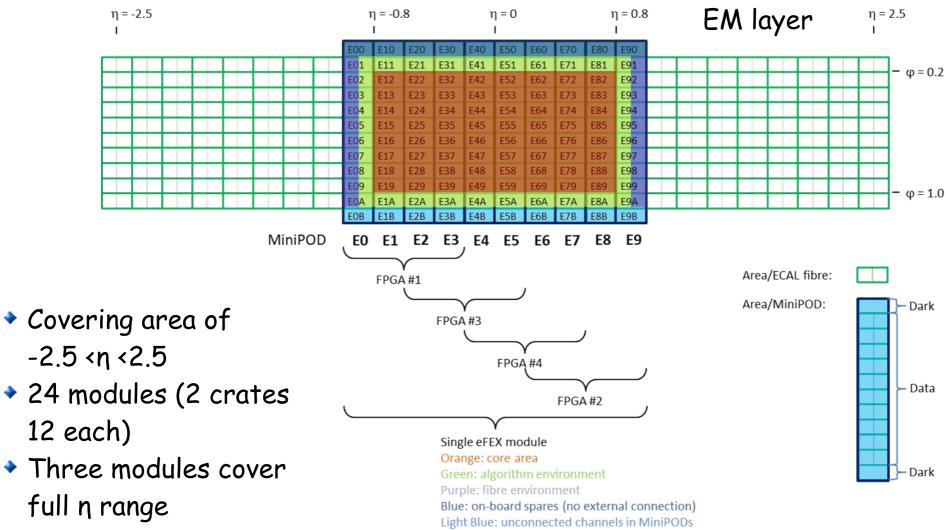
Phase 1 upgrades of L1Calo trigger

- To fully benefit from digital trigger signals from Lar new digital trigger processors built
 - Efex electrons, photons and hadronic taus
 - Jfex jets, forward electrons and global sums
 - Gfex wide jets and global sums
- Gradual move from old to new system:
 - At the beginning of Run3 used legacy
 - In 2023 started to switch over
 - Migration finished in 2024, legacy system not used any longer
 - In next slides will focus on eFex

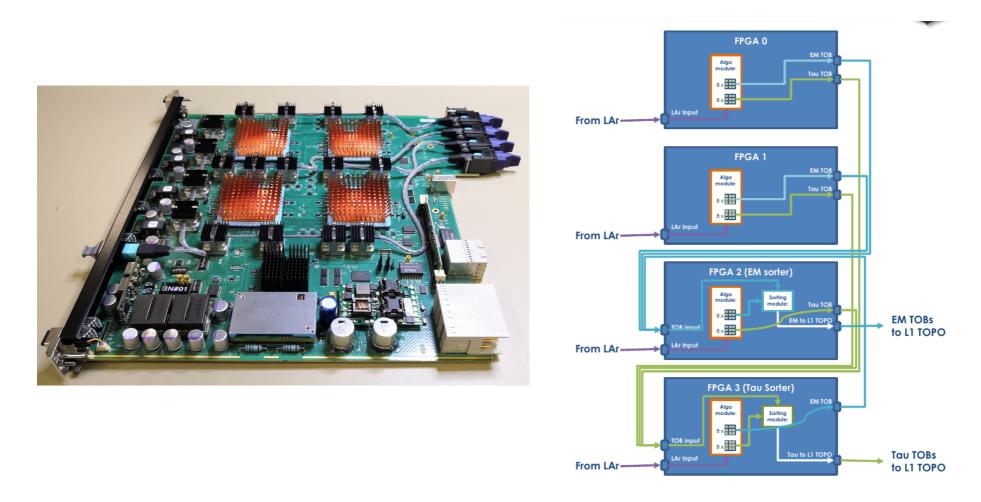




The eFex system, basic geometry



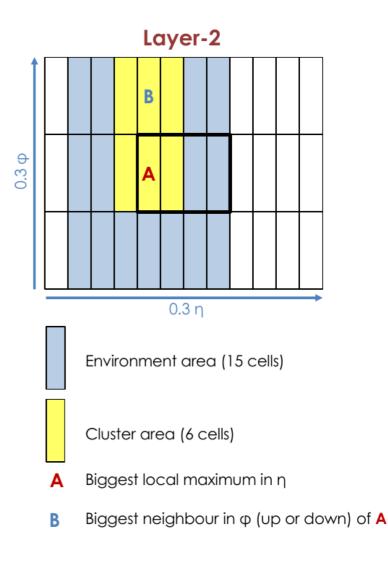
Efex board design



- Four processor FPGAs
- Two of them merge results (one em/gamma, one tau) before sending output into L1Topo

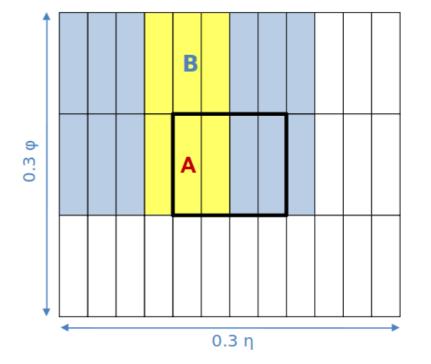
EM algorithm

- Electron algorithm:
 - Find seed (local maximum and biggest SC in TT in Layer 2) and direction of the cluster
 - Sum-up layers, calculate cluster (ToB) energy
 - Calculate isolation variables:
 - ≁ R_n
 - → Ws
 - ✤ R_{had}
 - Compare each isolation variable with three thresholds, calculate "isolation bits"
 - Re-calibrate ToB energy, send to Topo and readout
- Parameters:
 - Minimum ToB energy threshold
 - Maximum ToB energy to apply isolation
 - R_n (x3), W_s (x3), E_{had} (x3) thresholds
 - All coming from trigger menu!

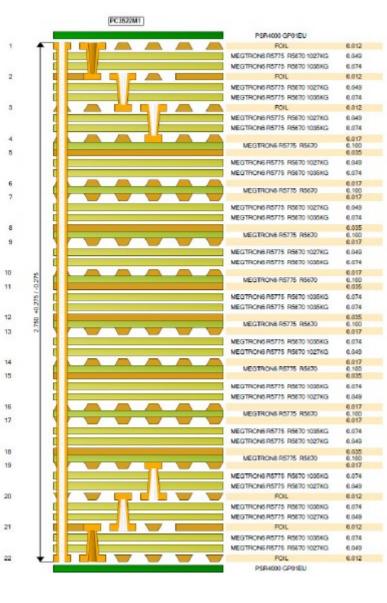


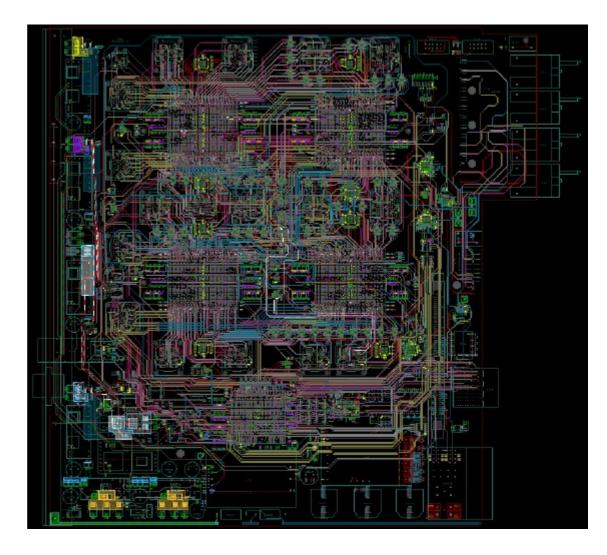
TAU algorithm

- Tau algorithm:
 - Find seed (two seed finders, biggest TT and SC in TT) and the direction of the cluster
 - Sum-up layers, calculate cluster (ToB) energy
 - Calculate isolation variables:
 - Jet Veto (like R_n but different size)
 - Frac (like E_{had} but different layers, longlived particles)
 - Compare each isolation variable with three thresholds, calculate "isolation bits"
- Parameters:
 - Minimum ToB energy threshold
 - Maximum ToB energy to apply isolation
 - JetVeto (x3), Frac(x3) thresholds
 - All coming from trigger menu!

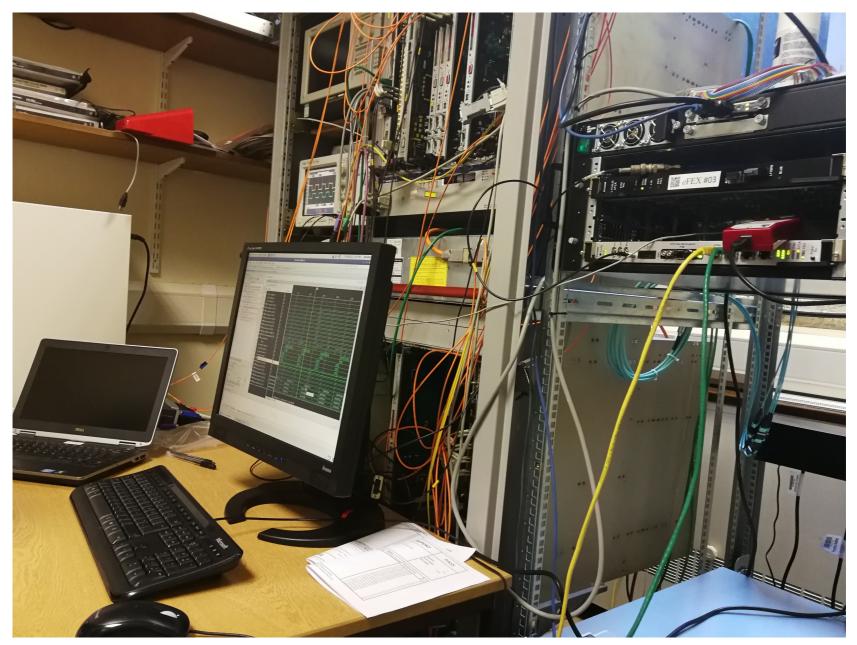


eFEX PCB design





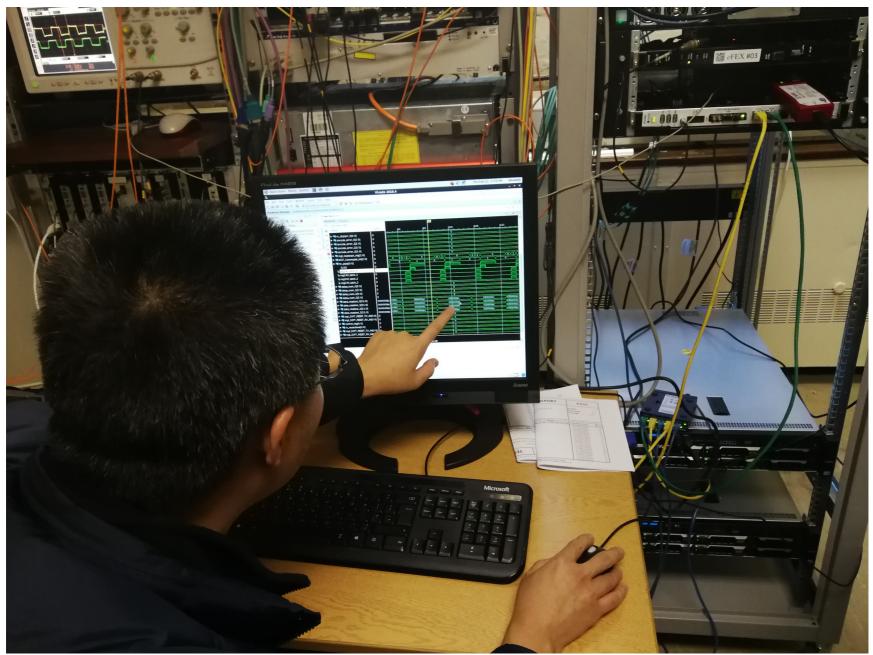
Early eFEX prototype board and firmware tests I



Early eFEX board and firmware tests II

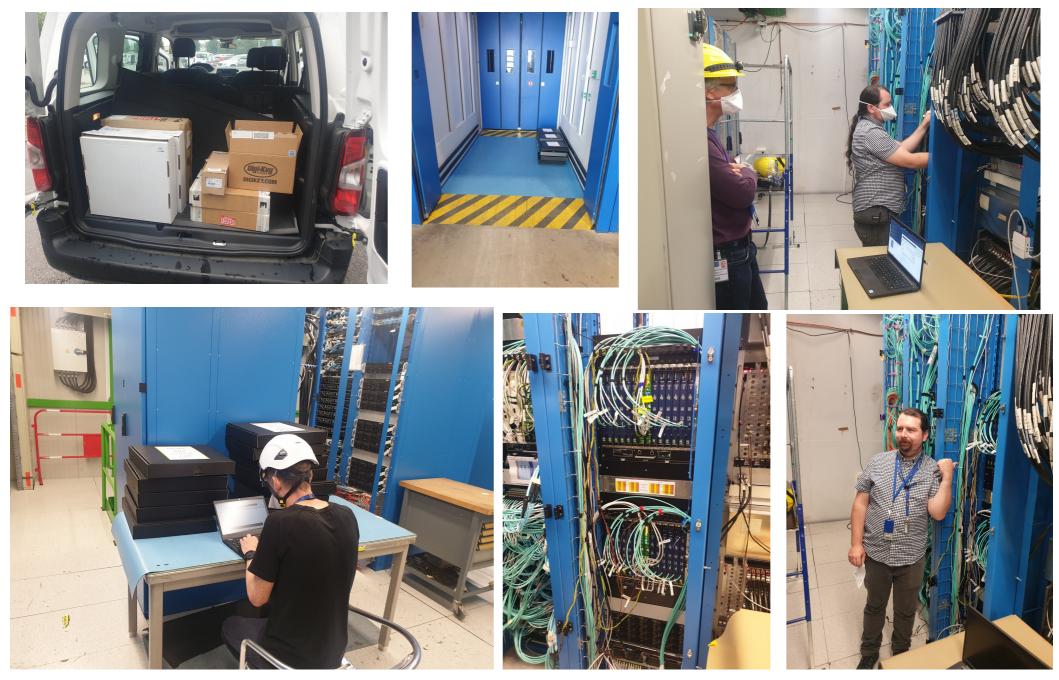


Early eFEX board and firmware tests III



eFEX -production board





Final system installation in Sep 2022

One of new processors (eFex) in numbers

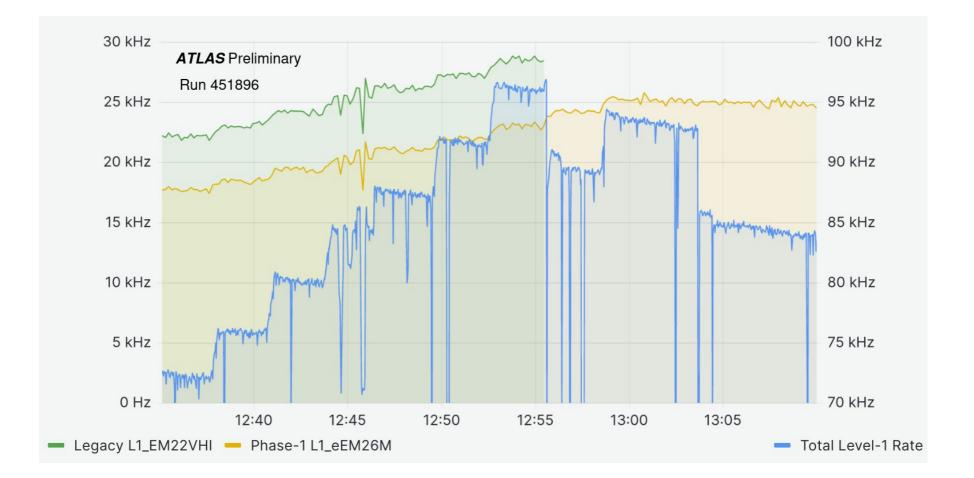
Data flow through the system (eFex):

- 24 electronic modules
- 4 programmable FPGA chips on each module
- 58 optical fibres/FPGA
- 20 useful data words/LHC tick
- 10 bits/data word
- 40 MHz LHC collision frequency (25 ns is LHC tick)
- After multiplication we get ~40000 Gb/s

Typical phone chat (mobile phone or WhatsApp): 100 kbit/s

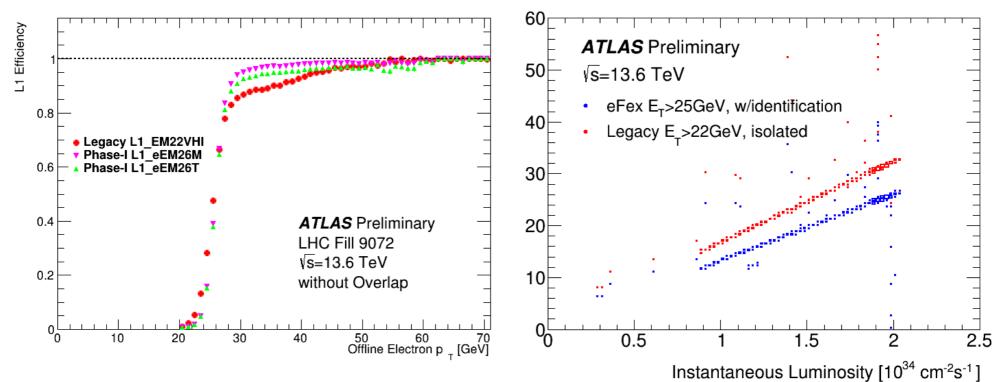
~ 400 M phone chats, all of them routed and processed by a system that is as big as average bookshelf

<u>eFEX electron trigger performance I</u>



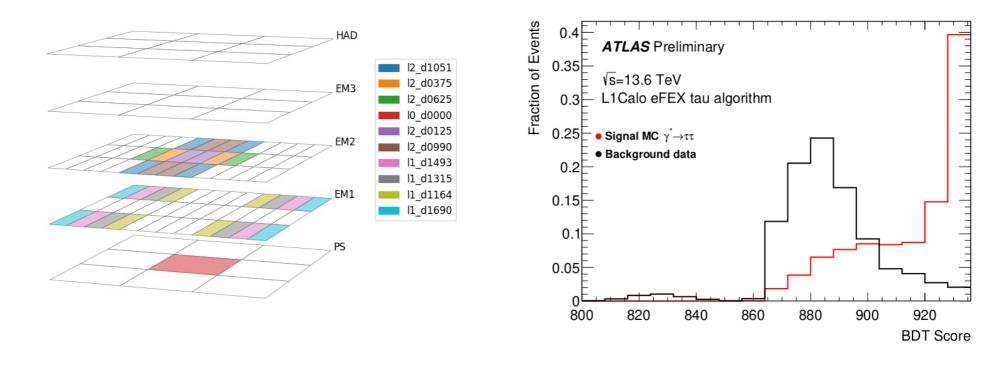
Switch over from main legacy electron trigger to Phase 1 system (more details here)

eFEX electron trigger performance II



- Comparison of legacy electron trigger with Phase I trigger more details
 - This is first, not very well tuned eFex trigger (several calibrations updated in the mean time)
 - Better (lower) trigger rate
 - Better efficiency

<u>Upgrades of eFex tau trigger</u>



- In 2024 switched from heuristic tau trigger algorithm described before to ML based algorithm
 - Find local cluster
 - Then run Boosted Decision Tree to identify isolated taus
 - After several re-tunings performs better than heuristic algorithm
 - Hope to benefit fully in 2025
 - More details here

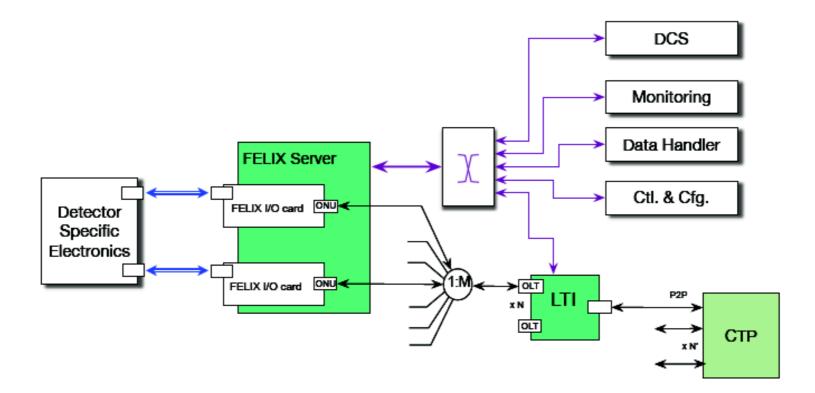
Conclusions

Conclusions

- To fully benefit from LHC capabilities, ATLAS has developed a sophisticated, multi-level trigger
- Extensive upgrades whenever possible
 - * (parts of) detectors
 - (most of) electronics
 - Combination of small adiabatic changes and revolutionary architectural modifications allow to cope with increasing luminosity and pile-up and fully exploit ATLAS physics potential

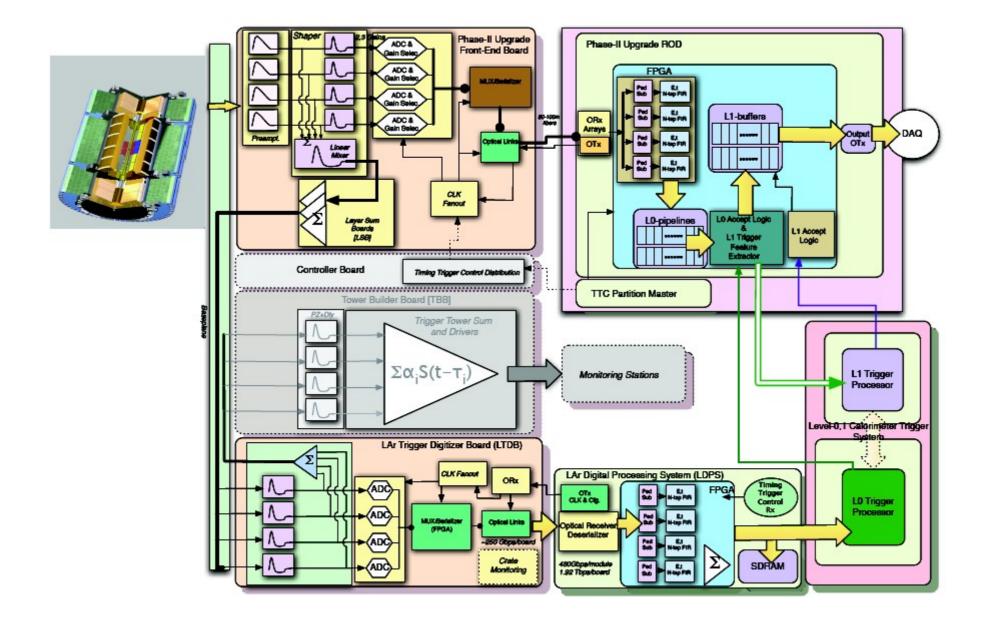
Slides that weren't good enough to make it into the talk

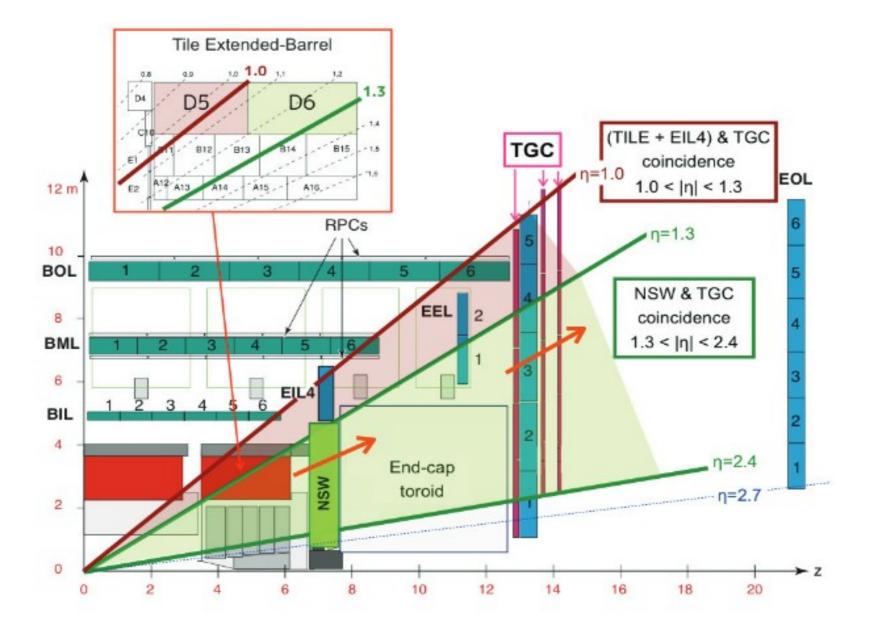
FELIX as TTC interface



- Front-End links
- —> PON or P2P links
- Multi-Gigabit network

Phase 2 LAr front-end

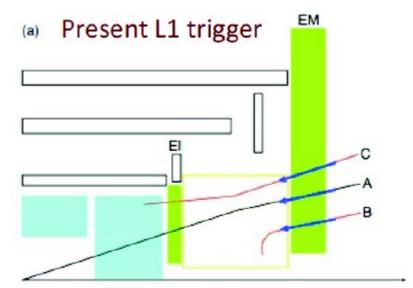


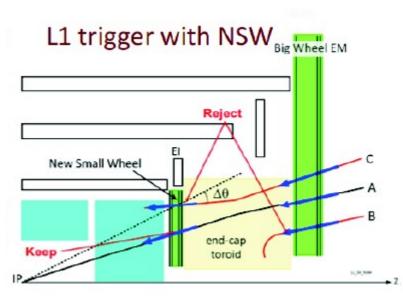


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Phase 1 upgrades of L1 trigger I

- Muon trigger rate in forward region dominated by fakes
- New muon detector in the forward area – New Small Wheel:
 - Detector technologies:
 - Micromegas
 - Small-strips Thin Gap
 Chambers (sTGC)
 - New sector logic and interface to Central Trigger

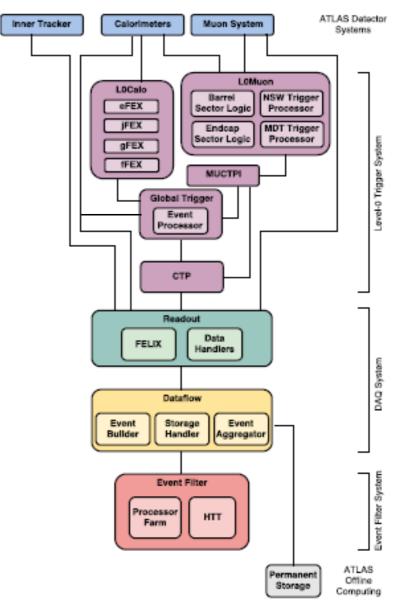




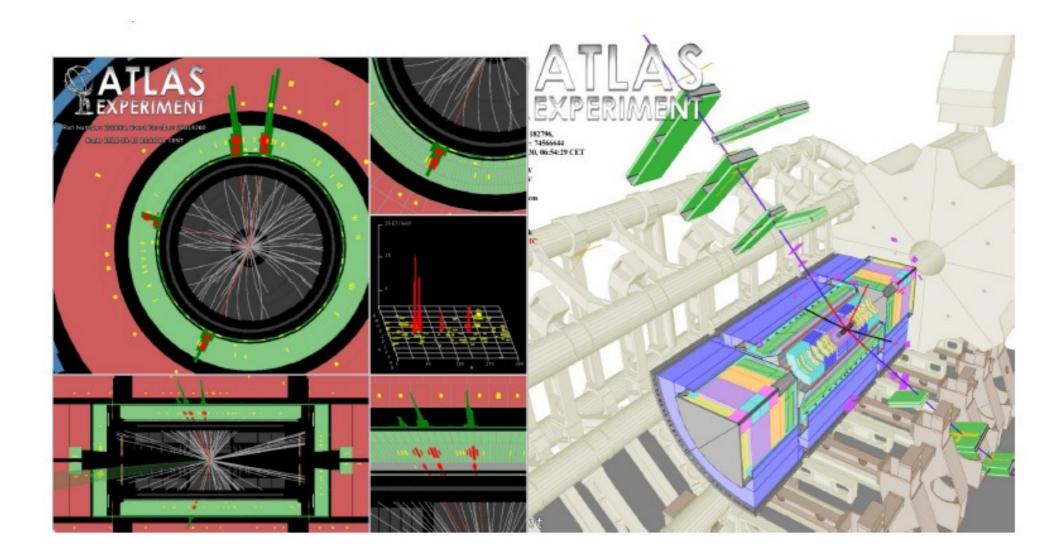
Phase 2 upgrades of ATLAS trigger

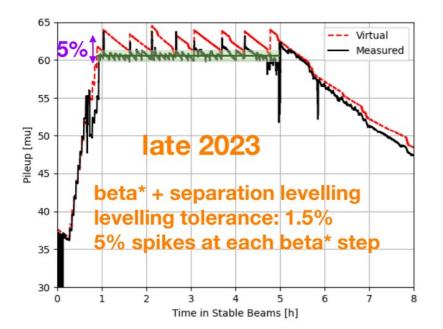
IDAQ Phase-II Upgrade Project

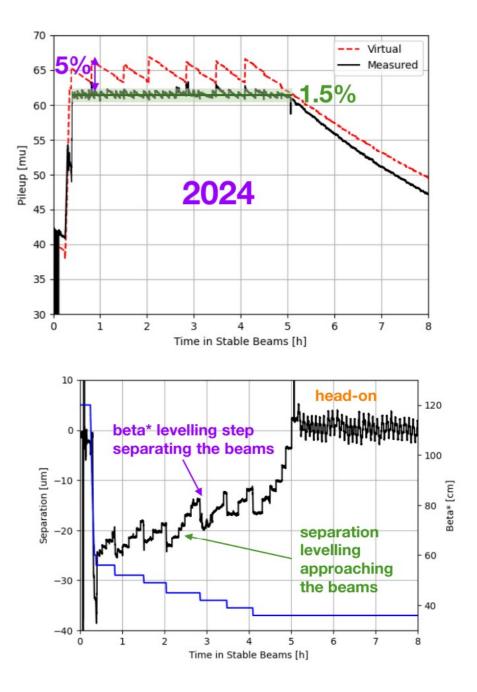
- Keep one HW and one SW level architecture
- Both levels see changes!
- Hardware level:
- Changes name (L1 to L0 :-))
- New Global trigger processor
 - Time multiplexed architecture
- (possible) new Timing Detector (High Granularity Timing Detector, HGTD)
- Muon Drift Tube (MDT) information added to trigger
- New Resistive plate chambers in the barrel to improve muon triggering
 Triggering Disco



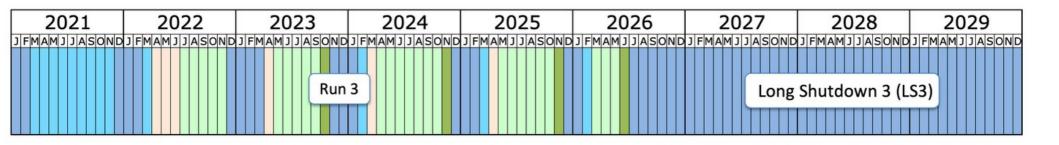
Regions of Interest (RoIs)



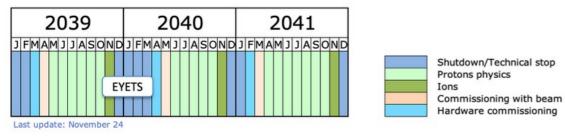


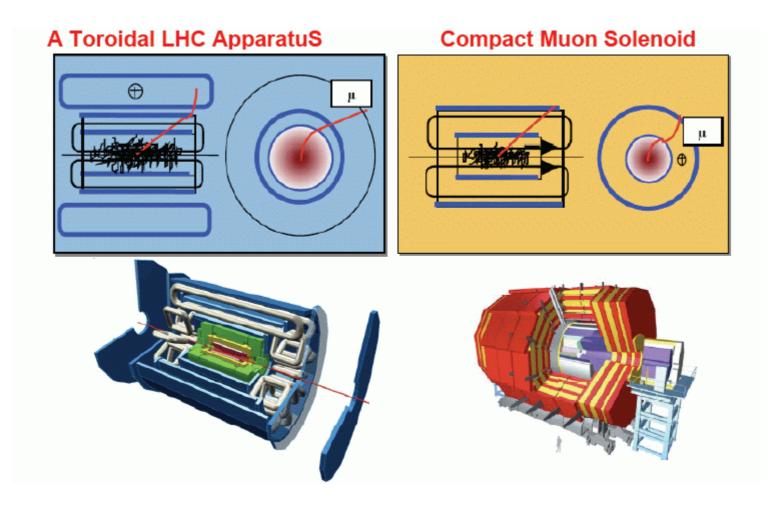


- Levelling strategy developing over time
- Recently combination of two effects
 - Separation of beams
 - β^* separation

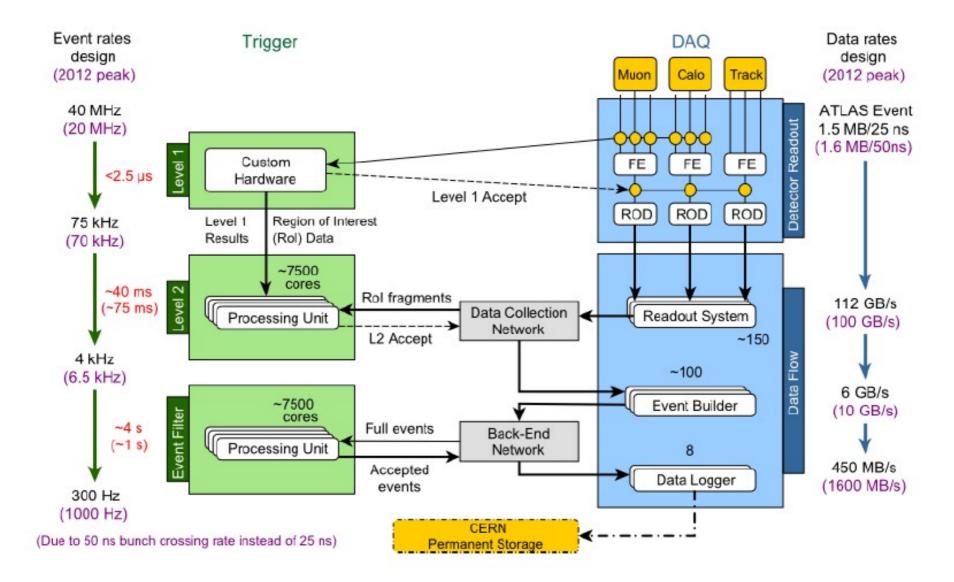


2030	2031	2032	2033	2034	2035	2036	2037	2038
JFMAMJJASOND	JFMAMJJASOND	J FMAM J J A SOND	JFMAMJJASOND	JFMAMJJASOND	JFMAMJJASOND			
	Run 4			Ľ	S4		Run 5	

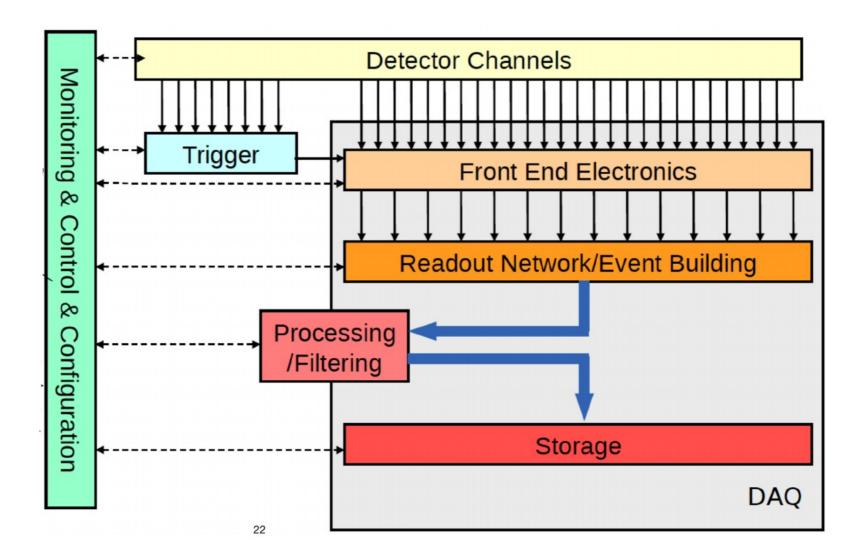




High Level Trigger during Run1

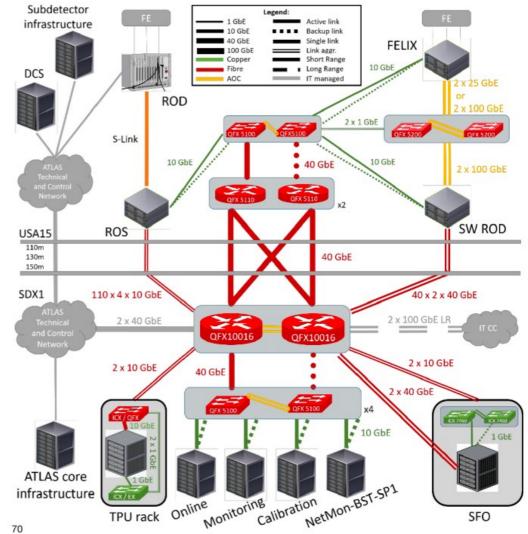


High Level trigger

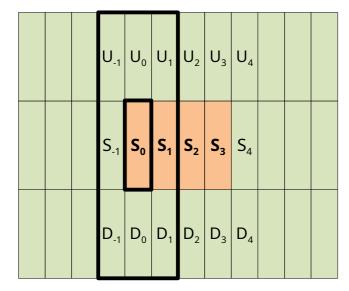


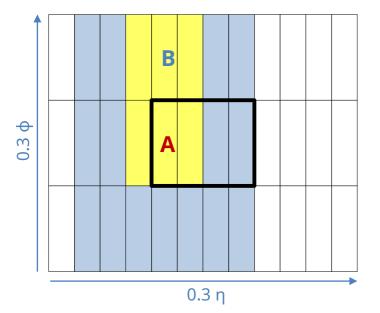
The DAQ network

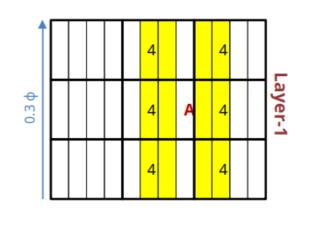
- The network system is the backbone of the ATLAS DAQ system
 - Multi-gigabit per second Ethernet infrastructure
 - Focus on high availability and performance
- Spans from USA15 to SDX1
 - Hundreds of > 150m long fibers
- Different virtual networks are provided
 - Main ones are DAQ control network for TDAQ control traffic and DAQ data network for Physics data traffic
 - Great degree of redundancy, can cope with all foreseeable single-component faults

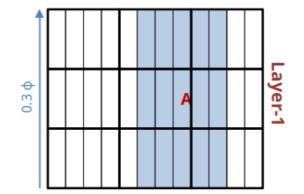


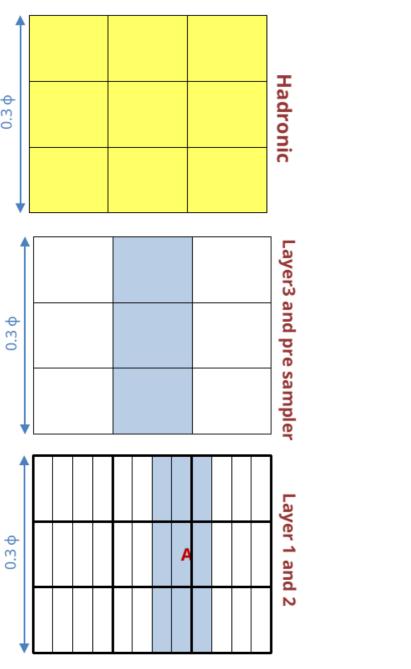
<u>eFEX electron finding algorithm</u>







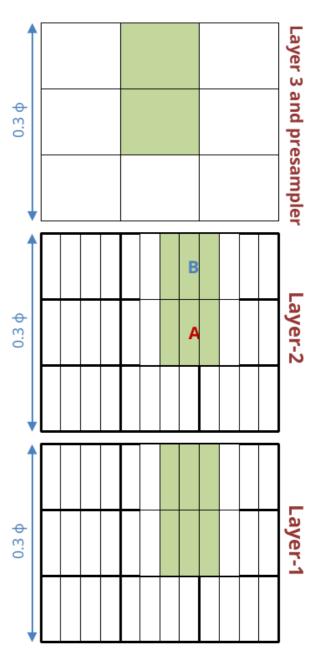




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Cluster energy