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Characterization results of MAPS digital prototypes for the ALICE ITS3

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ABSTRACT

The three innermost layers of the ALICE Inner Tracking System (ITS2) will be replaced by a truly cylindrical tracker, the ITS3, to be ready for LHC Run 4 (2029–2032). The ITS3 will be composed of three layers, each made by two self-supporting, ultra-thin (≤ 50 μm) flexible Monolithic Active Pixel silicon Sensors (MAPS) of large area (O(10 × 26 cm^2)). The final sensor will be realized using the 65 nm CMOS imaging process and stitching technology. Multiple small-scale test structures were included in the first production run (Multiple Layer Reticle 1 - MLR1) to validate the 65 nm CMOS imaging technology. First large-scale stitched MAPS were included in the second production run (Engineering Run 1 - ER1). The pixel cell performance has been qualified on the MLR1 Digital Pixel Test Structures (DPTS) in laboratory and with in-beam measurements. The large-area (1.4 × 25.9 cm^2) ER1 MOnolithic Stitched Sensor (MOSS) prototype has been used to prove the stitching principle and evaluate the detection efficiency and spatial resolution. This contribution will give an overview of the most recent results of the digital prototype tests.

1. Detector motivations and layout

A new Inner Tracking System ITS3 [1] will replace the three innermost layers of the ALICE ITS2 during LHC Long Shutdown 3 (2026–2028). The minimization of the distance between the first detection layer and the interaction point (19 mm) and the unprecedentedly low material budget of 0.09% X_0 per layer will further improve the tracking efficiency and the pointing resolution. This improvement will allow to increase the precision of measurements in the heavy-flavor sector and to bring another set of fundamental observables into reach [2], allowing for example for the measurement of B^0_s and Λ^0_b at low transverse momenta and of non-prompt D^+_s and Ξ^+_C decays in heavy-ion collisions.

The layout of the ITS3 includes two half barrels, each composed of three truly semi-cylindrical self-supporting layers. Each half-layer is made of one large-area (O(10 × 26 cm^2)) ultra-thin (≤ 50 μm) bent stitched Monolithic Active Pixel silicon Sensor (MAPS), which is held in position by an ultra-light carbon foam support structure. The detector is foreseen to be air cooled. The sensor technology for the ITS3 detector is being developed within the project.

2. ITS3 prototypes

The results of the characterization of two of the prototypes from the first two sensor productions for ITS3 are discussed in the next section: the Digital Pixel Test Structure (DPTS), aimed at the qualification of the Tower Partner Semiconductor Co. 65 nm CMOS imaging process, which was chosen for the ALICE ITS3, and the MOnolithic Stitched Sensor (MOSS), aimed at the implementation and validation of the stitched design. The DPTS is a small area (1.5 × 1.5 mm^2) chip, which includes a 32 × 32 pixel matrix with 15 μm pitch and features Time-over-threshold (ToT) measurement capabilities. The design of the DPTS is aimed to study the in-pixel front-end for the validation of the full signal processing chain. Multiple pixel design options were investigated with the first small-area prototypes. The *modified with gap* process showed the best performance [3]. Compared to the standard system formed by an n-well collection diode in a thin epitaxial layer, this modification features an additional low-dose n-type implant in between the two, with a 2.5 μm gap at the edges of the pixels, creating a planar junction deep in the sensor. MOSS is the first large-area (1.4 × 26 cm^2) sensor, which includes 10 Repeated Sensor Units (RSU), each comprising eight regions organized in two half units with pixel arrays of different pitches (18 μm and 22.5 μm). The two half-units differ in circuit density and in widths and spacing of the interconnecting metal structures.

3. Test results

3.1. Laboratory characterization results

An extensive campaign was conducted to fully characterize the DPTS chip with both laboratory and in-beam measurements. The ToT

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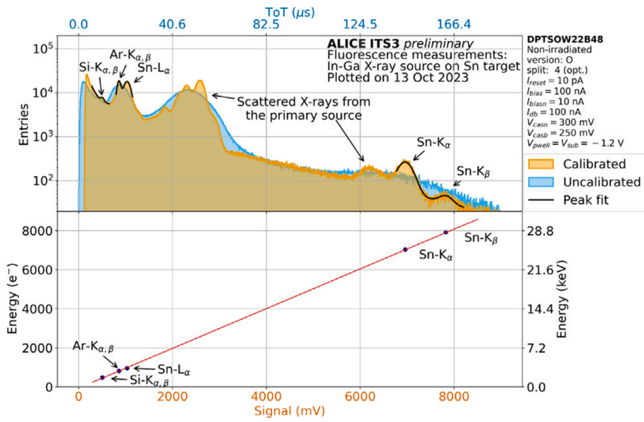

Fig. 1. Spectra of fluorescence photons from a tin target. In the calibrated spectrum (orange) the five peaks used for the energy calibration are highlighted.

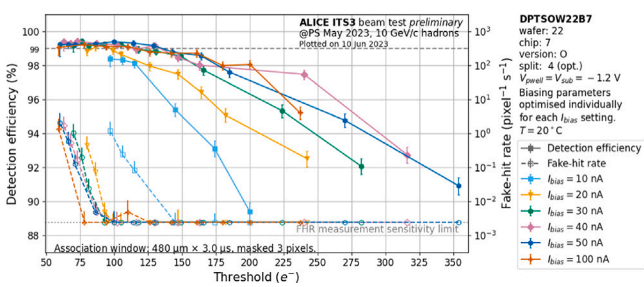

Fig. 2. Detection efficiency as a function of the applied threshold for different currents biasing the in-pixel amplifier.

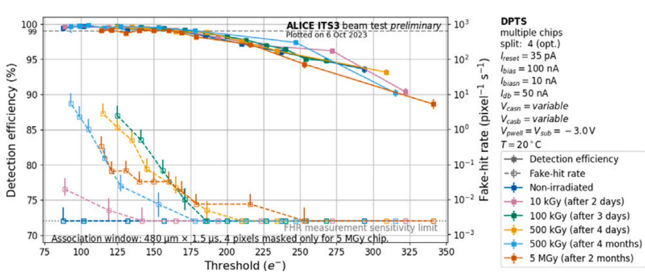

Fig. 3. Detection efficiency as a function of the applied threshold for samples which have received different ionizing doses.

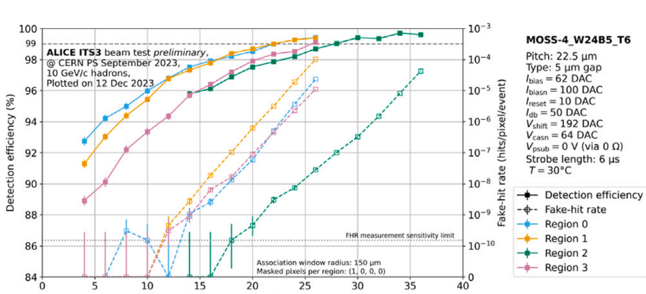

Fig. 4. Detection efficiency as a function of the applied threshold (via the parameter $V_{casb} \propto 1/thr$) for the four regions of a MOSS half-unit.

response of the DPTS was exploited to investigate the energy response of the detector when illuminated by fluorescence photons from a tin target. The characteristic Sn Kα, Kβ, Lα emission peaks, the Ar Kα peak and the Si Kα peak were identified (Fig. 1), thus allowing for the detector response energy calibration and linearity measurement up to 28.5 keV.

3.2. In-beam measurement results

The DPTS and MOSS in-beam performance was evaluated to assess the detection efficiency and the spatial resolution as a function of the applied threshold. The target performance is an efficiency higher than 99% over an operating range larger than 50 e$^-$, while keeping a fake-hit rate lower than 10 pixel^{-1}s^{-1} for the DPTS and lower than 10^{-4} pixel^{-1}event^{-1} for the MOSS.

Fig. 2 shows the DPTS detection efficiency and the fake-hit rate at different values of the main current (I_{bias}) biasing the in-pixel amplifier: the lower I_{bias} is, the lower the power consumption is. It was demonstrated that the DPTS power consumption can be lowered to 16 mV cm^{-2}, corresponding to an I_{bias} of 30 nA, still preserving the target performance.

Fig. 3 shows the DPTS detection efficiency and the fake-hit rate for samples which have received a ionizing dose up to 5 MGy. It was demonstrated that ionizing doses well beyond the ITS3 limit (10 kGy) do not affect significantly the detection efficiency.

Fig. 4 shows the MOSS detection efficiency and the fake-hit rate. The results for MOSS region 2 are in agreement with the target performance.

4. Conclusions

The R&D activities for the ITS3 sensor development are on track: the 65 nm CMOS pixel technology has been validated and the first large-area stitched sensors have been produced and are now under extensive characterization. It has been demonstrated that the small prototypes can be operated with a power consumption down to 16 mW cm^{-2} and the radiation hardness of samples irradiated up to 5 MGy was verified. Finally, a 99% detection efficiency and a fake-hit rate lower than 10^{-4} pixel^{-1}event^{-1} were measured on the large-area sensor.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

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