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The LHCb VELO detector: Design, operation and first results

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ABSTRACT

The design, operation and first results from the LHCb (Large Hadron Collider Beauty) experiment Upgrade I VELO (VErtex LOcator) are presented. The Upgrade I VELO, first installed in 2022, is a crucial new detector for providing tracking during Runs III and IV of the LHC (Large Hadron Collider). The VELO, consisting of 52 modules, closes to within 5.1 mm of the beamline. Each VELO module is made up of 4 sensors with 3, 130 nm CMOS ASICs per sensor providing precise tracking (Alves et al., 2013). The modules have a novel bi-phase CO_2 cooling substrate for reducing the radiation length of the detector while providing cooling under vacuum down to −30 °C. A new FPGA based SuperPixel clustering firmware reduces the data-rate by approximately 30% and is the first use of FPGA clustering in a collider experiment. During the VELO 2022–2024 commissioning period the SuperPixel performance has been validated, showing consistent rates between the packet rate and reconstructed clusters. The VELO material has been mapped confirming the safe re-installation of the RF (Radio Frequency) foil with respect to the VELO modules. Per-pixel equalisation across 41M channels has also been completed successfully reaching the design threshold of 1000 e^-.

1. Introduction

The LHCb (Large Hadron Collider Beauty) experiment is a dedicated machine for precision measurement of CP (Charge Parity) violation and rare processes in heavy flavour [1]. The LHC (Large Hadron Collider) Runs I and II represent 10 years of successful detector operation for the LHCb experiment. During this period the experiment collected 10 fb^{-1} of data. However, this first iteration of the detector came with several limitations. Relevant to this upgrade are the 1 MHz hardware trigger and low radiation hardness for higher luminosity operation.

As such, the LHCb experiment embarked on an ambitious upgrade program to prepare for operation at higher luminosity culminating in the Upgrade I detector [2]. Fig. 1 shows a schematic of the LHCb experiment after Upgrade I. In particular there are several new sub-detectors in the form of the SciFi (Scintillating Fibre Tracker), UT (Upstream Tracker) and VELO (VErtex LOcator); alongside a complete overhaul of the readout to accommodate a new software only trigger [3]. These upgrades will increase the sensitivity of the LHCb experiment to probe compelling problems in flavour such as Lepton Flavour Universality [4].

The VELO itself was completely redesigned for Runs III and IV, replacing the original strip detector with a hybrid-pixel design. This increased the effective readout channels from 180k to approximately 41M [5]. This new radiation hard design was installed during 2022 and is currently being commissioned for Run III data-taking at the LHCb experiment.

The VELO is isolated from the primary vacuum – where the LHC beams pass through LHCb – by a thin aluminium foil known as the RF (Radio Frequency) foil. Due to multiple failures in vacuum protection equipment the foil installed in 2022 was permanently deformed and required replacement during the 2023–2024 YETS (Year End Technical Stop). The foil was successfully replaced and surveyed with tomographic studies being shown in Section 3.2.

2. Module design

The VELO is a movable detector consisting of 52 modules (Fig. 2) positioned along the LHC beampipe under vacuum [5]. When fully closed the first active elements of the VELO are 5.1 mm from the interaction region. The 52 modules were designed with tight material budget constraints to reduce the radiation length of the detector and improve tracking performance.

Each VELO upgrade module consists of 4 hybrid silicon pixel detectors, with 3 VeloPix ASICs mounted on each sensor. The VeloPix ASICs are designed on 130 nm CMOS, have 256 × 256 pixels, and a pitch of 55 μm. Biasing for the Velopix is delivered via HV tapes that feed directly to the sensor tiles.

For readout, front-end hybrids and GBTx ASICs are mounted to the module and used to propagate data over flexible readout tapes to a vacuum feed-through board. These boards feed into OPB (Opto-and-Power Board) which are linked to the data centre – a large external computing cluster for event processing – via optical fibres.

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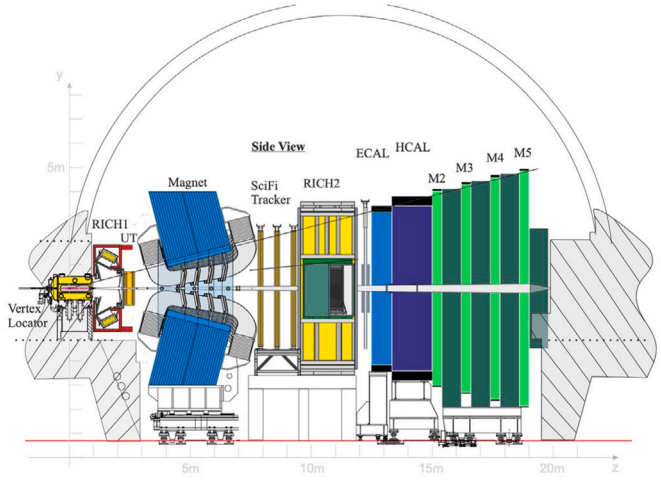

Fig. 1. Schematic of the Upgrade I LHCb experiment [2].

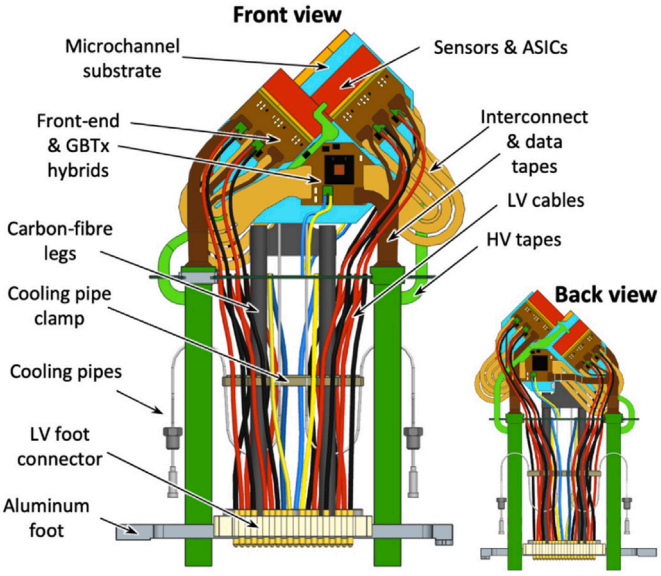

Fig. 2. Diagrammatic view of the module layout, highlighting the hybrid pixel sensors and the optical link chip (GBTx) hybrid [6].

2.1. Microchannel cooling

To remain resistant to radiation induced bulk and surface defects the VELO modules must be operated below −20 °C, and as such are nominally operated at −30 °C. There are a number of different heat sources on the modules. The 12 ASICs dissipate approximately 1.9 W each, the sensors 1 W each and the GBTx hybrids 1.6 W each giving a total power budget per module of 30 W. In order to control the temperature of the hybrid pixel modules under vacuum a novel silicon microchannel substrate was developed to deliver bi-phase CO_2 cooling [6]. For this application the silicon substrate offers a number of benefits to the cooling system. The first is that silicon has a high thermal conductivity; ≈ 150 W/(m K) at room temperature, improving to ≈ 190 W/(m K) at the nominal operational temperature of −30 °C [7]. Studies of the Thermal Figure of Merit defined as

$$TFM = \frac{\Delta T_{module-cooling}}{Power/\mathrm{cm}^2}, \quad (1)$$

demonstrated that these microchannel coolers could achieve between 1.5 and 3.5 K cm^2 W^{-1} above the 1 K cm^2 W^{-1} required by the VELO

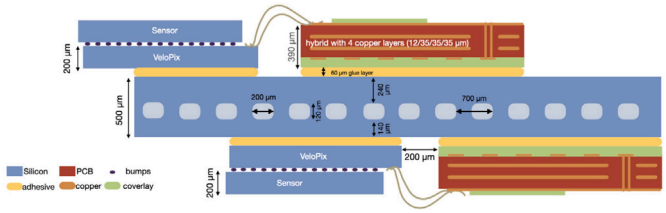

Fig. 3. Cross section of the VELO module (not to scale). The sensors overhang the cooler at the tip of the module by 5 mm in order to keep the material budget to the minimum for the first measured points on each track [6].

modules. Construction of planar silicon substrates is also a well understood technology allowing the entire substrate to be 500 µm thick, thus significantly reducing the radiation length of the detector [6].

Fig. 3 shows a general schematic of the silicon cooling substrate. The cooling substrate has 19 main cooling channels of dimension 120 × 200 µm with a pitch varying between 450 µm at the outlet, 700 µm under the tiles and 990 µm under the GBTx hybrids. All bends in the channels have a radius of 0.5 cm to ensure equivalent pressure drops across all channels. The channel size was optimised to reduce the risk of ruptures compromising the module cooling. The safety margin was carefully considered with pressure tests up to 187 bar, with nominal operation of the modules taking place at 14 bar. This cooling technology has been performing nominally since the first installation in 2022.

2.2. Superpixel firmware

Since the VeloPix ASIC front-ends are operating in a trigger-less readout at 40 MHz there can be significant latency variations between datagrams of up to 12 µs. To minimise the CPU processing penalty linked to this, firmware buffering and synchronising are vital.

To reduce bandwidth requirements of the VeloPix, pixels are aggregated into groups of 2 × 4 pixels — known as SuperPixels. This leads to a reduction in the data volume of ≈ 30% as most clusters have > 1 hits per cluster. However, even leveraging this, the rate being transmitted from the VeloPix GWT (Gigabit Wireline Transmitter) [8] – a custom transceiver – is still extremely high. As such, it is necessary to process the SuperPixels in real-time using an FPGA [9]. The platform specifically used by the LHCb is the PCIe40 [10] developed by the 'Centre de Physique des Particules de Marseille'.

For precision physics the most accurate x,y position needs to be extracted from the SuperPixels. Fig. 4 demonstrates the logic in which SuperPixels are classified, and then clustered for tracking. The first stage is classifying the SuperPixels as either isolated, surrounded by 8 empty SuperPixels, or non-isolated, having a neighbouring filled SuperPixel. Clustering for isolated clusters at this point is relatively simple with the true cluster location being identified from a look-up table of 255 possible arrangements. If the clustering is non-isolated 3 × 5 matrices of SuperPixels (clustering matrices) are used to match 3 × 3 cluster candidates. This is done by looking for patterns A or B in Fig. 4 and defining self-contained, and non-self-contained clusters, whether all the pixels are inside the candidate or they are not. For each clustering matrix all possible 'checking pixels' are run in parallel to ensure all candidates are captured in the most efficient way.

Using this clustering strategy the VELO is able to maintain readout at 40 MHz in line with the original design requirement. Early studies of the SuperPixel performance in Run III are presented in Section 3.1

3. Commissioning

Since the redesign, an extensive commissioning period has been required to ensure that the VELO reaches the requirements set out in Ref. [5]. This commissioning has demonstrated the performance of the VELO with respect to the novel clustering firmware, the noise response of the VELO, and has validated the mechanical installation of the new RF foil.

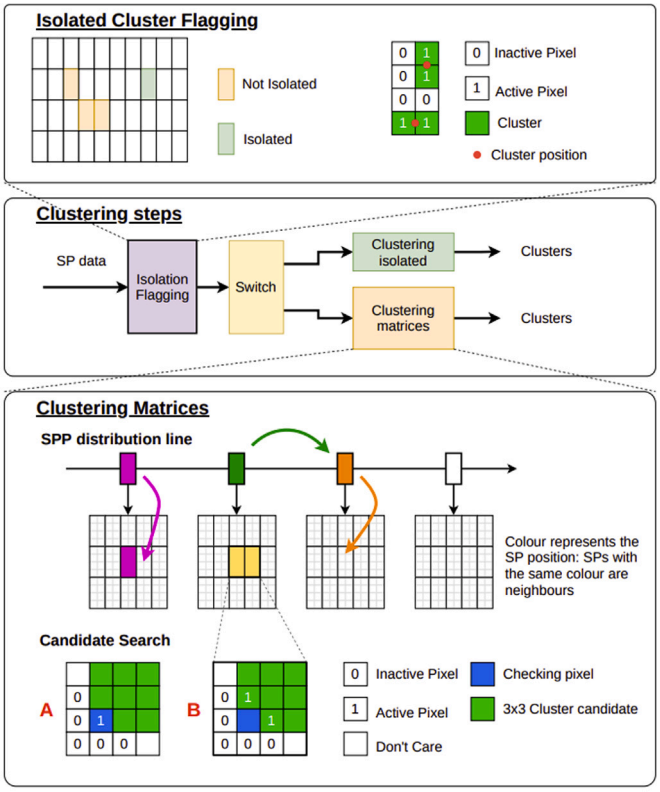

Fig. 4. Diagrams outlining cluster creation from SuperPixels. The top box shows the steps to produce clusters with the processing selection based on whether the SP is isolated or not. The bottom box shows the more complex treatment required for non-isolated SPs. A distribution line groups SP neighbours, and a candidate check is performed on each pixel to match condition A or B [9,11].

3.1. Clustering

The VELO is the first LHC detector to do clustering in firmware, so the demonstration of consistent behaviour is important for data taking. The Superpixel FPGA clustering can be compared to the raw SuperPixel packet rate (Fig. 5). Since the packets on average contain a single cluster a mismatch between the packet rate and the number of reconstructed clusters would indicate abnormal behaviour from the reconstruction algorithm or FPGA. It has been demonstrated that the FPGA clustering works consistently up to the design limit of 5.3 μ, where μ is the number of visible pp interactions per bunch crossings. There are also efforts to compare the more CPU intensive Online clustering to further validate the SuperPixel behaviour.

3.2. Tomography

To validate the position of material inside the VELO during operation, detailed tomographic studies have been completed. These studies use secondary vertices from the interaction point to map material inside the detector. Secondary vertices are reconstructed from tracks in the detector that terminate far enough from the pp collision that they are likely produced by hadronic interactions in the material. By using the PV resolution of the VELO ($\lesssim 50$ μm) it is therefore possible to map the material of both the module and the RF foil as seen in Fig. 6. During the final stages of the first closure, tomographic studies were used to validate the resolver and beam positions as seen by each module in the detector. Further to this the studies were used to validate the metrology of a new RF foil installed during the 2023–24 YETS. The foil was shown to be installed correctly with the expected tolerance between modules and the foil.

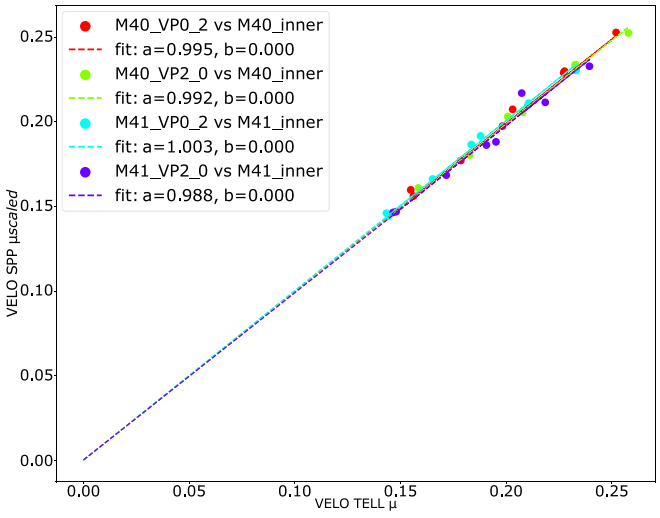

Fig. 5. Comparison of the Superpixel packet rate and clustering. The mu value quoted is relative to the detector and not aligned to the true μ of the experiment. The highest values of the VELO μ correspond to the design value of mu of 5.3.

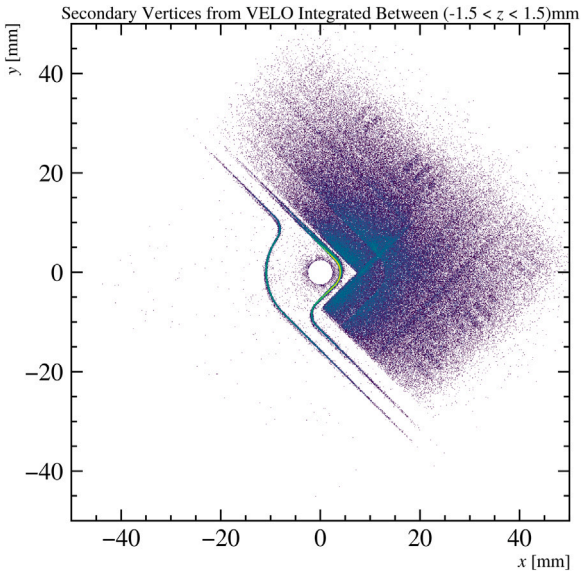

Fig. 6. Tomographic scan of a single VELO module. The VELO module itself can be seen alongside the outline of the RF foil.

3.3. Equalisation

To obtain a consistent noise response across the 41M pixel channels in addition to a global threshold value each pixel can be individually adjusted. For this purpose, the internal logic contains a 4 bit trim DAC that allows for fine adjustment of the noise thresholds. On a per pixel level threshold scans are done to identify the correct trim levels. These scans change the local threshold defined as

$$Threshold_{Local} = Threshold_{Global} + Trim, \quad (2)$$

to the largest and smallest available trim. In the case of VELO commissioning these scans where done to optimise for the design target of 1000 e^- (Fig. 7).

4. Conclusion

With the re-design of the VELO for Runs III and IV there has been considerable work to overcome challenges linked to the data rate,

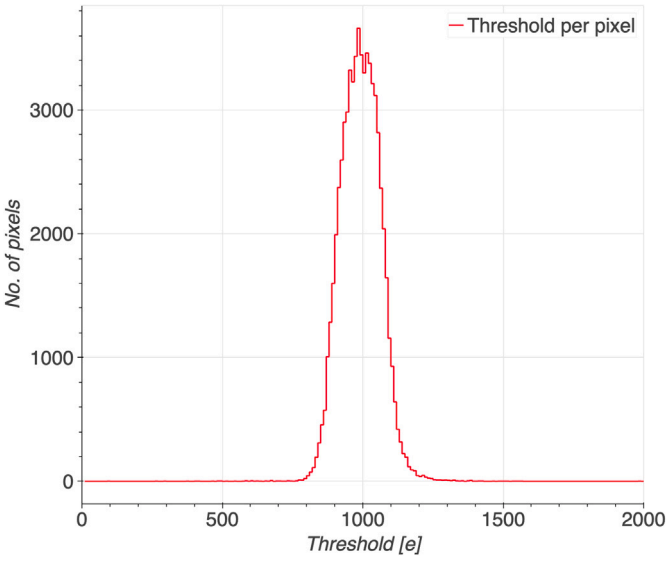

Fig. 7. Histogram of threshold per pixel. Results of the equalisation showing a successful calibration of a single ASIC to the target of 1000 e^-.

cooling and equalisation. From 2022–2024 there has been significant progress in installing, commissioning and developing the detector for high quality data taking within the LHCb experiment. It has been demonstrated that the FPGA clustering and equalisation can reach the design requirements. Future study of key performance metrics will support the physics reach of the experiment.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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