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Upgrade of the ALICE Inner Tracking System for LHC Run 4

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The ALICE experiment is preparing the ITS3, an upgrade of its Inner Tracking System for LHC Run 4. The three innermost layers will be replaced by wafer-scale, truly cylindrical, ultra-thin detector layers, made of Monolithic Active Pixel Sensors. This innovative technology will permit to reduce the material budget from 0.364%X_0 to 0.05%X_0 and to improve the tracking and vertexing capabilities. In this paper the detector concept, the R&D programme, including the already achieved demonstration of the operability of bent MAPS, results of first measurements on new developed 65 nm CMOS technology, chosen for ITS3, and the next steps, regarding first stitched wafer scale sensors, will be reported.

KEYWORDS: silicon detector, bending, cylindrical, wafer-scale, monolithic, pixel, MAPS, 65nm

1. Introduction

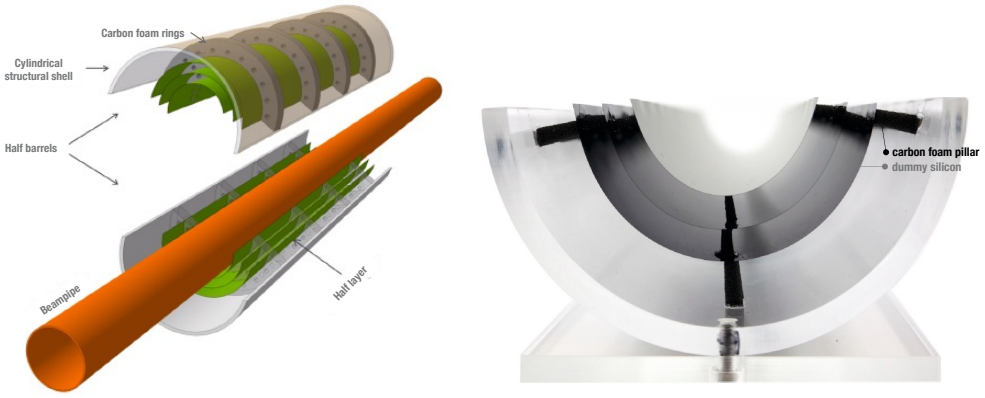
The ALICE experiment [1, 2] at CERN has been designed to study the properties of the strongly interacting, dense and hot matter created in ultra-relativistic Pb–Pb collisions and has been optimised for detection of large particles multiplicities and low momenta. It provides Particle IDentification (PID) in the range of momenta between 0.15 GeV/c to 20 GeV/c and excellent capabilities for primary and secondary vertex reconstruction. In 2021, a new Inner Tracking System, the closest detector to the Interaction Point (IP), named ITS2, has been installed in order to replace the previous detector to improve secondary vertex reconstruction and track reconstruction at low momenta. The basic building block is the ALPIDE chip [3] with a dimension of 15 mm by 30 mm, based on Monolithic Active Pixel Sensors (MAPS) technology. The ITS2 consists of a total of three inner layers (the inner barrel) and four outer silicon layers. The ITS2 inner barrel has a total of 432 ALPIDE chips, with a pixel pitch of 26.88 µm x 29.24 µm; the material budget per layer is 0.364% of a radiation length and the closest layer is at 23 mm from the IP.

The ALICE collaboration is planning a further upgrade, named ITS3, by replacing the ITS2 inner barrel with a novel vertex tracker based on truly cylindrical wafer-scale MAPS during the LHC Long Shutdown 3 (LS3), in 2026-2028 [4]. In this paper the strategy that lead to the ITS3 detector concept and the status and future R&D plans will be presented.

2. ITS3 detector concept

The concept of the ITS3 aims at reaching an unprecedented material budget and getting as close as possible to the IP. The latter will be implemented thanks to a new, thinner (500 µm vs 800 µm of the present one), beam pipe, with a smaller radius of 16 mm; the first layer of ITS3 will be at 18 mm from IP, to be compared with the actual ITS2 innermost layer at 23 mm. In order to reach this ambitious and challenging goal, the 432 sensors which constitute

the ITS2 inner barrel will be replaced with six (three on top plus three on bottom) truly cylindrical bent wafer-scale MAPS sensors. A scheme of the ITS3 design is reported in Figure 1(a).
The material budget will be discussed in section 2.1. The improvement in the performance w.r.t. ITS2 is summarized in Section 2.2.



(a) (b)

Fig. 1. (a) ITS3 design concept based on silicon-only cylindrical wafer-scale layers. (b) ITS3 mechanical mock-up of 3 half-barrel layers separated by carbon foam.

2.1 Material budget

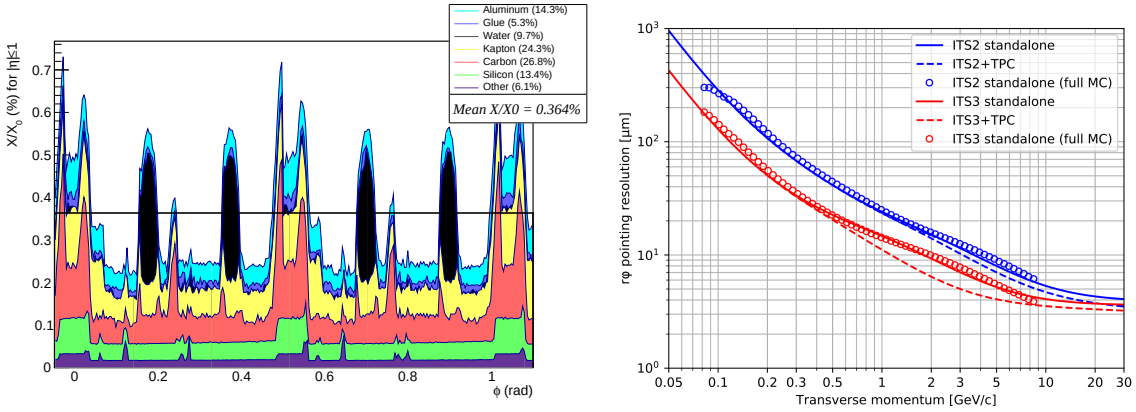
The material budget of the innermost layer of the ITS2 is reported in Figure 2(a), with an average 0.364%X_0 per layer. As can be noticed, the distribution is highly non-uniform due to overlaps and due to the several contributions from mechanical support, water cooling and circuit board (carbon fiber support and material budget for power supply and data transport). As can be noticed, only a small part, around 0.05 %X_0, is due to the silicon sensor. The basic ITS3 concept is to remove all material but the silicon itself (in addition to a support structure, more details in Sec.3.2), reducing to 1/7 the total material budget down to around 0.05%X_0. Moreover, this will lead also to a homogeneous distribution, with negligible systematic error from the material distribution itself.

2.2 Performance

Thanks to the reduced material budget and to the closer distance to the IP, ITS3 will improve both in tracking efficiency (in particular for momenta lower than 100 MeV/c) and impact parameter resolution, with respect to ITS2. This will boost the ALICE physics reach, largely based on low momenta and secondary vertex reconstruction. In Figure 2(b) [4] the projected pointing resolution of ITS3 is reported and compared with ITS2 performance. As can be seen, an improvement of a factor two is achieved in the full momentum range.

3. R**&**D status and plans

The key ingredients for ITS3, that would lead to a close to ultimate vertex detector concept are: the silicon bending, made easier also by the thinner design that will be used (from 50 µm to 20-40 µm), the cooling and support, the sensor design and the stitching. In



(a) (b)

Fig. 2. (a) ITS2 material budget per layer; several contributions are visible from mechanical support (Carbon and Glue in the legend), water cooling, circuit board (Aluminium and Kapton in the legend) and silicon sensor. (b) The pointing resolution for primary charged pions in central Pb-Pb collisions as a function of transverse momentum. The lines show the results with Fast Monte Carlo Tool; full lines for ITS only, and dashed lines for ITS+TPC (Time Projection Chamber) combined. Open circles show the results with full MC and ITS only.

this section each of these key steps will be discussed.

The mechanical support needed for ITS2 (see Section 2.1) will not be necessary anymore, since a new self-supporting arched structure will be used; furthermore, reducing the power consumption to below 20 mW/cm^2 will allow to replace the water coolant with air. Since signals and power distribution will be integrated in the sensor itself, the circuit board material will not be necessary. A summary of the ITS3 geometrical parameters is reported in Table I.

Beampipe inner/outer radius (mm)		16/16.5	
Number of sensors per layer		2	
Pixel size (μm^2)		O(20x20)	
Layer parameters	Layer 0	Layer 1	Layer2
Radial position (mm)	18	24	30
Pixel sensors dimensions (mm^2)	280 × 56.5	280 × 75.5	280 × 94

Table I. Geometrical parameters of ITS3.

3.1 Silicon flexibility and bending

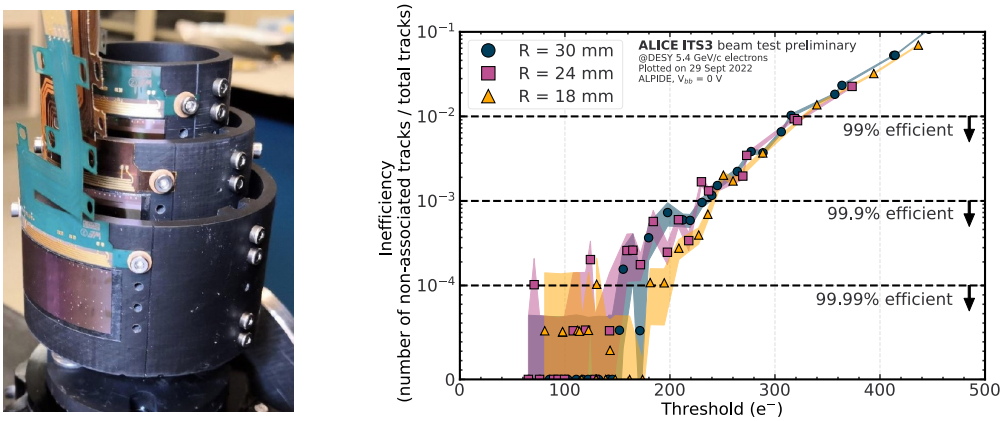
The silicon, below a certain thickness, and specifically already at 50 μm, is flexible enough to be bent to the ITS3 target radii without damage. The ITS3 will exploit this natural characteristic and enhance it, realizing truly cylindrical layers. In order to prove the feasibility of bending chip, it has been necessary to prove both the bending concept of large silicon dummy layer and also of true silicon detectors at the three ITS3 layers radii: 18, 24 and 30 mm. For the latter, the ALPIDEs chips (1.5 cm × 3 cm) have been used and more recently also MLR1 chips (see Sec.3.3) have been bent successfully to a radius of 18 mm. The performance of bent ALPIDEs have been also studied to validate this step in the R&D.

3.1.1 Bending of wafer scale silicon dummies

For the first mockup, wafer-scale, 50 µm dummy silicons have been bent using a custom method. A Mylar foil, in tension, is attached to a cylindrical mandrel and holds the dummy wafer; the cylinder is then rotated to realize the final bent sensor (more details can be found in [7, 8]). Already two full mockups have been successfully realized with this method; a picture of the first one, with the three half-layers visible, is shown in Figure 1(b). In the second mockup the carbon foam pillars have been replaced with rings, in order to realize a more uniform cylindrical shape.

3.1.2 Bending of ALPIDEs

Since 2020 ALPIDEs chips have been bent routinely in various ways: bending before or after bonding, different jigs, bending in both directions (more details in [7, 8]). A very first proof of concept to demonstrate the basic functionality of the chip can be found in [5].



(a) (b)

Fig. 3. (a) µITS3: 6 ALPIDE chips, bent to the target radii of ITS3. (b) Performance of µITS3 in terms of inefficiency versus the threshold applied to the chip, for the 3 different radii.

A smaller scale mock-up of the ITS3, called µITS3, has been realised using ALPIDE chips; in Figure 3(a) a picture of the six ALPIDE chips, bent to the target radii of ITS3 is shown. Its performance has been extensively studied in a beam test setup at CERN and DESY. In Figure 3(b) the inefficiency as a function of the threshold applied to the sensors bent at different radii measured at DESY (5.4 GeV/c electron beam), is reported. It can be noticed that independently from the radius an efficiency higher than 99% is obtained for a threshold lower than 300 electrons. Moreover, no non-uniformity among different bent radii has been observed.

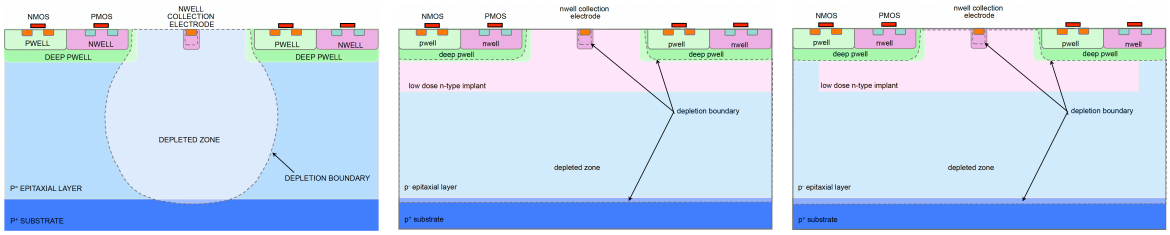
3.2 Cooling and support

In order to keep each half-bent layer in place in a self-supporting arched structure the layers will be held and separated by a set of ring spacers made out of carbon foam (see Fig.1(a)). This low density material is rigid, highly porous and has excellent thermal conductivity properties. In order to perform all the tests to find the optimal material, maintaining the low material budget, measurements in a wind tunnel setup were performed. Finally, a carbon foam with a density $\rho = 0.06$ g/cm^3 and a thermal conductivity of K = 0.033 W/m K has been chosen.

This material will allow air to flow between the layers to cool the detector. In particular, for the final detector, the temperature will be kept at 20°C. The carbon foam rings, in thermal contact with the sensors, will also act as radiators reducing the thermal gradient along the layer. Several thermal and stability tests are still ongoing, to further study the temperature gradient along the sensor and the vibrations induced by air flow (that should be negligible with respect to spatial resolution).

3.3 Sensor design

For the design of the sensor for ITS3, it was decided to move from the 180 nm process of ALPIDE to the new 65 nm CIS process of Tower Partners Semiconductor Co.(TPSCo) [6]. This technology provides 300 mm wafers which will allow the fabrication of sensors of 280 mm length. The first submission, the Multi-Layer Reticle 1 (MLR1), containing test



(a) (b) (c)

Fig. 4. Different sensor designs: (a) standard, (b) modified with blanket and (c) modified with gap.

structures for process exploration has been received in summer 2021. The submission was produced in four process splits in order to optimise the sensor for ionising particle detection, gradually modifying the doping levels of various implants. The submission also contained three different pixel sensor designs:

- a standard type, where the high resistivity epitaxial layer is typically not fully depleted 4(a)
- a modified with a blanket, a deep low dose n-type implant over the full pixel area to obtain depletion of the epitaxial layer over the full pixel area 4(b)
- a modified with gap, with the same implant but with a gap in the implant over the pixel boundary to enhance the lateral field and accelerate the signal charge towards the collection electrode 4(c).

In Figure 4 the schematic structure of the various sensor variants is shown. An intensive characterisation campaign has been performed both in laboratory, also with Fe-55 source, and with a beam test setup. In this paper, the results of the two main test structures will be presented: the Analogue Pixel Test Structure (APTS) and Digital Pixel Test Structure (DPTS). The main characteristics of the two chips are reported in Table II. The aim of the MLR1 submission was to verify the technology from the point of view of charge collection efficiency, detection efficiency and radiation hardness.

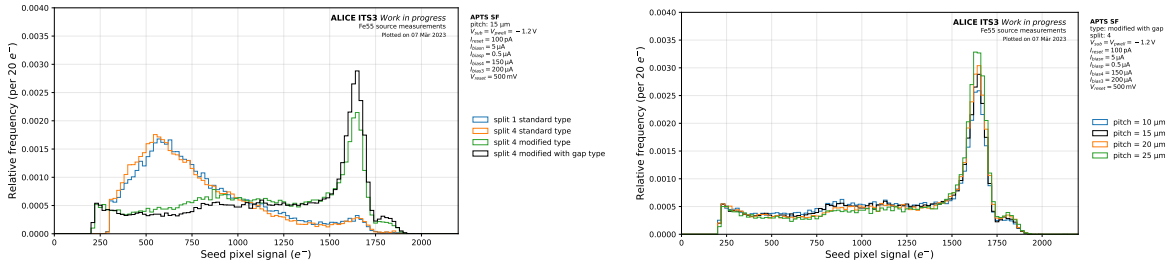
3.3.1 Charge collection efficiency

In order to validate the sensors from the point of view of charge collection efficiency, the sensor has been studied in a radioactive source setup with Fe-55. Two typical energy lines

	APTS	DPTS
die length	1.5 mm	1.5 mm
matrix	6x6 pixels	32x32 pixels
pitch	10, 15, 20, 25 µm	15 µm
active length	60, 90, 120, 150 µm	480 µm
readout	direct analogue of central 4x4 pixels	async. digital with ToT
process	standard, modified, modified with gap	modified with gap
split	1,2,3,4	1,2,3,4

Table II. Main characteristics of APTS and DPTS silicon sensors.

are expected: at 5.9 keV and at 6.5 keV [9]. Considering an average energy of 3.6 eV to create an e-h pair, the former, the Mn-K$_\alpha$ creates an average of 1640 e-h pairs while the latter, the Mn-K$_\beta$, an average of 1800.



(a) (b)

Fig. 5. APTS Fe-55 spectra of seed pixel[a] for different sensor types and a pitch of 15 µm (a) and for different pitches but for sensor modified with gap (b).

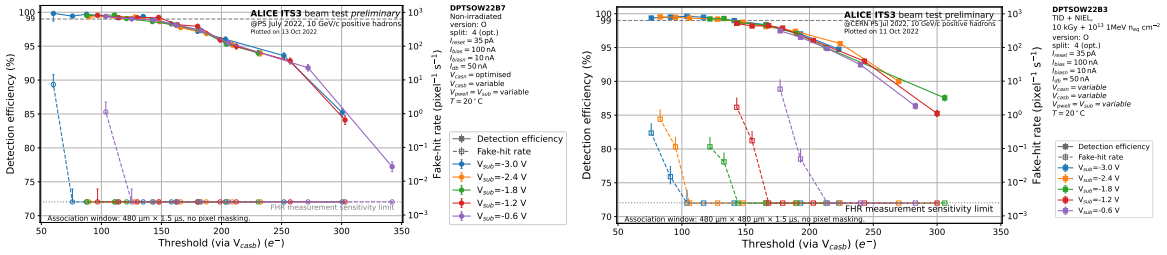
[a]The seed pixel is the pixel with the largest collected charge in a cluster (a set of adjacent pixels which collected an amount of charge higher than a certain threshold)

In Figure 5 the Fe-55 spectra taken with APTS for different sensor types and same pitch of 15 µm and for different pitches but for sensor modified with gap, are reported. In particular in Fig. 5(b) on the right, two peaks can be well distinguished, related to the K$_\alpha$ (calibration peak) and K$_\beta$. Looking at Fig. 5(a), a similar trend is also observed for the modified process, with the calibration peak slightly more pronounced for the modified type, but dominant in both the distributions. Instead the standard types show a different trend. Here the dominant peak is the one around 600 electrons, much more pronounced than the calibration peak. That dominant peak here corresponds to what is usually named charge sharing peak, i.e. when the signal is shared by multiple pixels.

The process modified with gap shows a better charge collection indicating a more efficient charge collection even when compared with the other variants.
In the modified with gap version, for all the pitches, the calibration peak is by far the dominant contribution to the distribution, much more pronounced than the sharing peak. This is in line with high charge collection efficiency. In addition, this would lead to a potentially better S/N also at higher thresholds. Moreover it can be noticed that, comparing different pitches, a similar result is observed; this would have the benefit of choosing the final pitch for the final sensor independently of the charge collection.

3.3.2 Detection efficiency and radiation hardness

To validate the sensors also from efficiency point of view the chip has been studied in several beam test setups and facilities (CERN at Geneva, DESY at Hamburg). The results here reported are obtained from the beam test of CERN PS 2022 with a positive hadron beam of 10 GeV/c. The telescope was realized using ALPIDE chips as reference planes to reconstruct the tracks and two DPTS were installed: one as trigger and the other as Detector Under Test (DUT). The DUT temperature was kept constant at 20°C.



(a) (b)

Fig. 6. DPTS detection efficiency (filled symbols) and fake-hit rate[a] (open symbols) as a function of threshold at different applied reverse biases for a not-irradiated chip (a) and a chip irradiated at 10 kGy and 10^{13} 1 MeV n_{eq} cm^{-2} (b) measured at CERN-PS with 10 GeV/c positive hadrons.

[a]The fake-hit rate is defined as the number of hits per pixel and second in the absence of external triggers. It is measured in dedicated run in a laboratory setup.

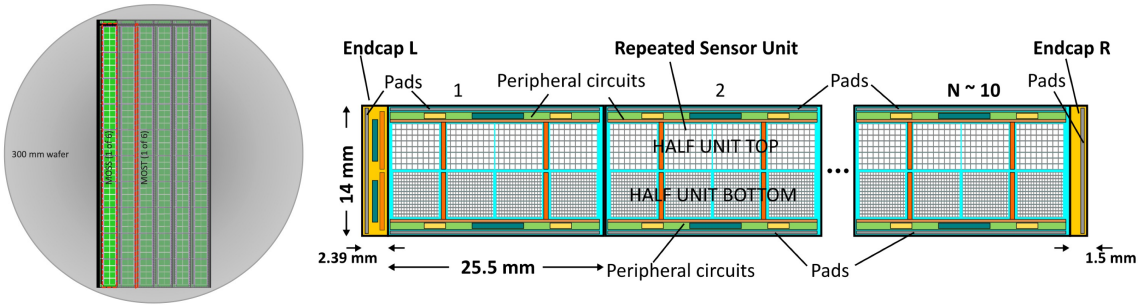
In Figure 6(a) the detection efficiency and Fake-Hit Rate (FHR) are reported as a function of threshold in number of electrons [10]. Several reverse biases applied to the sensor are also compared. As expected, the efficiency decreases as a function of the threshold while the opposite trend is observed for FHR. The optimal threshold operational value is a trade off between the maximization of efficiency and reduction of FHR. It can be noticed that for all the bias voltages reported, an excellent detection efficiency, higher than 99%, at acceptable fake hit rates and over large threshold range has been observed.

Moreover in Figure 6(b) the detection efficiency and FHR are reporoverted again as a function of the threshold in electrons for several reverse biases applied for a DPTS irradiated at 10 kGy and 10^{13} 1 MeV n_{eq} cm^{-2} [10], which is the estimated total dose during the operational life of ITS3. It can be noticed that no deviation is observed for the efficiency at all biases. The FHR indeed increases, as expected, but yet a large operation threshold margin can be chosen and the chip is perfectly operational.

3.4 Stitching of silicon detectors

The last crucial step to be validated is the stitching applied to the design of large and complex silicon detectors. Stitching will indeed be fundamental in order to produce a single large wafer-scale sensor, with the power distribution managed internally, confining the interconnections to the edges, outside the ITS3 acceptance. Stitching will be needed since the largest field of view that is used in the photolithographic steps in CMOS manufacturing defines the reticle size, and is only few centimeters (~ ALPIDE dimensions). With stitching the fabrication of a sensor that is larger than the field of view of the lithographic equipment is possible. The reticle which fits into the field of view is placed on the wafer with very high precision, achieving a tiny but well defined overlap and therefore avoiding dead area. A

wafer-scale sensor can be then realized.



(a) (b)

Fig. 7. Stitched prototype scheme layout (a) and MOSS architecture layout (b).

To qualify the stitching yield of the technology a wafer-scale pixel chip with a reduced read-out architecture is being designed: the MOnolithic Stitched Sensor (MOSS) prototype, with a dimension of 1.4 cm x 26 cm.

In Figure 7(a) the principle of the repetitive structures for the MOSS is illustrated; taking the red rectangular on the left (1 MOSS chip) from top to bottom 10 pixel matrices (reticle sizes) form a pixel sensor and are interconnected by means of stitching. The MOSS will be fundamental in order to understand the stitching rules to make a complex particle detector like the one needed for ITS3.

In Figure 7(b) a more detailed scheme of the MOSS stitched structure is reported. Each reticle comprises the pixel matrix with two different pixel pitches of 18 µm and 22.5 µm, reflecting the more or less aggressive design, in terms also of power consumption. The End cap L(Left) and R(Right) structures will distribute and receive data signals. Nevertheless, in order to allow connection to the reticle also in case of low yield, it will be possible to distribute power and signal also from top and bottom. The MOSS chip will then be tested both using the end cap and the side connections. The first prototype is expected to be delivered and tested middle 2023. The validation of the MOSS stitching structure will give important feedback on the stitching techniques, will allow the study of interconnect power and signal distribution on wafer scale design, the study of power, leakage, spread, noise and speed, and defines yield and design rules for manufacturing. This will be an important step for ITS3 project representing the last fundamental milestone.

4. Conclusions

ALICE foresees an upgrade of its Inner Tracking System during LHC-LS3. The concept is to replace the actual three innermost layers with truly cylindrical wafer-scale bent MAPS sensors to realise a close to ultimate vertex detector, named ITS3.

The R&D has already achieved fundamental steps. The silicon flexibility and bending also for wafer-scale dummy layers and bent MAPS have been proven. Two full mock-ups of the final ITS3 have been realized and the performances of bent MAPS at the three different radii have been studied and have been found to be uniform.

The cooling and support of the 6 half-layers are still under test, but several solutions have been found and proven.

The sensor design has also been validated, thanks to the first TPSCo 65 nm submission

(MLR1) received in 2021. An improved charge collection efficiency with the new design has been observed and a detection efficiency higher than 99% has been reached also at the level of radiation required by the ITS3 (10 kGy and 10^{13} 1 MeV n_{eq} cm^{-2}).

The recently designed prototype, MOSS, will be received in mid-2023 and the validation of its yield, uniformity and performances will represent the last important ITS3 milestone.

References

[1] ALICE collaboration, JINST 3, S08002 (2008), https://doi.org/10.1088/1748-0221/3/08/S08002
[2] ALICE collaboration, arXiv:2211.04384 (2022), https://doi.org/10.48550/arXiv.2211.04384
[3] ALICE collaboration, NIMA 845, 583 (2017), https://doi.org/10.1016/j.nima.2016.05.016
[4] ALICE collaboration, CERN Document Server, (2019), http://dx.doi.org/10.17181/CERN-LHCC-2019-018
[5] ALICE ITS project, NIMA 1028, 166280 (2022), https://doi.org/10.1016/j.nima.2021.166280
[6] Tower Partners Semiconductor Co., http://www.towersemi.com/
[7] M. Buckland on behalf of the ALICE collaboration, NIMA proceeding 1039, 166875 (2022), https://doi.org/10.1016/j.nima.2022.166875
[8] Arianna G. Torres Ramos on behalf of the ALICE collaboration, EPJ web of conferences 270, 00021 (2022) https://doi.org/10.1051/epjconf/202227000021
[9] Be' et al. Table of Radionuclides (Vol. 3 A = 3 to 244), Monographie BIPM-5(2006)
[10] G. Aglieri Rinella et al, in submission to NIMA, (2022), https://arxiv.org/abs/2212.08621