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The Compact Muon Solenoid Experiment

CMS Performance Note

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Discharge Studies in a CMS ME0 GEM Detector

CMS Collaboration

Abstract

The LHC is undergoing an upgrade to increase the instantaneous luminosity by half an order of magnitude; as a result, several detector systems are undergoing upgrades to operate at this higher luminosity. One such upgrade is the introduction of the ME0 GEM detectors in the endcap muon system of the CMS detector, which will extend pseudorapidity acceptance for muons to $\eta = 2.8$. New front-end electronics are being designed and tested on the ME0 detector. One such test is placing an alpha source under a hole in the drift board of the chamber to induce discharges in the detector. This is done with the electronics attached and it is found that the VFATs reset and become unconfigured during these discharges. It is unclear how the discharge resets the VFATs since the discharge creates a large electromagnetic pulse and any voltage probes nearby will act as an antenna. They will pick up a signal from this pulse, making their reading unreliable. To better understand the cause of VFAT resets, attempts have been made to simulate the conditions of a discharge. A clamping circuit is used to inject pulses into the power rails of the VFATs. It is found that a 7V pulse is reduced to a 100mV ripple. Gas Discharge Tubes are also used to manually inject a large amount of charge into the VFAT channels. The readout channels of the VFATs are damaged as a result, but the VFAT does not reset. Injecting charge directly into the GND of the VFAT forces the VFAT to reset and creates similar LV ripples as seen with alpha discharges. Additionally, it has been found that the VFAT reset is tied to the frequency of the incoming signal.

Discharge Studies in a CMS ME0 GEM Detector

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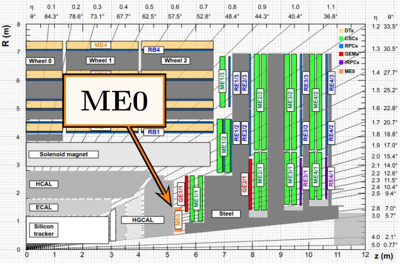
CMS Collaboration

- The Compact Muon Solenoid (CMS) experiment is being upgraded as part of the High Luminosity Upgrade
- Three new Gas Electron Multiplier (GEM) detectors are being added to the Muon spectrometer, one of which is ME0
- It will sit in the very forward region ($2.0 < |\eta| < 2.8$)
- ME0 is a stack of six GEM chambers, each chamber has three GEM foils



Quadrant of CMS showing the placement of ME0 [1].

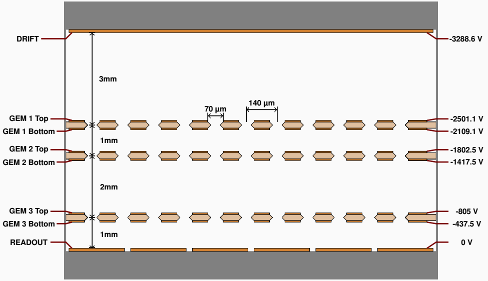
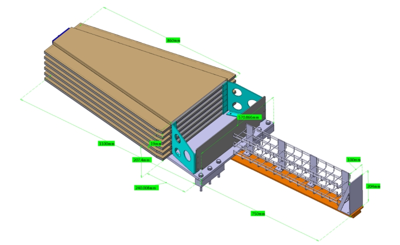
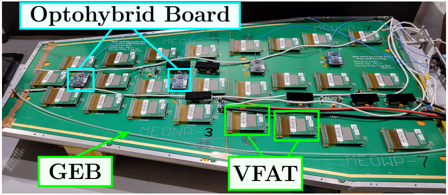


Diagram showing the GEM foils in an ME0 chamber.


Layout of ME0 stack showing six chambers [1].

- Electronics Integration is still ongoing for the ME0 Chamber
- One integration test stand is at the Florida Institute of Technology (FIT)
- Observed that the Very Forwards ATLAS and TOTEM (VFAT) front-end readout chips reset during a chamber discharge
- Discharges are expected during normal operation and reset VFATs means lost data while they are down
- Thus began investigations to prevent these VFAT resets

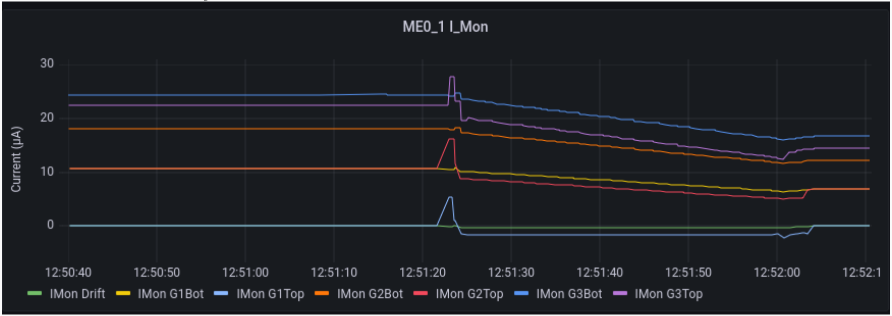


Example of the ME0 GEM Electronics Board (GEB) fully instrumented with front-end electronics. The GEB is split into a Narrow GEB (left side of the detector), and a Wide GEB (right side). A group of six VFATs are connected to an Optohybrid Board, which then connects to the backend.

OH	GBTs 0-8	VFATs 0-3	VFATs 4-7	VFATs 8-11	VFATs 12-15	VFATs 16-19	VFATs 20-23
0	0: READY	0: GOOD (RUN)	4: LINK BAD	8: GOOD (RUN)	12: GOOD (SLEEP)	16: GOOD (RUN)	20: GOOD (SLEEP)
	1: READY	1: GOOD (RUN)	5: LINK BAD	9: GOOD (RUN)	13: LINK BAD	17: GOOD (RUN)	21: LINK BAD
	2: READY	2: GOOD (RUN)	6: LINK BAD	10: GOOD (RUN)	14: LINK BAD	18: GOOD (RUN)	22: LINK BAD
	3: READY	3: GOOD (RUN)	7: LINK BAD	11: LINK BAD	15: LINK BAD	19: GOOD (RUN)	23: LINK BAD
	4: READY						
	5: READY						
	6: NOT_READY						
	7: NOT_READY						

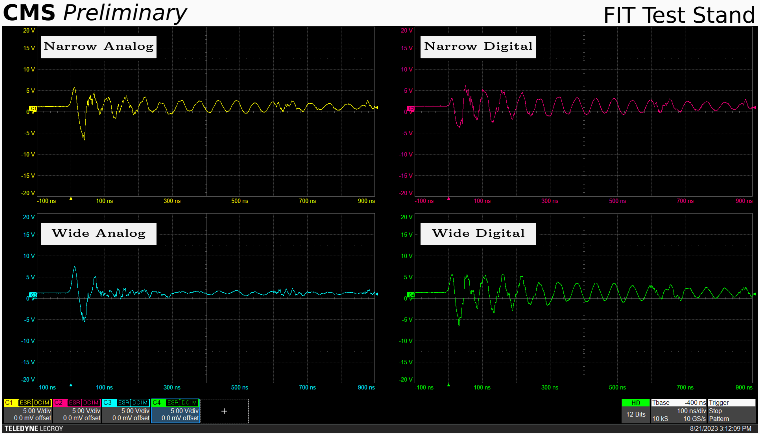
Example of the status of the front-end electronics after a Discharge. Some VFATs are unaffected (GOOD (RUN)), some get unconfigured (GOOD (SLEEP)), and some get reset (LINK BAD). For this example, the GigaBit Transfer (GBT) ASICs reset as well (NOT READY).

CMS *Preliminary* FIT Test Stand



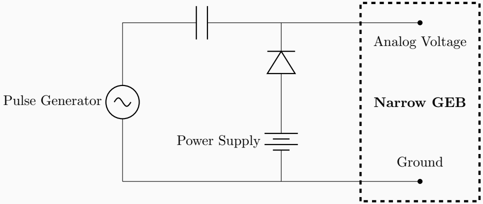
Example of a current spike observed in the HV current due to an alpha discharge in the chamber. I_Mon is the current monitored by the HV power supply. Each of the foils have a top and bottom, each with a HV channel, along with the drift making seven HV channels. The drop in current following the spike is the HV supply automatically ramping down the voltage after the current exceeds the current limit for that channel. The higher than normal currents observed before the discharge is due to HV probes being attached to the HV pads on the chamber and these probes have a resistance of only 200MΩ.

LV Alpha Discharges

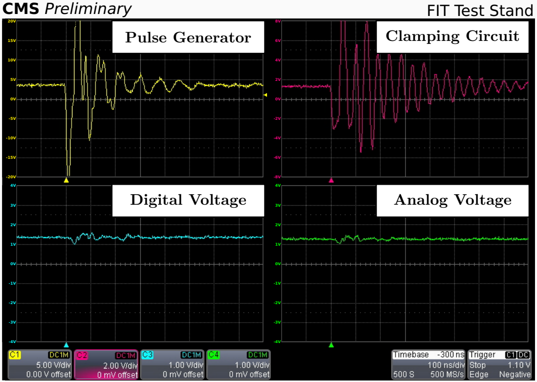


An example of LV ripples observed on the GEB during a discharge. The power supplied to the VFATs are split between an analog voltage supply and a digital voltage supply and these voltages were measured near the input to the VFAT on the GEB. Nominal voltage for both voltage supplies is 1.3V, and the discharge causes voltages to reach $\pm$5V. There are issues with attempting to measure the effect of discharges, since they are both damaging to the chamber and produce a large EM pulse. Attempts were made to reproduce VFAT resets without a discharge. The probes used here were shielded in copper to mitigate the effects from the EM pulse.

Injecting pulses into LV

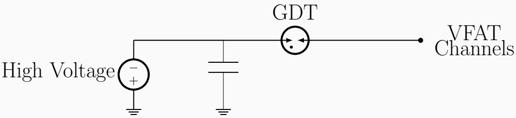


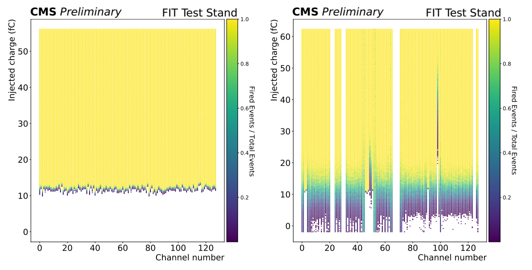
An example of a clamping circuit injecting voltage ripples into the voltage supplied to a VFAT. The theory being the voltage ripples cause the VFATs momentarily power off. Maxing out the pulse generator produces a ±20V pulse, which then produces ±7V ripple on the 1.3V supplied voltage. The digital and analog voltages were monitored near the VFAT, similar to the previous slide. It was found that capacitors on the GEB and VFAT filter out this ripple and the VFATs did not reset.

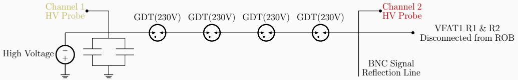


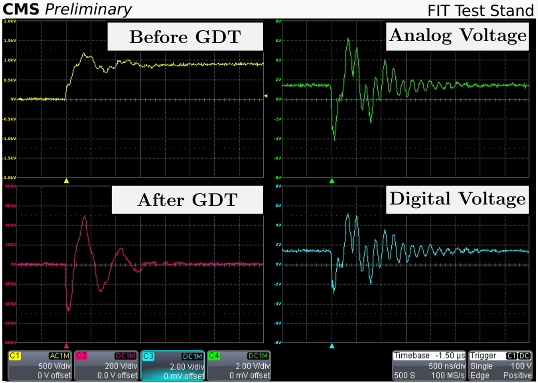
Injecting Charge into VFAT Channels

An example of charge injection S-curves for an undamaged VFAT channels (left), and the damaged channels after injecting charge with a Gas Discharge Tube (GDT) (right). During a discharge, a large amount of charge enters the VFAT readout channels, which could possibly cause the VFAT to reset. This was replicated by shorting a GDT into the VFAT channels. A GDT is a surge protection device, when a certain voltage is placed across it, it shorts out. The damage on the channels can be seen with an S-curve plot. S-curves are taken by injecting charge into the VFAT channel 100 times and recording of those 100 injections how many times the VFAT channel triggers. This is done for a variety of amount of charge injected and is shown for all 128 VFAT channels. Even with lasting damage done to the VFAT channels, the VFAT did not reset.



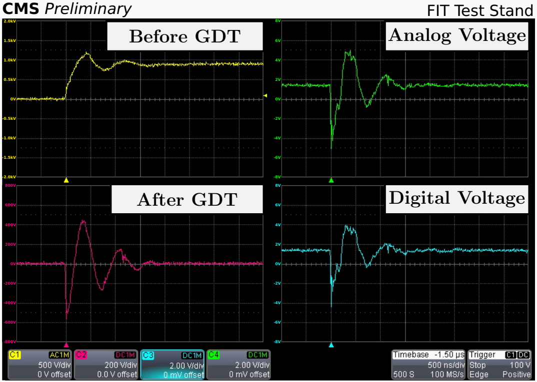






Voltage ripples from GDT circuit injecting charge into GND and subsequent LV ripples from GEBs. Theory here is that during a discharge a voltage gets applied to GND, causing the voltage ripples on the GEBs. The GDT circuit was connected to R1 & R2 on the VFAT, which connects the readout board GND to the VFAT analog GND. With the GDT circuit discharging at 920V, this produced a $\pm$4V ripple on the GEBs. An untermninated coaxial cable was used to create signal reflections, increasing the frequency of the LV ripples to more closely mimic the behavior seen from alpha discharges. This setup was able to consistently cause VFATs to reset.

Voltage ripple from the GDT circuit without the signal reflection line. This was done to see if the behavior of the VFAT reset would change. It was found that even though the amplitude of the LV ripples are the same as with the previous set up, the VFAT did **NOT** reset. This means the VFAT reset is related to the frequency of the incoming signal.



References

[1] CMS Collaboration, *The Phase-2 Upgrade of the CMS Muon Detectors: Technical Design Report*, CERN-LHCC-2017-012, CMS-TDR-016, (2017).