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Characterisation of analogue MAPS produced in the 65 nm TPSCo process

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Abstract: Within the context of the ALICE ITS3 collaboration, a set of MAPS small-scale test structures were developed using the 65 nm TPSCo CMOS imaging process with the upgrade of the ALICE inner tracking system as its primary focus. One such sensor, the Circuit Exploratoire 65 nm (CE-65), and its evolution the CE-65v2, were developed to explore charge collection properties for varying configurations including collection layer process (standard, blanket, modified with gap),

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pixel pitch (15, 18, 22.5 µm), and pixel geometry (square vs hexagonal/staggered). In this work the characterisation of the CE-65v2 chip, based on ^{55}Fe lab measurements and test beams at CERN SPS, is presented. Matrix gain uniformity up to the $\mathcal{O}(5\%)$ level was demonstrated for all considered chip configurations. The CE-65v2 chip achieves a spatial resolution of under 2 µm during beam tests. Process modifications allowing for faster charge collection and less charge sharing result in decreased spatial resolution, but a considerably wider range of operation, with both the 15 µm and 22.5 µm chips achieving over 99% efficiency up to a ~180 e^- seed threshold. The results serve to validate the 65 nm TPSCo CMOS process, as well as to motivate design choices in future particle detection experiments.

KEYWORDS: Particle tracking detectors (Solid-state detectors); Solid state detectors; Analogue electronic circuits

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Contents

1 Introduction

Monolitihic Active Pixel Sensors (MAPS) combine the passive sensor and active readout chip onto the same silicon die. MAPS offer a variety of advantages with respect to their hybrid counterparts, including a lower material budget, cost, reduced power consumption, and smaller pitch as bump bonding is not needed. MAPS have already seen adoption by a wide variety of ongoing and proposed (collider) physics experiments including the STAR Experiment [1], the ALICE Experiment [2], the EIC [3], and the FCC-ee [4].

The ALICE experiment implemented a full MAPS-based tracking detector, consisting of 7 concentric layers, during its Inner Tracking System (ITS) upgrade during the second long shutdown of the LHC, denoted ITS2 [2], in the first adoption of MAPS at the LHC. To further improve tracking and vertexing performance, the ITS3 upgrade [5] seeks to replace the three innermost layers of the ITS2 with three fully cylindrical layers consisting of wafer-scale bent sensors, targeting an excellent spatial resolution of the chips (5 µm) and low material budget (0.09% X_0/layer). The layers will rely on the stitching technique supported in the commercially available TPSco 65 nm CMOS imaging process. In the context of the ITS3 upgrade, a set of small-scale test structures were produced in a submission in December 2020: Analogue Pixel Test Structure (APTS [6]), Digital Pixel Test Structure (DPTS [7]), and the Circuit Exploratoire 65 nm (CE-65 [8]). A second submission at the beginning of 2023 allowed for the evolution of some of the small-scale test structures, including the CE-65v2: the evolution of CE-65.

The CE-65v2 chip was developed to investigate the charge collection and electrical properties of the 65 nm CMOS process through a selection of chip variants. The chip consists of a matrix of 1152 pixels organised in 48 columns and 24 rows, with a rolling-shutter readout. The in-pixel electronics consists of a AC-coupled amplifier that is DC-separated from the input stage of the readout electronics, allowing for the application of a resetting voltage for the reverse biasing of the sensor to the reset node. A resetting voltage of 10 V was applied throughout these studies in order to achieve full depletion. In total, there are 15 variants of the CE-65v2 chip targeting the exploration of 3 main axes:

- Process variation: Standard, Modified, Modified with Gap
- Pitch variation: 15 µm, 18 µm, 22.5 µm
- Matrix geometry: square vs hexagonal

In this work, the first two axes are explored. A total of four chips corresponding to the 15 µm and 22.5 µm chips in the Standard process and the 15 µm and 22.5 µm chips in the Modified with Gap process were considered in these studies.

Adopting a smaller pitch allows for an improvement in spatial resolution, but comes with significant drawbacks with respect to power consumption, readout-rate, as well as difficulties during manufacturing. Thus it becomes necessary to explore the pitch size at which the desired spatial resolution can be achieved, without compromising other aspects of the chip and system design.

The process variations are detailed in ref. [9]. Figure 1a depicts the Standard process consisting of an n-well collection electrode, and in-pixel CMOS circuitry that is isolated from the epitaxial layer by a deep p-well. The depletion region begins to develop at the n-well collection electrode and follows a balloon shape in the epitaxial layer until the p+ substrate is reached. Due to the limited depth of the epitaxial region of $O(10\,\mu m)$, the lateral region remains undepleted, resulting in diffusion-dominated charge collection. In effect, charge collection is slow and subject to charge trapping, whilst exhibiting high charge sharing between pixels. Figure 1b depicts the Modified with Gap process which has, in addition, a deep low-dose n-type implant between the epitaxial layer and the CMOS circuitry, with gaps at the pixel edges. The depletion region in the Modified with Gap process extends laterally, as the gaps allow for the development of the electric field. The lateral electric field induces drift-dominated charge collection even at the edges, resulting in faster charge collection and reduced charge sharing.

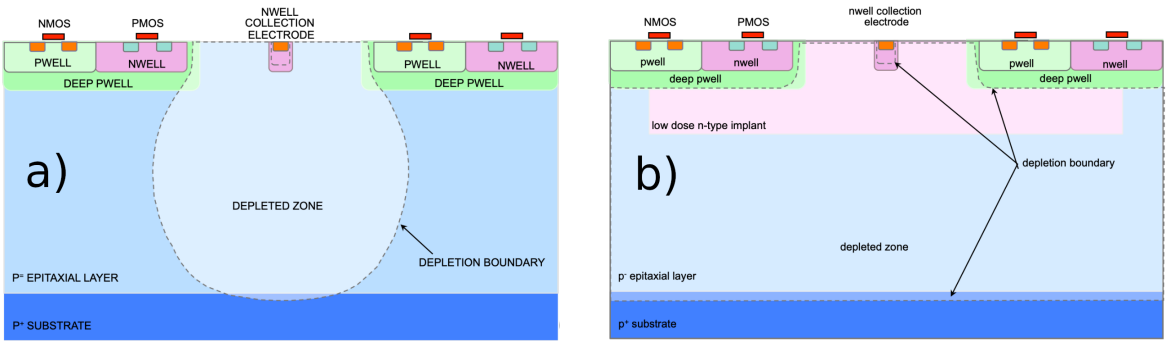

Figure 1. Cross-sections of the CE-65v2 pixels detailing the Standard process (a) and the Modified with Gap process (b). Reproduced with permission from [5].

2 Characterisation with radioactive source

An extensive characterisation of the CE-65v2 chip was performed using X-rays from an ^{55}Fe source. In particular, the X-ray spectrum of ^{55}Fe is determined by the electron transitions possible during the electron capture decay of ^{55}Fe to ^{55}Mn. The most prominent peak (K_α) is at a known energy of 5.9 keV, with a secondary peak (K_β) at an energy of 6.5 keV, with the peak width being determined primarily by the energy resolution of the given detector. A mapping from the measured Analog-to-Digital Units (ADUs), resulting from the quantization of the measured voltage by a 16-bit Analog-to-Digital Converter, to energy can be performed by matching the peak position of the K_α (and K_β) X-rays. The energy is often expressed in terms of electrons corresponding to the number of electron-hole pairs produced by the impinging X-ray. The different flavours of the CE-65v2 were measured at constant 20^oC using a chiller for temperature control. The signal is computed by subtracting temporally

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consecutive pixel frames to minimize baseline noise fluctuations. For a given event the 3×3 matrix surrounding the most energetic pixel is considered. If the pixel passes a threshold of 1000 ADUs then it is considered a seed for cluster reconstruction. Adjacent pixels must pass a threshold of 300 ADUs, corresponding to approximately 2 times the Root Mean Square (RMS) noise, to be considered neighbours. Figure 2a depicts the measured ^{55}Fe spectrum for single pixel clusters for the CE-65v2 chip in the Modified with Gap process with a 15 µm pitch. The main K_α peak, centered around ~6900 ADUs, is fitted with a Gaussian distribution to extract the peak position. The neighbouring K_β peak, which would be expected at ~7480 ADUs, cannot be resolved due to pixel-to-pixel gain variations across the matrix. The same procedure was repeated for the 22.5 µm pitch chip, as well as the 15 µm and 22.5 µm chips in the Standard process, yielding similar spectra and peak positions. As shown in figure 2b, the main K_α peak position for the 15 µm Standard process chip is within 1.6% of the 15 µm Modified with Gap process chip. This outcome is anticipated, as the capacitance should not vary significantly when the chips are fully depleted. The same procedure was repeated for the single-pixel spectrum of individual pixels, yielding much cleaner spectra, at the cost of limited statistics, as can be seen in figure 3a.

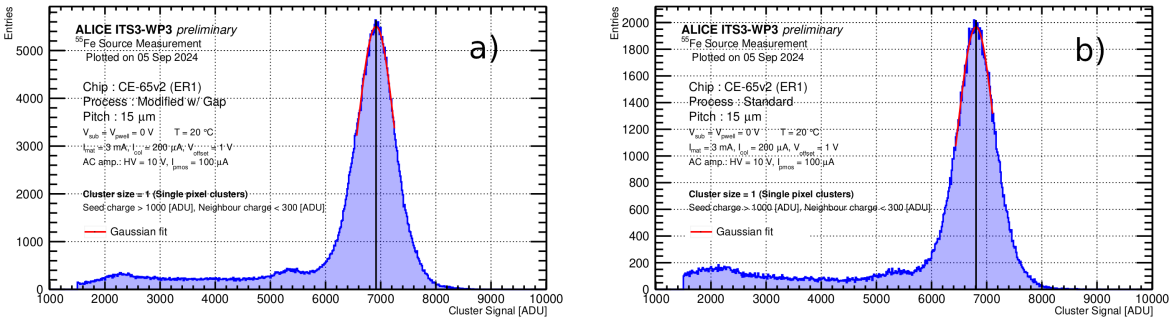

Figure 2. ^{55}Fe spectrum for single pixel clusters of the entire matrix of the CE-65v2 chip in the Modified with Gap process (a) and Standard process (b) with a 15 µm pitch. The Gaussian fit is marked in red.

The energy resolution of 4.8%, obtained as the ratio of the Full Width at Half Maximum and mean peak position, is considerably better than that of the global spectrum in figure 2a, where it is 11.5%. Moreover, the K_β peak can be clearly resolved. Figure 3b summarizes the gain uniformity of the 15 µm chip in the Modified with Gap process by depicting the K_α peak position for each individual pixel, normalized by the mean K_α peak position for all pixels. No clear spatial pattern can be discerned, and indeed the variance of the gain between pixels is of $O(5\%)$. Similar trends hold for the other three chips, with the variance being of $O(5\%)$ in all cases. The initial characterisation with radioactive sources provided valuable insights into the gain uniformity and baseline performance, which were essential for validating the test beam measurements.

3 Testbeam results

Test beam measurements were conducted at CERN SPS (H6 beamline) [10] to study the efficiency and resolution of different CE-65v2 variants. A telescope consisting of six ALPIDE [11] planes and using the DPTS [7] chip as a trigger was used. The telescope resolution was estimated to be 2.2 µm using a telescope optimizer [12] for the given geometry. All tests were conducted at 20^oC using a chiller to stabilize the device under testing. Data analysis was carried out using the Corryvreckan

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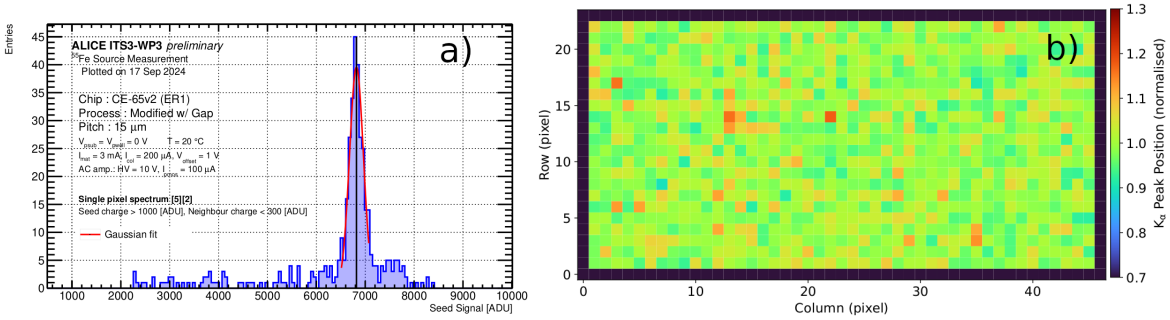

Figure 3. a) ^{55}Fe spectrum for single pixel clusters for an individual pixel (x=5, y=2) of the CE-65v2 chip in the Modified with Gap process with a 15 µm pitch. The Gaussian fit is marked in red. b) Gain distribution of the CE-65v2 chip in the Modified with Gap process with a 15 µm pitch obtained by considering the normalized K_α peak position (figure 3a) for each pixel.

framework [13], with tracks reconstructed using a straight-line track model that required hits on all six ALPIDE planes. Clusters on the CE-65v2 chip were built by summing all pixels in a 3×3 window around a seed pixel passing an 100 e^- threshold. The maximum cluster size is thus by definition 9. For electron threshold scans, identical seed and neighbour threshold cuts were applied for the pixels in the cluster, before their contributions were summed. A signal-to-noise ratio greater than 3 was required for all seed pixels. Multiple cluster candidates were considered corresponding to each pixel passing the required seed e^- threshold and signal-to-noise ratio. Clusters within a 75 µm radius were associated with a given track, with the nearest cluster selected in cases of multiple candidates.

The efficiency as a function of electron threshold was studied for each of the four chip variants. In the Standard process, an efficiency of over 99% is achieved up to ~130 e^- and ~150 e^- for the 15 µm and 22.5 µm chips respectively, as depicted in figure 4a. The efficiency drops with respect to increasing threshold, but does so faster for the 22.5 µm pitch chip. In the Modified with Gap process, an efficiency of over 99% is achieved up to ~180 e^- for both the 15 µm and 22.5 µm chips, as depicted in figure 4b. The drop in efficiency is considerably slower with respect to the Standard process chips. The difference with respect to pitch size is marginal, with the 22.5 µm chip maintaining slightly higher efficiency.

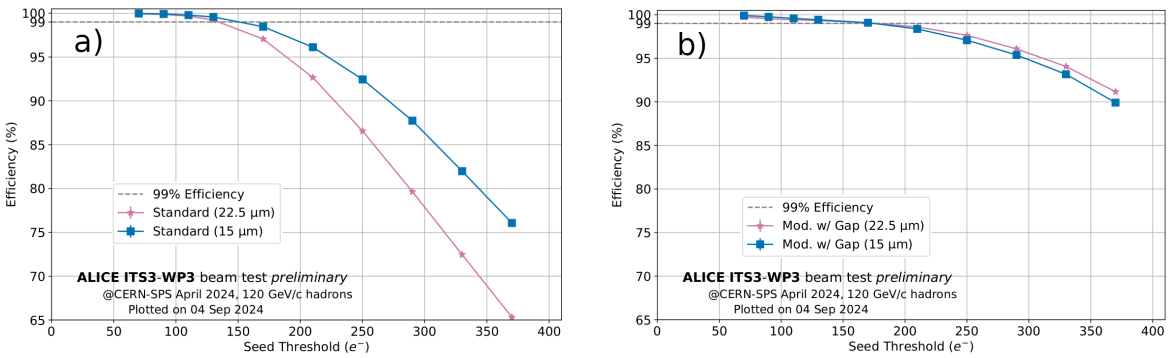

Figure 4. Efficiency as a function of seed threshold (e^-) for the CE-65v2 chip with 15 µm (blue) and a 22.5 µm pitch (pink) in the Standard (a) and the Modified with Gap process (b). The 99% efficiency line (dotted) is marked explicitly.

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The spatial resolution of the chip variants was likewise studied with respect to increasing electron threshold. For each threshold the full analogue information was used to compute the centre-of-mass position of a given cluster using the seed and neighbour thresholds given previously in this section. In the Standard process, an excellent resolution of ~1.5 µm and ~2 µm can be achieved at a seed threshold of 70 e^- for the 15 µm and 22.5 µm chips, as depicted in figure 5a. The performance degrades quickly in the 70 e^-–250 e^- range as the cluster size decreases, before plateauing at ~3 µm and ~4 µm for the 15 µm and 22.5 µm chips. For both chips a resolution that is considerably better than the binary resolution of pitch/$\sqrt{12}$ is achieved. Figure 5b depicts the resolution as a function of increasing e^- threshold for the Modified with Gap process chips. The Modified with Gap chips achieve a worse resolution compared to the Standard process chips for all considered thresholds, especially for the 15 µm pitch chip. The resolution is, however, more stable with increasing thresholds. Comparing the two pitches for the Modified with Gap process chips, the 22.5 µm chip displays less variation increasing slightly to just above 5 µm resolution, in parity with the Standard process chip.

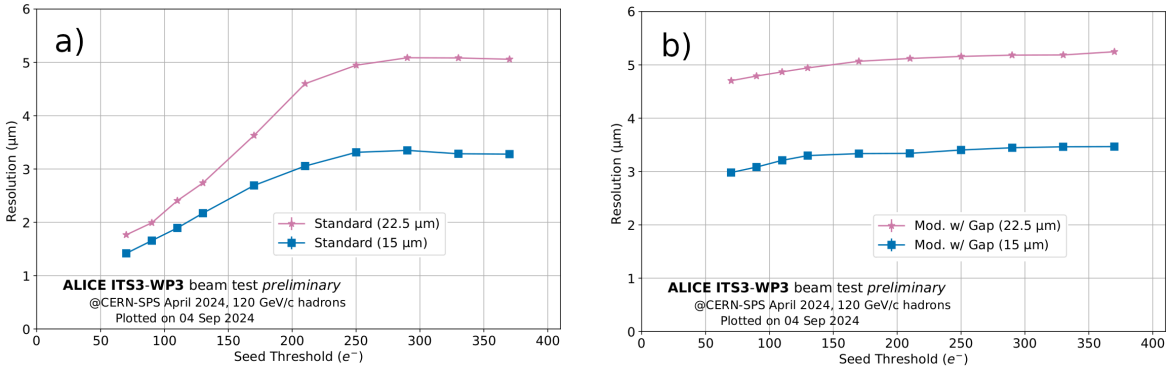

Figure 5. Resolution as a function of seed threshold (e^-) for the CE-65v2 chip with 15 µm (blue) and a 22.5 µm pitch (pink) in the Standard (a) and the Modified with Gap process (b).

Charge sharing behavior significantly impacts both efficiency and spatial resolution, making it essential to assess across different pixel configurations. To study the extent of charge sharing for the different CE-65v2 variants, the accumulated charge ratio was determined by charge-ordering the pixels in a given cluster, and successively summing the charge of individual pixels, until a cluster size of 9 was obtained. The accumulated charge was then normalized by the total charge, defined as the sum of the charge of all pixels in a 3x3 window around the seed pixel, to obtain the accumulated charge ratio. Figure 6a depicts the accumulated charge ratio as a function of pixels in the cluster for the 22.5 µm pitch chip in the Standard process. The average charge fraction carried by the central pixel is less than ~60%, with the most probable value being even lower at ~45%, showing the high charge sharing characteristic of the Standard process. The most extreme charge sharing was found for the 22.5 µm pitch chip in the Standard process due to the competing effects of a larger pitch, whereby more charge is collected due to the larger area, and the electric field not propagating well at the pixel edges, resulting in considerably less charge drift. It is important to note that due to charge ordering, negative noise contributions, resulting from the frame subtraction described in section 2, can appear in the larger cluster size bins, as shown on the right side of figure 6a. These noise contributions may cause the accumulated charge ratio to exceed 100%.

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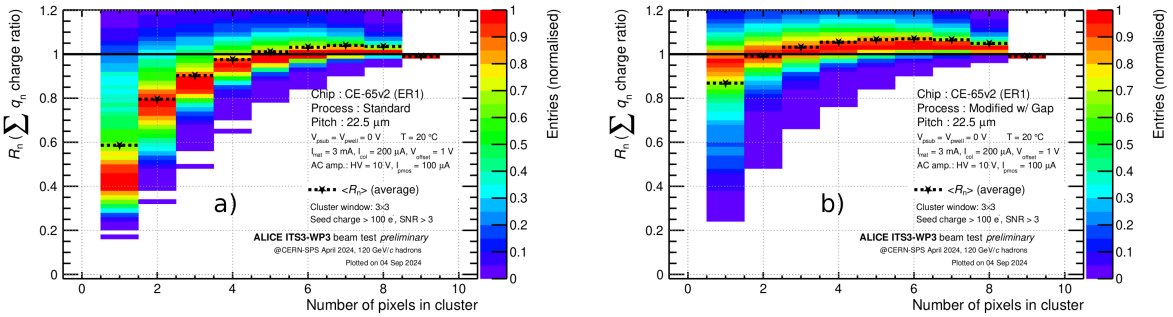

Figure 6. a) Accumulated charge ratio as a function of number of pixels in a cluster for the CE-65v2 chip with a 22.5 µm in the Standard (a) and Modified with Gap process (b).

Figure 6b, on the other hand, depicts the accumulated charge ratio as a function of pixels in the cluster for the 22.5 µm pitch chip in the Modified with Gap process. The average charge fraction carried by the central pixel is considerably higher with respect to the Standard process chip, with the charge fraction being over 85%. When considering the two most energetic pixels, both the average and most probable value of accumulated charge are around unity, suggesting that the vast majority of events consist of single-pixel or two-pixel events. Indeed, it is to be expected that if a hit occurs close to the edge of the pixel, then charge is shared with the neighbouring pixel, otherwise it is almost entirely collected due to the strong drift current evident in the Modified with Gap process. Due to the Gap modification at the pixel boundaries, the electric field does propagate well at the pixel edges, unlike in the Standard process. Coupled with a larger pitch this results in the lowest charge sharing of the four chip variants that were studied.

4 Conclusion

This work presents the first results of the CE-65v2 chip. A detailed comparison of the Standard process and the Modified with Gap process, as well as varying pixel pitch (15 µm, 22.5 µm) was made with particular emphasis on charge sharing properties and their ramifications on efficiency and resolution. Gain uniformity up to the $O(5\%)$ level was demonstrated for the considered CE-65v2 variants in ^{55}Fe lab tests. An excellent resolution in large-matrix 65 nm CMOS test structures was obtained during beam test measurements at the CERN SPS. The sub 3 µm spatial resolution obtained in the Standard process for both pitches satisfies FCC-ee requirements [4], and allows tradeoffs in pixel pitch with respect to power consumption, readout-rate, and manufacturing-ease. This enables a wide range of applications for 65 nm TPSCo MAPS. However, the spatial resolution was observed to quickly degrade when the chip is operated outside the low electron threshold regime, making it particularly sensitive to noise and radiation defects, including charge trapping. The Modified with Gap process displays a wide operating range with over 99% efficiency being achievable up to ~180 e^- for both the 15 µm and 22.5 µm chip. The wider range of operation and faster charge collection makes the process more suited for high radiation environments.

The complete characterisation of the CE-65v2 chip is currently underway. A full analysis of the CERN SPS results including the Modified "intermediate" process modification and 18 µm pitch chips is in progress. In addition, the use of the resetting voltage as a tool to tune charge sharing, and the impact of a hexagonal matrix pixel arrangement on cluster size and resolution are likewise being

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studied. Radiation tolerance studies using irradiated CE-65v2 chips were performed in May 2024 at DESY, and will complement the results obtained thus far. In summary, the characterisation of the CE-65v2 chip has supplemented the APTS [6] and DPTS [7] studies in the validation of the 65 nm TPSCo process as a candidate technology for advanced particle detection applications, including the ALICE ITS3 upgrade. The demonstrated spatial resolution, efficiency, gain uniformity, and ongoing studies pertaining to matrix geometry and radiation tolerance will further help refine the design parameters necessary for efficient tracking systems in future high-energy physics experiments.

Acknowledgments

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