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RD50-MPW: a series of monolithic High Voltage CMOS pixel chips with high granularity and towards high radiation tolerance

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Abstract: A series of monolithic High Voltage CMOS (HV-CMOS) pixel sensor prototypes have been developed by the CERN-RD50 CMOS working group for potential use in future high luminosity experiments. The aim is to further improve the performance of HV-CMOS sensors, especially in terms of pixel granularity, timing resolution and radiation tolerance. The evaluation of one of this series, RD50-MPW3, is presented in this contribution, including laboratory and test beam measurements. The design of the latest prototype, RD50-MPW4, which resolves issues found in RD50-MPW3 and implements further improvements, is described.

Keywords: Particle tracking detectors; Particle tracking detectors (Solid-state detectors); Radiation-hard detectors

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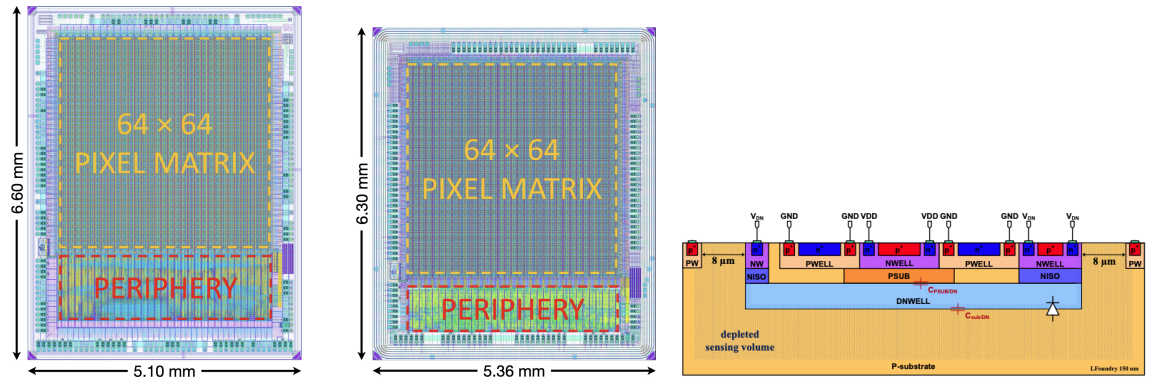
1 Introduction

Tracking applications in future physics experiments, such as High Luminosity LHC upgrades, e^+e^- colliders and the FCC-hh, impose extreme requirements on sensor technologies in terms of high granularity, fast timing resolution and excellent radiation tolerance while being low-mass and low-power, covering large areas and having an affordable cost per area. Depleted monolithic CMOS sensors are a very promising technology. However, to meet all these requirements in a single device, further R&D is needed to advance the performance of the sensors. The series of RD50-MPW chips are generic R&D prototypes, in the 150 nm High Voltage CMOS (HV-CMOS) technology process from LFoundry S.r.l, aimed at further developing depleted monolithic CMOS sensors while tackling the challenges of especially high pixel granularity (50 µm × 50 µm), fast timing resolution (0.1 ns) and excellent radiation tolerance (10^{16} n_{eq}/cm^2). An overview of the main results achieved so far within this programme is available in [1].

RD50-MPW3 consists of a matrix of 64 × 64 pixels and a digital periphery for effective pixel configuration and fast data transmission via I2C protocol and a 640 Mb/s LVDS line. The chip uses a column-drain readout architecture. It was fabricated on standard value, 1.9 kΩ·cm and 3 kΩ·cm resistivity p-type substrate. A detailed description of the design of RD50-MPW3 can be found in [2]. This paper presents the latest evaluation results of RD50-MPW3 in 1.9 kΩ·cm, including laboratory measurements in section 2 and test beam measurements in section 3. The design of the latest prototype, RD50-MPW4, is described in section 4. Figure 1 shows the layout views of RD50-MPW3 and RD50-MPW4, and the cross-section of a single pixel.

2 Laboratory measurements of RD50-MPW3

The leakage current of both a single pixel and n-type chip ring, measured when the substrate is biased through a topside p-type ring on the chip edge and using a probe station with needles, are shown in figure 2. The breakdown occurs at a bias voltage higher than 120 V, on the n-type chip ring. Before breakdown, the leakage currents of a single pixel and the chip ring are in the range of pA and nA respectively, which is within the range similar to other HV-CMOS sensors [4].



(a) RD50-MPW3. (b) RD50-MPW4. (c) Pixel cross-section (not to scale). Reproduced with permission from [3].

Figure 1. Layout views of RD50-MPW3 and RD50-MPW4, and cross-section view of a pixel.

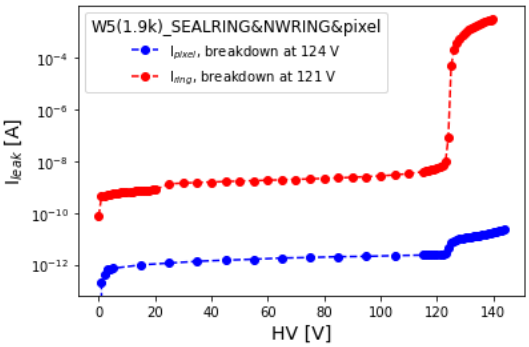


Figure 2. I-V curves of RD50-MPW3, including the leakage currents of a single pixel (blue line) and n-type chip ring (red line), measured at room temperature.

The baseline of the DAQ system is Caribou [5]. The time stamping mechanism of the RD50-MPW3 is operated with a 20 MHz clock, therefore allowing for a timing precision of 50 ns. The performance of the 64×64 pixel matrix is tested by analysing the S-curve response of each pixel to injection pulses when the chip is biased to -90 V. Figure 3 shows the Equivalent Noise Charge (ENC) of pixels extracted from the S-curves, including a map for each pixel in the matrix (figure 3(a)) and their histogram (figure 3(b)). The pixel matrix has a mean ENC value of 934 e^- with a standard deviation of 304 e^-. The high noise is due to coupling effects, as explained in section 4, and the large standard deviation due to large noise differences between the top and bottom halves. As a result, a threshold voltage of 1.3 V, i.e. 400 mV above baseline voltage (equivalent to 9 ke^- input charge), is used for this measurement. The pixel gain is measured to be 82.9 $\mu V/e^-$.

3 Test beam results of RD50-MPW3

The hit detection efficiency of RD50-MPW3 before and after neutron irradiation has been measured in a dedicated test beam using 4.2 GeV electrons at DESY in July 2023. The beam track positions on the RD50-MPW3 chips are obtained using the Adenium telescope [6]. Synchronisation between the RD50-MPW3 chips and Adenium is achieved with the AIDA TLU [7], using a time-stamp and

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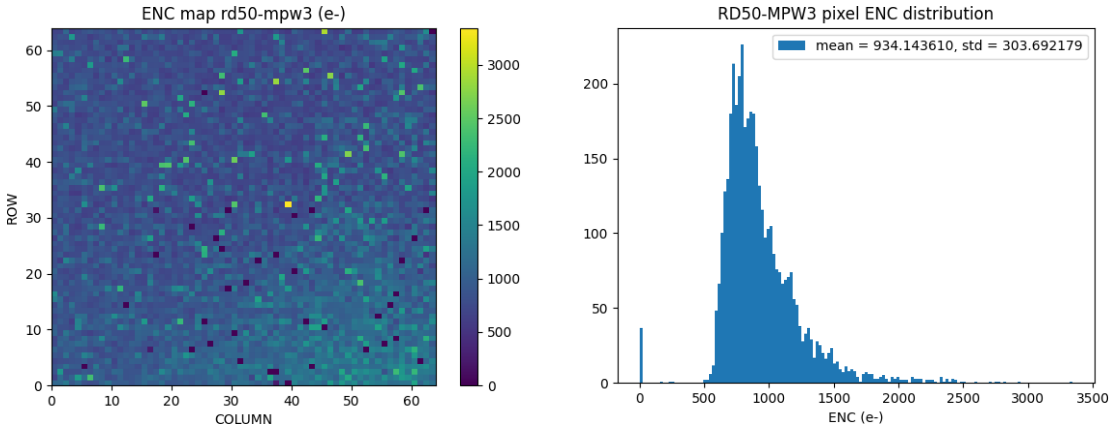
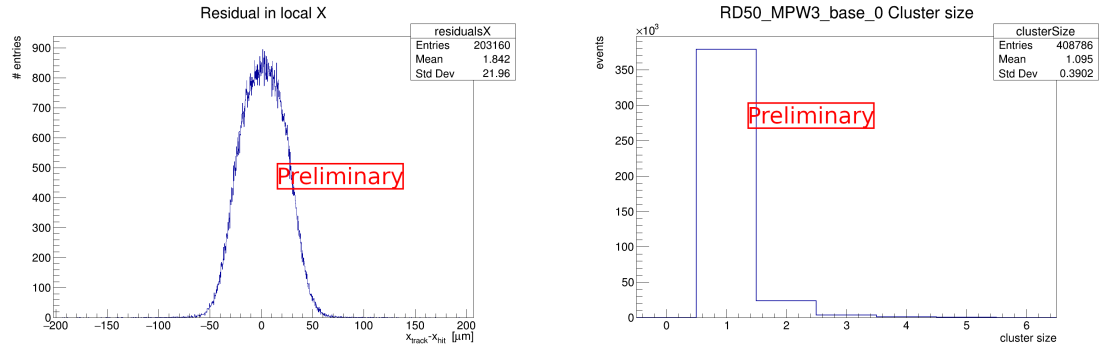


(a) ENC map. (b) ENC histogram.

Figure 3. ENC map and histogram for the pixel matrix of RD50-MPW3.

trigger number based approach. Two scintillators operated in coincidence are used as trigger. The RD50-MPW3 DAQ is fully integrated into the EUDAQ framework [8]. In order to handle the full readout rate a custom data collector, which receives User Datagram Protocol (UDP) packages generated by the FPGA on the *Xilinx Zynq 7000* board, is implemented with a speed of up to 1 GBit/s. The data analysis is performed with Corryvreckan [9].

The spatial resolution is obtained by comparing the intersections of a track from the telescope and a hit in RD50-MPW3, and is shown in figure 4(a). The discrepancy of the evaluated value of $\sim 21.96\,\mu\text{m}$ and the expected binary resolution of $62\,\mu\text{m}/\sqrt{12} \approx 17.8\,\mu\text{m}$ is currently under investigation. The measured cluster size of ~ 1.095 pixel per cluster shown in figure 4(b) can be explained by the high bias voltage of $-90\,\text{V}$ and the high threshold of $\sim 4.5\,\text{ke}^-$, as both reduce charge sharing effects between neighbouring pixels. Thus, this cluster size does not allow using centre of gravity approach to improve the spatial resolution of RD50-MPW3.



(a) Spatial residuals in X-direction. (b) Cluster size distribution.

Figure 4. General characteristics of non-irradiated RD50-MPW3. The spatial resolution is determined from the standard deviation of the residual.

For the evaluation of the efficiency, the number of hits that can be associated with a track at the interception position with RD50-MPW3 (N_{hit}) is compared to the total number of track interceptions (N_{tot}). The efficiency is thereby calculated by $\epsilon = N_{hit}/N_{tot}$. Figure 5(a) shows the total efficiency at

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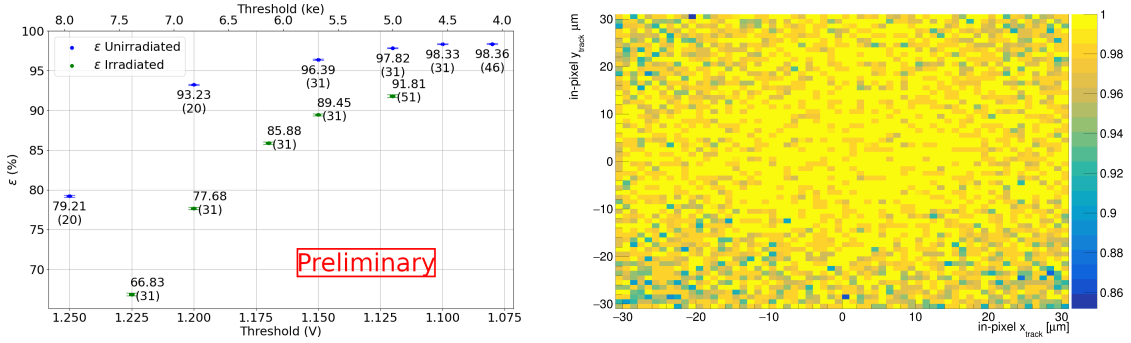
various threshold settings. The best total efficiency of ~ 98.3% is achieved at a threshold of 4.09 ke^- (equivalent to 1.08 V). Due to the noise issue presented above in section 2, an increasing number of rows has to be masked for lower threshold settings for both the non-irradiated and irradiated samples evaluated. An efficiency drop after irradiation is observed. The in-pixel efficiency in figure 5(b) shows a slight efficiency drop in the corners, which is due to charge sharing.



(a) Total efficiency as a function of the threshold.

(b) In-pixel efficiency map.

Figure 5. Efficiency measurements of non-irradiated and 1×10^{14} n_{eq}/cm^2 neutron irradiated samples when biased to −90 V. (a) The green data points correspond to the irradiated sample. The numbers of rows masked during data taking is indicated by the numbers in the brackets. (b) The in-pixel efficiency is evaluated with a threshold of ~ 4.5 ke^- for a non-irradiated chip.

4 Design of RD50-MPW4

4.1 Resolving high noise

The higher noise in the bottom half of the RD50-MPW3 pixel matrix indicates possible noise coupling from the digital readout periphery that operates at a clock frequency of 40 MHz. To better understand the issue, the parasitic-extracted view of RD50-MPW3 is used in simulation to replicate the high noise. In order to simplify this analogue simulation, a large amount of inverters driven by a 40 MHz clock signal are used to substitute the readout periphery and emulate its digital activity. Only one column of pixels is simulated to keep the simulation time reasonable. Figure 6(a) shows the simulated analogue output signals of three pixels at different locations: one from the bottom row which is the closest to the periphery, one from the middle of the matrix and one from the top row.

The simulation shows large noise with a frequency of 40 MHz in the output signals, which decreases from the bottom pixel to top pixel (peak to peak noise being 200 mV, 120 mV and 20 mV). This result confirms the noise coupling from the digital readout periphery. Since the digital power and ground domains in RD50-MPW3 are shared by the pixel matrix and periphery, the same simulation is performed after separating their digital power and ground domains. Figure 6(b) shows the simulated pixel output signals when the pixel matrix and periphery use different metal lines and pads for digital power and ground. The noise values of the three pixels are decreased to 20 mV and no location dependence is observed. Thus, the separated power and ground scheme is used in RD50-MPW4 as an attempt to resolve the high noise issue.

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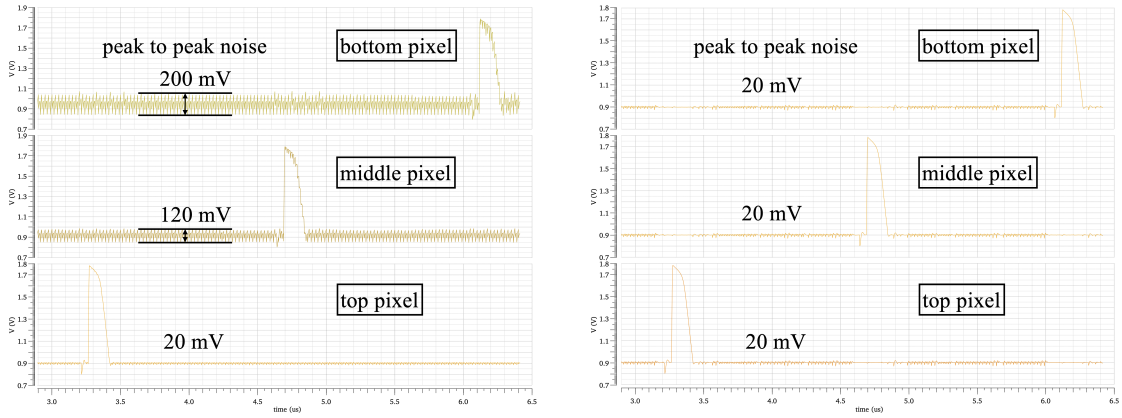

(a) Shared power and ground.

(b) Separated power and ground.

Figure 6. Simulated analogue output signals of pixels from different locations for two power and ground domains schemes: (a) the pixel matrix and readout periphery share the same digital power and ground; (b) the digital power and ground of the pixel matrix and periphery are separated.

4.2 Improved chip ring

RD50-MPW4 is fabricated on a Czocharlski-grown wafer with a substrate resistivity of 3 kΩ · cm. The chip is thinned down to 280 µm, and its backside is processed through the boron implantation, rapid thermal annealing, and metallisation. RD50-MPW4 requires a breakdown voltage greater than 300 V to enable a full depletion of the sensor substrate. This can be achieved by using the front-side (or edge) biasing method, which has proven performances on various depleted monolithic CMOS detector prototypes [10, 11]. In order to realise such a biasing method in RD50-MPW4, a new chip ring structure is required to be implemented.

The chip rings of RD50-MPW4 are designed based on the guard ring structure of a monolithic CMOS detector prototype LF-Monopix2 [4], featuring 5 floating n+p[1] guard rings which are implemented in the form of concentric arcs in the corners. In RD50-MPW4, the deep n-well is implemented at the innermost guard rings (GR1 and GR2), the GR3 is equipped with an n-well with intermediate depth, and the GR4 and GR5 are formed by using the standard (shallower) n-well implant (figure 7). Measurements on the test structures for this guard ring design have shown a breakdown voltage beyond 300 V [12, 13].

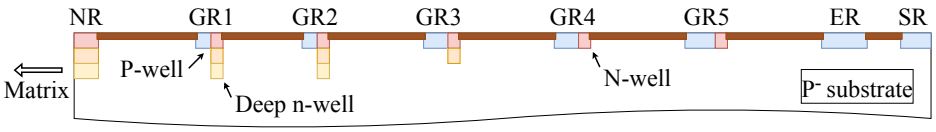

Figure 7. Schematic cross-section view of the new ring structure implemented in RD50-MPW4. The N-Ring (NR) is formed with the deep n-well implant, where the 3 n-type implants with different depths are distinguished by their colours. The n+p type ring structure is employed for the floating Guard Rings (GR1 to GR5), with different depths of the n-well. The Edge Ring (ER) is designed to use the p-well implant, and is electrically connected with the Seal Ring (SR).

[1]The so-called "n+p" well is a combination of p-well and an n-type implant. Using such a structure for the guard ring implants allows a breakdown voltage of 460 V ~ 500 V [11].

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5 Conclusion

The latest HV-CMOS prototype in the RD50-MPW series, RD50-MPW3, has been evaluated in laboratory and test beam facilities. The high coupling noise in the pixel matrix has been studied and understood. A succeeding chip, RD50-MPW4, has been developed to resolve the noise issue and further improve the radiation tolerance by increasing its breakdown voltage with a new chip ring structure.

Acknowledgments

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