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Outer Barrel services chain characterisation for the ATLAS ITk Pixel detector

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Abstract: For the high-luminosity upgrade of the ATLAS Inner Tracking detector of the ATLAS experiment, a new pixel detector will be installed to allow for a bigger bandwidth and cope with the increased radiation among other challenges. This contribution will present the evaluation of the Outer Barrel Pixel layer services chains. A full data transmission study covering data merging will be presented from the pixel module all the way to the FELIX data acquisition system, using most of the components foreseen for the detector. Challenges and results of the services chain of the Outer Barrel will be highlighted.

Keywords: Pixelated detectors and associated VLSI electronics; Particle tracking detectors (Solid-state detectors); Performance of High Energy Physics Detectors

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Contents

1 Introduction

The ATLAS experiment [1] will replace its current inner tracking system with a new all-silicon inner tracker (ITk) [2] for the upgrade of the High-Luminosity Large Hadron Collider (HL-LHC). An increase in the average number of pile-up events per bunch crossing from about 45 up to 200 and in the peak luminosity from $2 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$ to $5\text{–}7.5 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$ make this replacement needed. The target of the new upgraded ATLAS detector will be to collect about $4000\,\mathrm{fb^{-1}}$ of data. Requirements on the radiation hardness, granularity and data rate capabilities for the new detector are therefore much harder than for the current one.

The ATLAS Pixel ITk detector will consist of >10000 silicon modules [2] which means that there will be 5×10^9 pixels covering an active area of around $13\,\mathrm{m^2}$. These numbers are a factor fifty larger in the number of channels and a factor six larger in the sensitivity area with respect to the current ATLAS pixel detector. Furthermore, the on-detector readout will be done at 1.28 Gbps and the data will be converted into optical signals and multiplexed in fibres at rates of 10 Gbps. The readout chip has been designed by the RD53 collaboration and the results shown in this paper have been obtained with ITkPixv1.1 [3]. The detector will use evaporative CO_2 cooling and serial powering. This paper covers the results of the full chain data transmission tests performed in the context of the Outer Barrel Layer (OB) of the Pixel ITk detector for HL-LHC.

2 Outer Barrel data transmission chain overview

The goal of the OB data transmission chain is to ensure error free communication for both uplinks and downlinks. Uplinks involve data sent from the detectors with the sensed information to the Data Acquisition System (DAQ) at a maximum speed of 1.28 Gbps while downlinks carry clock, trigger and slow commands sent by the DAQ to the detector at a speed of 160 Mbps. A limit for total acceptable data loss was set to −20 dB by the ATLAS data transmission task force coordination management and it is stated as a requirement for the detector. This loss was deemed acceptable to interpret the data error-free. Each component has undergone individual testing and qualification for data transmission, ensuring that the cumulative losses across the system remain well below the specified threshold. The ultimate test involves assembling all the components into a complete system to verify the overall data transmission quality when all the elements are integrated.

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The data transmission chain within the Inner Tracker's OB layer comprises a mix of active and passive components. Figure 1 shows the system configuration used for the measurements presented in this paper.

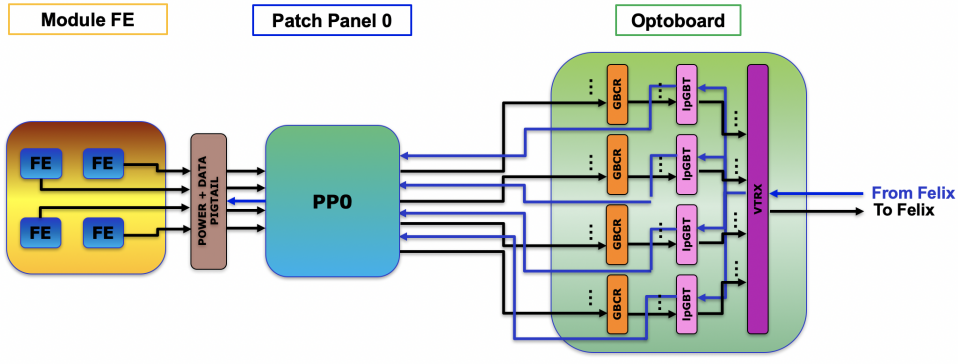

Figure 1. Diagram that includes the main components of the data transmission chain of the OB for ITk pixel upgrade.

The active components are:

- The Front-End (FE) modules consist of four ITkPixv1.1 readout chips bump-bonded to a planar sensor and glued to a flexible PCB. These modules are responsible for transmitting the uplinks at a rate of 1.28 Gbps and downlinks at 160 Mbps [4]. The data links (black arrows in figure 1) use Aurora 64/66 bits communication protocol [5]. Concerning the command link (blue arrows in figure 1) there is one link per module and every chip can be addressed individually via their chip ID. Otherwise the commands can be broadcast to all the chips within the module. For the measurements of this paper instead of a module, a digital quad was used so there is no sensor attached to ITkPixv1.1 but the rest is the same.

- The "GigaBitCableReceiver", GBCR [6], is a gigabit transceiver that features up to six upstream receiver channels. Its role is to enhance signal quality by equalising the signals received from the electrical services chain.

- The "low power Gigabit Transceiver", lpGBT [7], is a radiation-tolerant device that combines up to six 1.28 Gbps data links (in the ATLAS ITk Pixel context) and sends them to the FELIX DAQ system. It also receives the commands sent from FELIX and addresses them to the specific module at 160 Mbps.

- The VTRX+ [9] is a radiation hard electrical/optical transceiver.

The lpGBT, GBCR and VTRX sit on a common board called optoboard.

In addition to these Application-Specific Integrated Circuits (ASICs), which have been specifically designed to withstand the challenging environment of the HL-LHC, the data transmission chain includes several passive components crucial to facilitating the communication process. These passive elements include:

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- The module hybrid is a flexible printed circuit board (PCB) with minimal material, to which the readout electronics and sensors are wire-bonded. It serves as interconnection between the FEs and the external cables enabling data merging among the FEs. This functionality is explained in section 4.
- The data and power pigtails are responsible for transmitting data to and from the detector and supplying the necessary power. They deliver low voltage to the transistors and high voltage to the sensors. These pigtails are connected on one end to the module and on the other end to the Patch Panel 0 PCB (PP0).
- The Patch Panel 0 (PP0) is a PCB that connects the data lines to the twinaxial cables, sends the commands to the modules and delivers the power.
- The optoboard [10], receives data from the PP0 via twin-axial cables that extend up to 6 meters, equalises the data and serialises it. It then converts the electrical signals into optical ones, which is transmitted to the DAQ.

In conclusion, this section details the components and systems that comprise the Inner Tracker's OB data transmission chain, encompassing both active and passive elements which crucial for its reliable operation.

3 Outer Barrel data transmission measurements

This section outlines the various tests performed at the system level, serving the purpose of ensuring error-free communication in the OB data transmission chain.

Firstly, eye diagrams, which are visual representations of signal quality of both uplinks and downlinks were recorded. The signals were directly probed at various key points in the system, including the input/output of the GBCR and the input of readout chips in the module. Parameters such as the equalisation level provided by the GBCR or the amount of pre-emphasis and amplitude of the signal set in the Front-End (FE) electronics were studied for these tests. Finally, manual checks were performed to ensure that the lpGBT phase alignment was correct. The optimisation of these parameters were instrumental in gaining insights into the analogue response of the signal.

Once the eye diagrams had been understood and various configurations were identified as optimal or less optimal for the data transmission chain, decoding tests were performed. This check operates on the decoded data (data after it has passed through the entire data transmission chain) and counts the number of bit flips (changes in individual bits) in the 'fixed' bits of the Aurora Idle frame, a specific frame continuously sent in the Aurora protocol. The configurations identified as optimal in the measurements should correspond to no bit flips observed by the soft error counters.

The final check performed was to readout signal from the module, in which data propagates over the full chain and is interpreted to generate plots. Every pixel is injected a high charge (above threshold) a known number of times via an external capacitance and it is checked if it fired for every injection.

Figure 2 shows two eye diagrams. The left one represents the data line operating at a speed of 1.28 Gbps. It was captured at the output of the lpGBT, on the optoboard, which is the end of the electrical transmission line before the VTRx. In this test, the ITkPixv1.1 output amplitude was set to a medium range value with no in chip pre-emphasis and the GBCR was providing medium equalisation. On the right, the eye diagram of the command that operates at a rate of 160 Mbps

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can be observed, measured at the input of the module. The command bypasses the GBCR so there is no equalisation. Both eye diagrams exhibit open eyes, indicating a successful data transmission. However, it is worth noting that in the data line, the jitter is more relevant due to its higher speed and it is in the order of 370 ps which is within specifications.

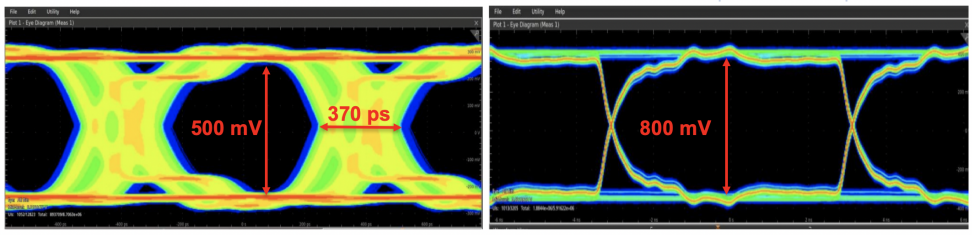

Figure 2. Eye diagrams of data (left) and command (right) line of the OB data transmission chain.

The decoding measurements were conducted with manual phase alignment of the incoming data to the lpGBT. Table 1 presents the results of this test for the configuration of the data line shown in the eye diagram. It also includes the outcome of the readout test performed with one of the FEs of the modules. The top row lists the applied phase in the lpGBT. In the 'SOFT ERRORS' row, the green colour code indicates an error-free communication scenario, the orange colour signifies the overflow of the error counter register, thus noisy, data and the red colour means that there is no data flow as the lpGBT couldn't lock. It can be observed that for more than half of the phases, there are no bit flips in the data received.

Table 1. Decoding and readout tests outcome for one data line at 1.28 Gbps for different phase settings of the lpGBT.

lpGBT PHASE	0	3	6	9	12	15
SOFT ERRORS	Perfect scan	Perfect scan	No data flow	Perfect scan	Noisy data	No data flow

4 Data merging in the Pixel detector and merging tests

Given the mechanical constraints of the OB region, it is not possible to have a physical data link for each FE in a module and therefore read them individually. To address this constraint and becuase the expected occupancy allows for it, a data merging mechanism has been introduced. It serves both for data readout and material reduction. To optimise material usage, data merging has been adopted across all layers of the OB. Figure 3 explains this concept for ITkPixv1.1 in the leftmost plot. Each FE can receive up to 4 data links at 320 Mbps and send out 4 links at a programmable speed. In the case of the ATLAS detector the output speed is set to 1.28 Gbps.

Two types of data merging are used depending on the distance of the detector layer from the interaction point, as shown in the middle and right images of figure 3. In the first type, FE1 sends data to FE4 and FE3 sends data to FE2. FE2 and FE4 act as transmission chips of the module sending the data out. In the second type, FE1, FE2 and FE3 send data to FE4, which is the transmission chip for the entire module.

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Figure 3. Data merging shceme of ITkPixv1.1. FE chip (left) input and output lines capabilities and the two modes of data merging (center and right) used in the OB layer.

ITkPixv1.1 encountered a known issue where data flow was affected by the phase relationship between data and clock signals of the internal serialiser during data merging. In order to verify that the data merging capabilities can be achieved, a workaround to this issue was developed. The phase between the clock and the data coming from a FE can be adjusted acting on the power rail of the FE which can be used to align the data before the merging. A 'trim scan' was developed to explore all 16 possible values of the global configurations register 'Voltage_trim' [3] which enables adjustments of up to ±160 mV relative to the nominal voltage of 1.2 V for both AVDD and DVDD. This means that the transistors can be powered in a range from 1.04 to 1.36 V, and each trim step is approximately 20 mV. This scan injects charges into the pixels and triggers them 100 times while the module is configured to operate in data merging mode. An example of the described scan is shown in figure 4. The colour axis represents the occupancy and the total recorded injections is also noted for every combination of trim values. The X and Y axis are the 16 possible values of AVDD and VDDD respectively. Several regions can be identified. The white corner signifies that there are no hits recorded in that region. Blue/green areas detect data losses, as the number of expected injections, shown in the right vertical scale, should be 100 and these regions see 20–50 hits. Finally, the yellow regions indicate that the data flow is error free, as 100 injections are recorded. Setting the trim values to anything within the yellow region for each FE will guarantee data transmission during data merging operation. This scan also shows that the values set during the module quality assurance process for the registers TrimA and TrimD represented with a black dot are not compatible with data merging and should be moved if operated in this mode.

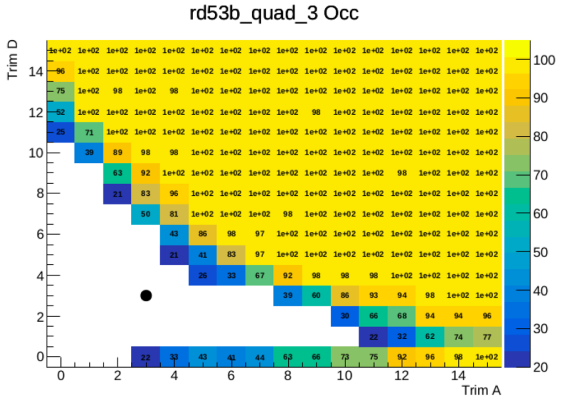

Figure 4. Trim scan output of a FE configured in type one of the two data merging modes.

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5 Conclusion

The OB system test for the ATLAS pixel ITk upgrade was crucial for assessing the data transmission capabilities. Three distinct measurements collectively showcased the reliability and effectiveness of the system. Furthermore, data merging with ITkPixv1.1, while successful, requires operating chips beyond their nominal voltages. A fix addressing this issue has already been implemented for the final readout chip, ITkPixv2. These findings suggest that the OB services chain are in the right path to ensure error free communication in the future detector while highlight the need of careful system test characterisation.

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