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The μ-RWELL in High Energy Physics and beyond

2024 JINST 19 C02057

G. Bencivenni,[a] R. de Oliveira,[b] E. De Lucia,[a] G. Felici,[a] M. Gatta,[a] M. Giovannetti,[a,*] G. Morello[a] and M. Poli Lener[a]

[a]*INFN, Laboratori Nazionali di Frascati, Via Enrico Fermi 54, 00044 Frascati (Roma), Italy*
[b]*CERN, Esplanade des Particules 1, 1217 Meyrin, Switzerland*

E-mail: matteo.giovannetti@lnf.infn.it

Abstract: The μ-RWELL, a resistive Micro-Pattern Gaseous Detector with a single amplification stage, is crafted using a copper-clad polyimide foil intricately micro-patterned with a blind hole (well) matrix. This matrix is integrated into the readout Printed Circuit Board, complemented by a thin Diamond-Like-Carbon sputtered resistive film, in order to mitigate the transition from streamer to spark regimes, enabling the attainment of substantial gains ($\geq 10^4$). However, this arrangement diminishes the detector's capacity to withstand high particle fluxes. For low-rate applications, the simplest resistive configuration utilises a single resistive layer with edge grounding. This design, however, exhibits a non-uniform response under elevated particle irradiation. To overcome this behaviour, new current evacuation geometries have been developed. In this work, we examine the efficacy of various high-rate resistive layouts, trialled at the prestigious CERN H8-SpS and PSI πM1 beam testing facilities. These designs are tailored to meet the demanding requisites of detectors operating in the HL-LHC environment, as well as those of future experiments at the next generation colliders, such as the FCC-ee/hh and CepC.

Keywords: Gaseous detectors; Micropattern gaseous detectors (MSGC, GEM, THGEM, RETHGEM, MHSP, MICROPIC, MICROMEGAS, InGrid, etc); Particle tracking detectors (Gaseous detectors)

*Corresponding author.

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Contents

1 Introduction

The μ-RWELL, figure 1, is a single-amplification stage resistive Micro Pattern Gasour Detector (MPGD) [1]. The R&D efforts for the μ-RWELL are focused on augmenting its stability to intense irradiation, while streamlining its fabrication processes for straightforward industrial transfer. This is a pivotal step towards its widespread application in fundamental research at future colliders, extending even beyond the realm of High-Energy Physics (HEP). Comprising two primary components, the detector includes a cathode — a rudimentary FR4 Printed Circuit Board (PCB) with a fine copper layer on one side — and the μ-RWELL_PCB, which forms the detector's core. The μ-RWELL_PCB is a multi-layered circuit fabricated using standard photo-lithography techniques. It consists of a patterned single copper-clad polyimide (Apical®) foil,[1] serving as the detector's amplification component; a resistive film of Diamond-Like-Carbon (DLC) acting as a discharge limitation stage; and a conventional PCB for readout, segmented into strip, pixel, or pad electrodes.

By applying a suitable voltage between the copper layer and the DLC, the well serves as a multiplication channel for the ionization occurring in the drift gas gap, figure 2. The charge induced on the resistive film disperses with a time constant [2, 3], which depends on the surface resistivity and the distance between the resistive layer and the readout plane. The μ-RWELL spark suppression mechanism is akin to that of Resistive Plate Counters (RPCs) [4–7]: the streamer formed within the amplification volume, which induces a substantial current through the resistive layer, results in a local reduction of the amplifying voltage. This quenches the multiplication process in the gas, significantly mitigating the discharge amplitude. Consequently, it allows the detector to operate at high gains

[1] The foil is 50 μm thick polyimide coated on one side with a 5 μm thick copper layer, akin to the base material used in GEM.

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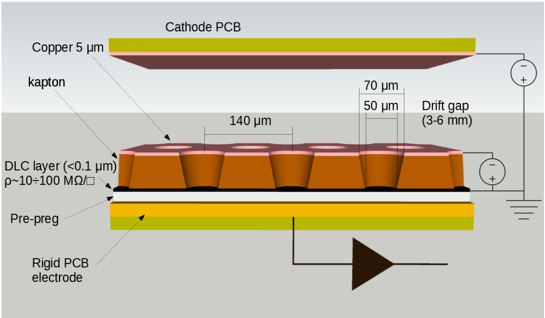

Figure 1. Layout of the µ-RWELL.

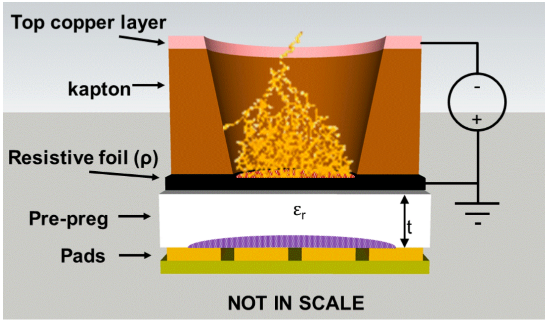

Figure 2. Principle of operation of the µ-RWELL.

($\geq 10^4$) with a single amplification stage. The drawback of this protection mechanism is its diminished capacity to handle high particle fluxes. Indeed a detector relying on a simple single-resistive layout suffers at high particle fluxes of a non-uniform response over its surface, more evident as the size of the detector increases. This effect, related to the average resistance encountered by the charge produced in the avalanche, depends on the distance between the particle incidence point and the detector's grounding line. In the following, new resistive layouts have been developed for high rate purposes and their performance in terms of efficiency and rate capability was measured in beam tests at CERN H8-SpS and PSI πM1 and with an X-ray tube respectively.

2 The high rate layouts

The simplest scheme for current evacuation in a µ-RWELL employs a single resistive layer with a grounding line at the edge of the active area, figure 3, (Single-Resistive Layout, SRL). In large devices, the path of the current to the ground can be heavily influenced by the particle's incidence point. To mitigate this effect, the key is to minimize the average path to the ground connection by introducing a densely grounded network within the resistive stage. We have developed three distinct high rate (HR) layouts featuring dense grounding schemes: the Double-Resistive Layer (DRL), the Silver-Grid (SG), and the Pattern-Etching-Plating (PEP).

2.1 The Double-Resistive layout

The DRL layout is sketched in figure 4. The first DLC film, sputtered on the back-plane of the amplification stage [8], is connected to a second DLC layer by means of a matrix of metalized vias (v1). A further matrix of vias (v2) connects the second DLC film to the underlying readout electrodes, providing the grounding of the whole resistive stage. The vias density is $\leq 1\,\mathrm{cm}^{-2}$.

2.2 The Silver-Grid layout

The Silver-Grid (SG) layout, is sketched in figure 5. The conductive grid deposited on the DLC layer acts as a high density 2-D current evacuation system. In the first prototypes the conductive grid has been screen-printed using a silver paste, from which the name of the layout. The presence of a conductive grid on the DLC can induce discharges over its surface. This effect, depending on the resistivity, requires the introduction of a small dead zone in the amplification stage above the grid lines (see figure 5). The SG layouts exhibit a geometrical acceptance lower than DRL due

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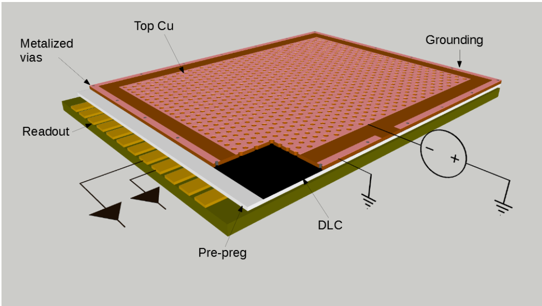

Figure 3. Sketch of the Single-Resistive layout.

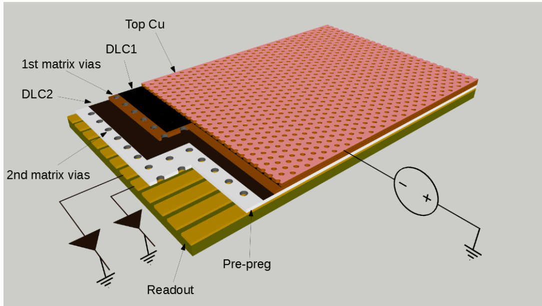

Figure 4. Sketch of the Double-Resistive layout.

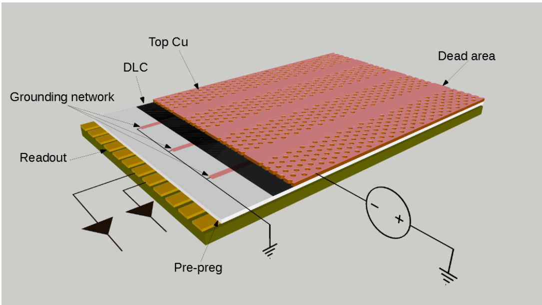

Figure 5. Sketch of the Silver-Grid layout.

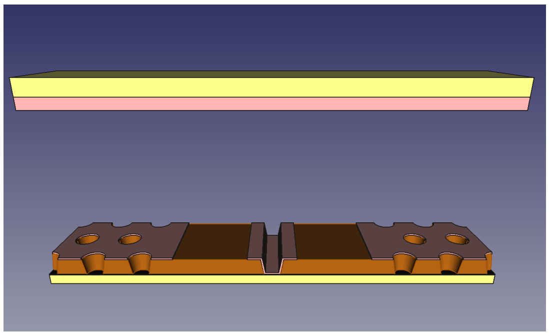

Figure 6. Sketch of the Patterning-Etching-Plating (PEP) layout.

to the presence of a dead zone. Thanks to the DLC+Cu technology, allowing the photo-etching of very thin grid lines ($\simeq$100 µm width), for the SG2++ it has been possible to reduce the dead zone down to 5% of the active area.

2.3 The Pattern-Etching-Plating layout

The Pattern-Etching-Plating (PEP) layout, figure 6, is a single DLC layer high-rate scheme recently developed. This approach aims to create a layout akin to an SG µ-RWELL without necessitating DLC+Cu technology. The ground connection is established by etching conductive grooves directly from the top copper layer of the base material through the Apical foil to reach the DLC. PEP is an acronym representing the three primary processes involved in this layout's production:

- Patterning — patterning the top copper to reveal thin Apical lines, which will form the ground connections (the central 50 µm wide zone in figure 6).
- Etching — etching the exposed Apical to create longitudinal grooves in the detector, while the remaining active area is shielded by the copper (serving as a protective mask in this phase).
- Plating — filling the groove with silver glue using screen-printing techniques, adhering to the DLC, and subsequently creating a plating between the top copper layer and the silver glue.

Post groove connection fabrication, often colloquially referred to as PEP or "PEP lines", the standard process for creating amplification holes commences. It is crucial to isolate the top copper from the PEP line, since the former is put to High Voltage (HV) while the latter is grounded. In the initial PEP version, the distance between the closed blind holes and the PEP lines was set to 750 µm, resulting in a dead zone around 80%, and a PEP layout with a dead zones less than 2–3% is planned.

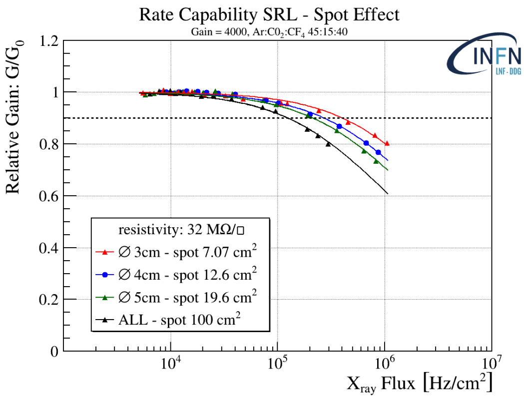

Figure 7. Normalised gain for the SRL as a function of the X-ray flux and different beam spot at a nominal gas gain of 4000.

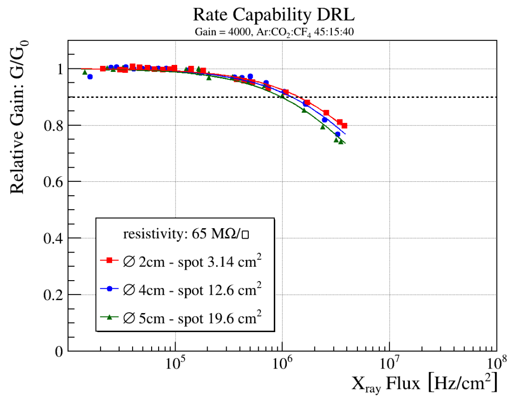

Figure 8. Normalised gain for the DRL as a function of the X-ray flux and different beam spot at a nominal gas gain of 4000.

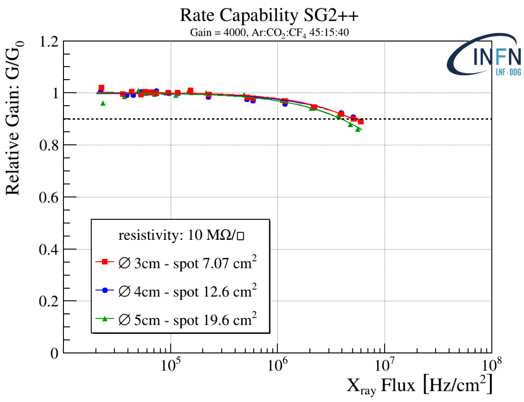

Figure 9. Normalised gain for the SG2++ as a function of the X-ray flux and different beam spot at a nominal gas gain of 4000.

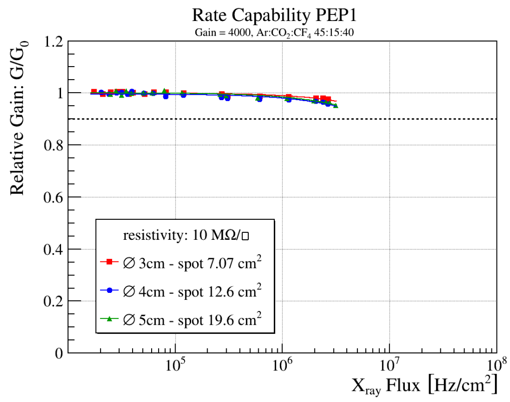

Figure 10. Normalised gain for the PEP as a function of the X-ray flux and different beam spot at a nominal gas gain of 4000.

3 Performance of the high rate layouts

The validation plan for the various layouts encompasses intensive local irradiation tests using the X-ray facility at the LNF-DDG laboratory, as well as pion/muon beam experiments at CERN H8-SpS and PSI πM1. The gain reduction due to the particle flux on the HR layouts, in relation to the beam spot size, has been examined using a high-intensity 5.9 keV X-ray tube. A series of 2 mm thick lead collimators with varying hole diameters, from 1 to 5 cm, were employed to define the X-ray spot. The detectors were equipped with a 100 μm thick Apical window, and a copper-clad Apical foil served as cathode, in order to significantly reduce the X-ray absorption. The normalized gas gain curves of the SRL and HR layouts, plotted against the X-ray flux for various X-ray spots, are depicted in figures 7, 8, 9, and 10. The measurements have been performed at a gas gain of 4000 and the detectors have been operated with Ar:CO_2:CF_4 = 45:15:40. Given that the irradiated area surpasses the basic current evacuation cell defined by the dense grounding network (table 1), the gain reduction in the HR layouts is largely invariant with respect to the spot size when X-ray fluxes exceed 1 MHz/cm^2. The observed variances

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Table 1. Geometrical parameters of the HR-layouts compared with the low rate baseline option (SRL).

Layout	ground-pitch (mm)	dead-zone (mm)	geometric acceptance (%)
SG1	6	2	66
SG2	12	1.2	90
SG2++	12	0.6	95
DRL	6	0	100
PEP	9	1.5	83
SRL	100	0	100

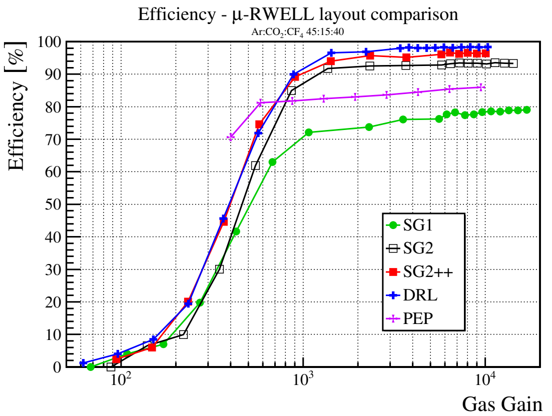

Figure 11. Efficiency as a function of the gas gain for the HR layouts.

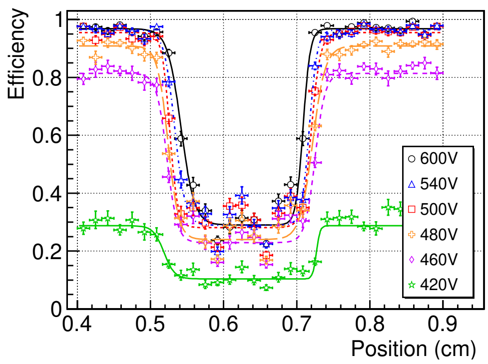

Figure 12. Zoom of the efficiency profile in the dead zone for different voltages for SG1.

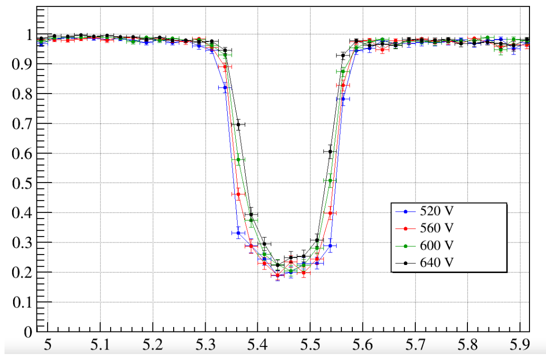

Figure 13. Zoom of the efficiency profile in the dead zone for different voltages for PEP.

in the rate capability measurements of the different layouts are primarily attributed to the varying DLC surface resistivities in each detector. In figure 11, the efficiency of the HR-layouts is reported as a function of the detector's gain. The PEP was irradiated with a 150 GeV/c pion beam at SpS, whereas the other HR layouts were tested with a 350 MeV/c low momentum pion beam at PSI. Efficiency was assessed over a fiducial area of 3×3 pads surrounding the anticipated hit location. At a gain of 5000, the DRL demonstrates an efficiency of 98%, while the optimized Silver-Grid layout (SG2++) approaches a maximum efficiency of about 97%. As anticipated, the inclusion of larger dead zones in the active area for SG1, SG2, and PEP layouts results in detection efficiencies of 78%, 95%, and 85% respectively, which exceed their geometrical acceptance. An efficiency larger than the geometrical acceptance, characteristic of detectors with GEM-like amplification stages [9, 10], is observed in areas corresponding to the dead zones. The wells proximate to these dead zones also gather the primary ionization produced above the inefficient regions, a phenomenon known as the "focusing effect", which aids in recuperating detection efficiency. Concurrently, amplification within these wells is likely enhanced due to the concentration of drift field lines. Additionally, as depicted in figures 12 and 13, enhancing the High Voltage (HV) applied to the amplification stage leads to improved efficiency within the dead zones.

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4 μ-RWELL in High Energy Physics

4.1 μ-RWELL for high rate enviroment

The μ-RWELL technology is proposed for the realization of the innermost regions of the muon detection system for the phase-II upgrade of the LHCb experiment at the High Luminosity Large Hadron Collider (HL-LHC). The detector is scheduled for installation during the Long Shutdown 4 of the LHC (LS4) and is expected to commence data acquisition in Run 5, projected for 2032.

As indicated in table 2, the regions R1 and R2 are predicted to encounter maximum input rates ranging from several tens of kHz/cm^2 to nearly 1 MHz/cm^2. To accommodate these demanding conditions, new detectors with a rate capability of a few MHz/cm^2 are needed. Approximately 600 detectors of various sizes, ranging from 30×25 to 74×31 cm^2 and corresponding to an area of approximately 130 m^2 of Diamond-Like-Carbon (DLC) sputtered on Apical foils, are planned for instrumentation in these regions. In this context, a DC Magnetron sputtering machine (jointly funded with the CERN MPT workshop) for DLC deposition on Apical foils has been recently acquired and is currently undergoing a testing phase.

Table 2. Maximum input rate expected at 1.5×10^{34} cm^{-2} s^{-1} and total instrumented area for each station and region of the muon detector.

Rates (kHz/cm^2)	M2	M3	M4	M5
R1	749	431	158	134
R2	74	54	23	15
R3	10	6	4	3
R4	8	2	2	2

Area (m^2)	M2	M3	M4	M5
R1	0.9	1.0	1.2	1.4
R2	3.6	4.2	4.9	5.5
R3	14.4	16.8	19.3	22.2
R4	57.6	67.4	77.4	88.7

4.2 μ-RWELL for tracking apparatus

4.2.1 Future experiment at future accelerator

The μ-RWELL is currently being explored for its potential application in the IDEA (Innovative Detector for Electron-Positron Accelerators) project at future circular electron-positron colliders, particularly for its tracking capabilities, in two subsystems: the pre-shower and the muon system. A primary objective of the IDEA collaboration is to fabricate a substantial volume of μ-RWELL_PCB (of the order of 1000 m^2), while maintaining cost-effectiveness. Despite the significant scale, the devices are required to ensure excellent spatial resolution and cost-efficiency. In this context, the μ-RWELL technology emerges as a promising candidate, especially considering the ongoing endeavours to transfer its manufacturing technology to industry (section 5). The outcomes of a preliminary study, examining the dependency of cluster size and spatial resolution on varying Diamond-Like-Carbon (DLC) resistivities, are illustrated in figure 14 and figure 15, respectively.

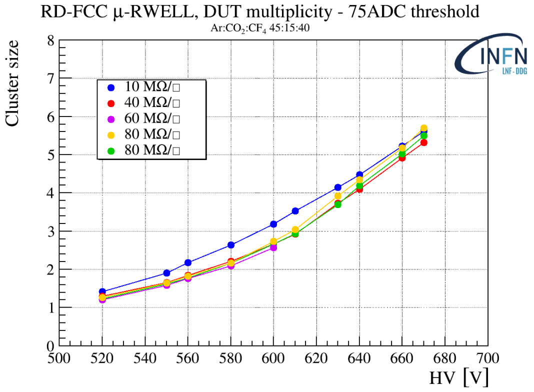

Figure 14. Strip cluster size as a function of the HV.

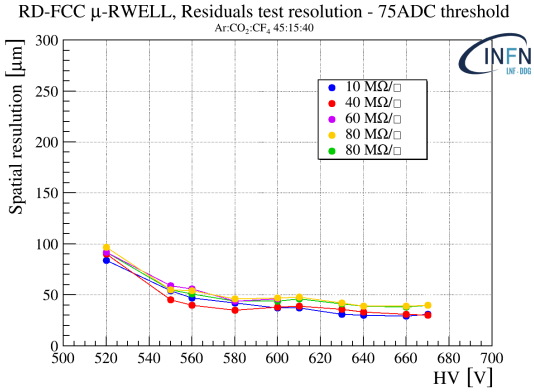

Figure 15. Residuals as a function of the HV.

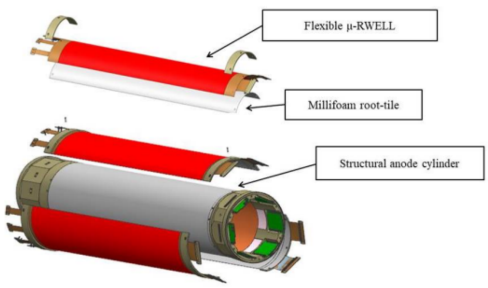

Figure 16. Sketch of the assembly of the three roof-tile detectors on the anode cylinder.

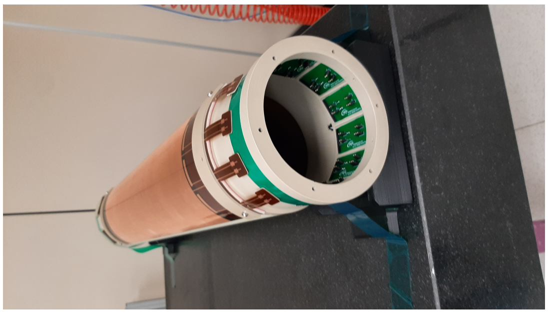

Figure 17. The C-RWELL anode with the first µ-RWELL tile assembled.

4.2.2 Inner trackers for Super-Charm-Tau-Factories

The concept of a cylindrical µ-RWELL (C-RWELL) as a low mass Inner Tracker (IT) has been developed within the research and development efforts for future high luminosity electron-positron colliders with a centre of mass energy around 10 GeV (Super-Charm-Tau-Factories — SCTF), with the requirement of minimizing the multiple scattering effects of outgoing particles, reducing systematic errors in the vertex reconstruction. The unique capability to integrate the amplification stage, the resistive layer, and the readout board into a single flexible element renders the µ-RWELL technology apt for non-planar geometries. The detector is designed modularly: the cylindrical µ-RWELL_PCB is segmented into three "roof tile" detectors (figure 16). These tiles can be removed and replaced if necessary, thanks to the capability of opening (and re-closing) the cylindrical support. The first roof tile has been successfully mounted onto the structure as a preliminary trial for the ultimate assembly procedure (see figure 17). Following the completion of the detector, a cosmic ray test utilizing APV25 Front-End Electronics (FEE) is planned.

5 The technology transfer

To instrument the large area required by the Muon-LHCb upgrade, establishing a partnership with the industry is essential. Therefore the technology transfer of the µ-RWELL constitutes one of the project's critical milestones. Currently, the production of the µ-RWELL is centralized at the CERN-EP-DT-MPT

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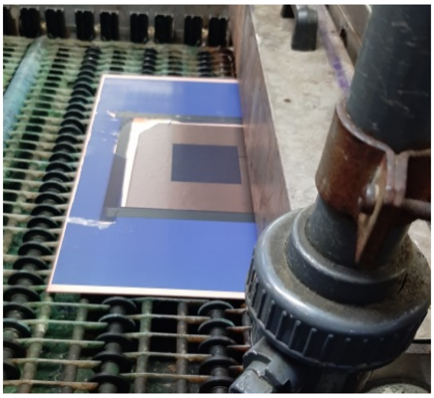

Figure 18. Brushing machine for DLC patterning.

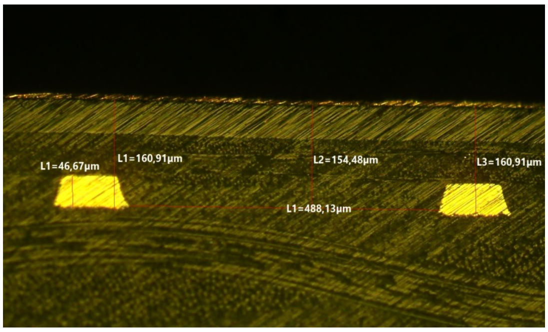

Figure 19. The cross section of DLC foil glued on PCB.

Workshop.[2] Within the scope of the AIDA-Innova project,[3] µ-RWELL prototypes are envisioned to be co-produced partially by industrial partners and completed at CERN under the supervision of the LNF-INFN research team. In the initial phase, the R&D process follows a straightforward loop: the detector layout is conceptualized at LNF, the prototype (with its PCB manufactured by industry) is assembled by CERN, and the LNF research team conducts the prototype's validation and, if necessary, implements adjustments to the design. With each successful completion of this loop, the industrial partner's task, in this case ELTOS S.p.A.,[4] involves selecting and fine-tuning manufacturing processes compatible with standard industrial techniques. A pivotal milestone in the industrialization of detector manufacturing was the recent acquisition of the DLC magnetron sputtering machine. With this machine, installed at the CERN-EP-DT-MPT Workshop and operational since the summer of 2023, the goal is to produce large sample of DLC-Apical-Copper foil during 2024. Within this framework, the collaborative manufacturing of the detector can be outlined as follows:

- DLC is sputtered onto the bare side of the Apical foil (opposite the 5 µm copper layer) using the CERN-INFN sputtering machine at CERN.
- The PCB readout for the µ-RWELL is manufactured by ELTOS. The precise copper patterning of the PCB is crucial for ensuring alignment in subsequent steps.
- The DLC-coated side of the DLC-Apical-Cu foil produced at CERN must be patterned to delineate the active area and prevent potential short circuits with other PCB layers. This process involves the use of photo-resist and patterning with a brushing machine (figure 18).
- The subsequent step involves adhering the DLC foil to the PCB using a single layer of 106-prepreg (approximately 50 µm thick) (as depicted in figure 19).
- Copper patterning followed by Apical etching of the through-vias (specific to the Pattern-Etching-Plating µ-RWELL) is performed, concluding with their final plating for DLC grounding. While CERN handles these tasks, ELTOS could potentially undertake the copper etching.
- The amplification stage is patterned by etching the matrix of holes in Apical, a process exclusively performed by CERN, which possesses the necessary technological expertise.

Currently, the trials conducted at ELTOS have primarily focused on three of the aforementioned stages: patterning of the DLC, planarizing of the PCB, and the adhesion of the DLC foil to the PCB. Until

[2] Advancement and Innovation for Detectors at Accelerators — CERN-EP-DT-MPT Workshop website.
[3] EU-funded AIDAinnova project.
[4] Eltos website.

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now, the tests at ELTOS have been focused on three of the above mentioned manufacturing steps: the DLC patterning, the PCB planarizing and the gluing of the DLC foil onto the PCB.

6 Conclusions

In this paper, we have explored various resistive layouts of the µ-RWELL suitable for high rate applications. The rate capability and performance of these prototypes have been rigorously validated using a 5.9 keV X-ray gun and pion/muon beams at CERN and PSI. The layouts proposed here present diverse solutions that meet the stringent requirements for detectors envisaged for the phase-2 upgrades of the muon apparatus at the High Luminosity Large Hadron Collider (HL-LHC), as well as for use in the future accelerators FCC-ee/hh and CepC. The feasibility of fabricating the detector on flexible substrates paves the way for its application in non-planar geometries, such as the instrumentation of the Inner Tracker in future Charm-Tau factories. A rate capability exceeding 1 MHz/cm^2 coupled with a detection efficiency ranging between 97 to 98% are among the notable achievements of the technologies discussed. Furthermore, it is important to highlight that the PEP layout, particularly with its optimization, can be produced using full sequential-build-up technology. This advancement facilitates the transfer of the manufacturing process to industrial production, marking a pivotal step in the broader application of this technology.

Acknowledgments

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