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A simulation methodology for establishing IR-drop-induced clock jitter for high precision timing ASICs

Gianmario Bergamin[a,*] **and Alexandre Pierre Soulier**[b]

[a] *CERN,*
Esplanade des Particules 1, 1211 Geneva, Switzerland
[b] *Laboratoire de Physique de Clermont, IN2P3,*
Campus Universitaire des Cézeaux, 4 Avenue Blaise Pascal, 63178 Aubière Cedex, France

E-mail: gianmario.bergamin@cern.ch

Abstract: The combination of 3D tracking and high-precision timing measurements has been identified by the European Committee for Future Accelerators as a fundamental requirement to increase detection capabilities for future applications. Among others, on-chip high-quality clock is a key factor determining the overall resolution of timing ASICs. However, in large and dense chips, power-grid drops can severely affect the non-deterministic jitter of the clock, representing a limit to the performances. This contribution presents a simulation framework based on commercial tools to derive power supply-induced jitter, providing a pre-silicon methodology to assess its impact to timing indeterminism. The flow is presented together with practical examples and results.

Keywords: Pixelated detectors and associated VLSI electronics; Timing detectors; Digital electronic circuits

*Corresponding author.

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1 Introduction

The European Committee for Future Accelerators (ECFA) has identified high-precision timing measurement as a critical research area for future accelerators. To address the challenges posed by increased luminosity and large particle track pile-up, the use of "4D techniques", which involves 3D tracking and Time of Arrival (TOA) evaluation, is essential for improving vertex location in future High-Energy particle detectors. High-performance sampling and high-precision timing distribution are crucial figures of merit to be considered when dealing with ps-level resolutions [1].

A commonly used approach for TOA measurement is the TDC-based chain, where a Time To Digital Converter (TDC) converts the time elapsed between the arrival of the hit and an internal clock reference signal. Its timing resolution can be expressed as $\sigma^2_{\text{toa}} = \sigma^2_{\text{FE}} + \sigma^2_{\text{TDC}} + \sigma^2_{\text{clk}}$, where the first term includes the contribution of the analog front-end, the second directly depends on the bin size of the TDC and the last represents the clock jitter [2]. The continuous scaling and integration of VLSI technology pose a severe limitation to the quality of the clock in modern ASICs due to the phenomenon of power supply-induced jitter [3]. The dynamic IR drop generated by the running logic reflects into increased cell delay, degraded transition time and increased jitter for the standard cells, thus increasing the uncertainty of the clock reference. Large pixel arrays may be especially susceptible to this issue, as they often contend with limited access to power and ground routing resources, leading to notable power fluctuations.

The literature [3] already presents various modeling approaches for the phenomenon, but, as they are all based on theoretical or analytical methods, they are hardly applicable during the design of complex ASICs. A simulation-based methodology exploiting commercial tools has been therefore developed and applied, for the first time in the field of High Energy Physics, to correlate the digital activity of the ASIC with the induced clock jitter, providing a pre-silicon methodology for assessing its impact on the timing performances of the ASIC.

2 Flow description

The proposed flow fully relies on commercial Cadence EDA tools and allows deriving the IR-drop-induced jitter within a Digital-On-Top implementation approach. Figure 1 reports the required steps and tools.

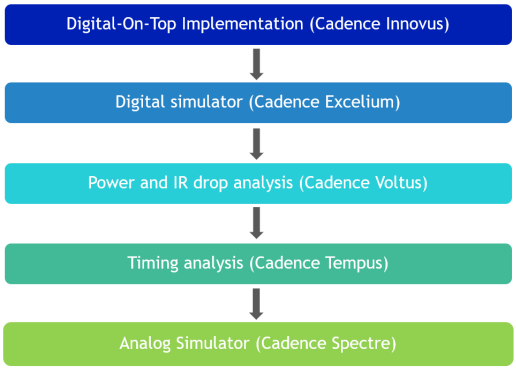

Figure 1. Flow steps.

First, the digital-on-top design implemented in Innovus is simulated with digital tools and realistic stimuli. The extracted activity information is then used to perform dynamic power and IR drop analysis, where the Effective Instance Voltage (EIV), calculated as the difference between the supply and ground seen by the clock buffers, is derived and recorded at every simulaton cycle. Analog simulations are then performed to simulate the extracted clock network together with the EIV values annotated per each cell, allowing to derive the real arrival time of the clock to all the sinks for every cycle. Finally, the IR-drop-induced jitter contribution can be calculated identifying the two cycles with maximum difference in clock arrival time.

Digital-On-Top implementation. Digital-On-Top (DOT) Synthesis and Place&Route is the fundamental starting point of the flow. The full chip is assembled in Cadence Innovus where each analog macro block is characterized with the corresponding liberty file and abstract. Full chip gate-level netlist and SDF (Standard Delay File) containing internal ASIC delays are derived and imported into a digital simulation environment.

Digital simulation. The goal of this step is to emulate the real application of the ASIC, providing realistic stimuli and configurations and checking the correctness of the outputs. Gate-level netlist is annotated with SDF per corner and detailed Verilog models are used to represent the behavior of analog macros within the DOT simulation. Value Change Dump (VCD) files are generated to obtain cycle-accurate instance-based activity information.

Dynamic power and IR drop analysis. DOT design is imported in Cadence Voltus to perform Dynamic power and IR drop analysis. Power Grid Views (PGV) are needed to accurately capture current and capacitance distribution inside digital standard cells and analog macros [4]. Based on input VCD file and cell liberty file power information, a dynamic current profile is extracted by the dynamic power analysis engine for every cell in the design, reporting the current consumption in each simulation cycle. Dynamic IR drop analysis extracts the capacitance and resistance of the ASIC power grid and applies the above-mentioned current waveforms, extracting dynamic voltage drop for power and ground nets in the design. The realistic power supply values (EIV) seen by the cells in the design in each simulation cycle, at the exact moment of their switching, are exported into EIV files. Figure 2 reports the output of this last step, namely the generated current and voltage profile for a buffer switching at 40 MHz. The EIV considered in the Voltus analysis is the mean voltage seen by the buffer in the window where the current profile shows a dynamic consumption.

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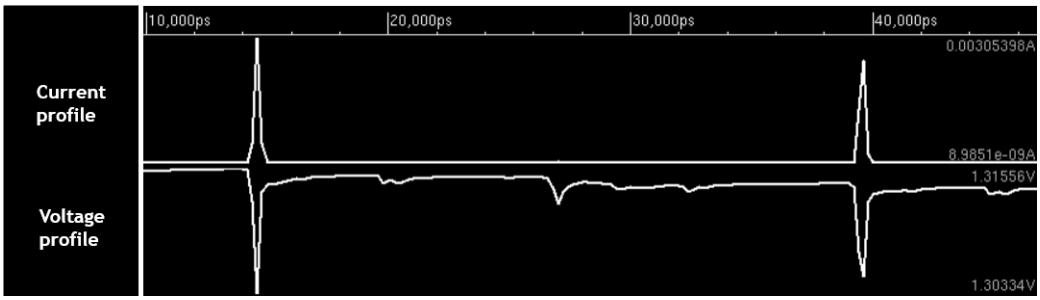

Figure 2. Example of dynamic power result (top) and corresponding dynamic IR drop (bottom) for a single buffer. The EIV is calculated as the average of the dynamic IR drop in the window where the total current differs from the leakage one.

Timing analysis. Cadence Tempus addresses the gap between Digital-On-Top implementation and analog simulations needed for accurately measuring clock path delays. Tempus is provided with the full chip DOT design and with EIV files, and automatically exports the path to be analyzed (in this case the clock tree paths, from the clock source to the endpoints) to the analog simulator (Cadence Spectre) via a Spice netlist.

Analog simulation. One analog simulation is launched per each simulation cycle, where each element in the clock path under analysis is annotated with its realistic power supply, derived from EIV files. Design parasitics are directly ported from Innovus (through a Standard Parasitics Exchange File) into the Spice netlist. Finally, the realistic arrival time of the clock, including the IR drop effect, is derived by measuring rising and falling delays through cells and nets of the path under study. Considering the scenario of figure 3, the Peak-To-Peak jitter can be calculated as:

$$\text{jitter}_{\text{peak-to-peak}} = \text{Max}(t\_0, t\_1, \ldots, t\_N) - \text{Min}(t\_0, t\_1, \ldots, t\_N)$$

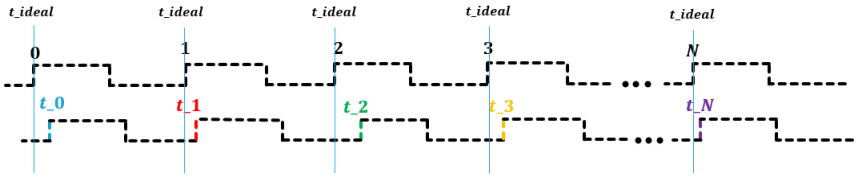

Figure 3. Realistic clock arrival time including IR-drop effect.

3 Altiroc case study

The proposed flow was tested and debugged during the Altiroc [5] design phase. The ASIC is composed of 225 pixels over a total area of 2×2 cm^2, and performs Time Of Arrival and Time Over Threshold measurements using the above-mentioned TDC chain. The increasing IR drop over the pixel matrix (figure 4) poses severe concerns about the measurement clock quality, which is generated in the periphery and spans the full ASIC. The varying digital activity inside the chip and the corresponding IR-drop-induced jitter can be therefore a significant limitation for the overall timing performances of the chip. In this sense, this scenario is a perfect test case for the presented analysis. A UVM (Universal

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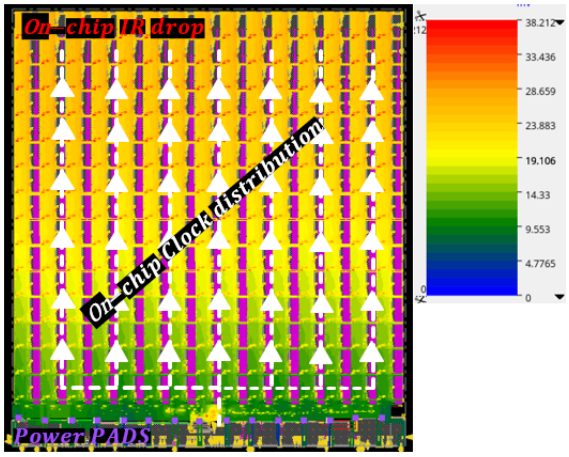

Figure 4. Dynamic IR drop in *mV* for Altiroc3 ASIC (background) and schematic representation of measurement clock (foreground).

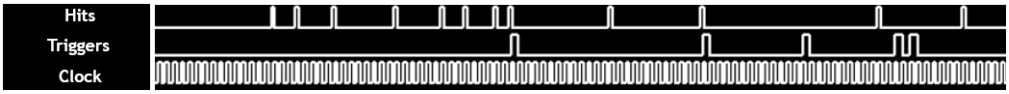

Figure 5. Waveforms of simulation scenario.

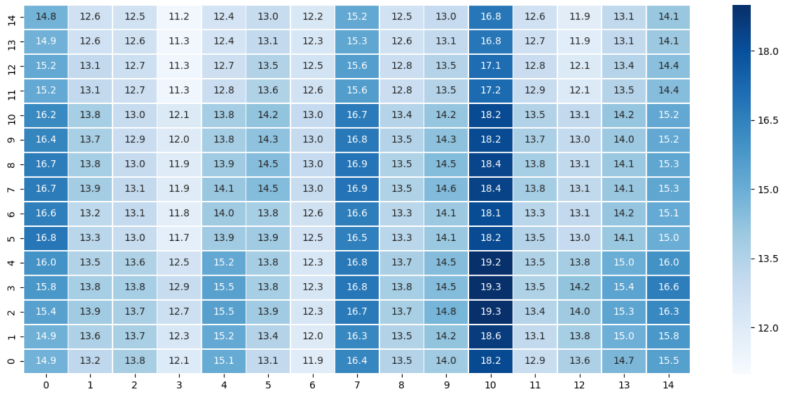

Figure 6. Peak-To-Peak Jitter in *ps* for 225 pixels of Altiroc.

Verification Methodology) environment has been used to simulate the DOT-implemented design for VCD extraction. As shown in figure 5, the ASIC is initially set in an "IDLE" state with no input activity (no impinging hits nor L1 triggers are sent for readout). In the second part of the simulation, the chip is instead provided with realistic input stimuli according to physics events, emulating its realistic behavior in the experiment and checking the correctness of the output data. Following the steps reported in section 2, the realistic delay (including the IR-drop induced degradation in the ASIC distribution) of each clock rising edge in figure 5, is then derived for all 225 pixels in typical corner (1.2 V). The Peak-To-Peak jitter, computed as the difference between the maximum delay and the minimum delay among all clock rising edges in simulation, is reported in figure 6 in *ps*. To compare the effect of the digital activity induced by injected hits and triggers, the same analysis was repeated on the restricted simulation period where no input stimuli were present, resulting in a much more

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stable power supply and reduced Peak-To-Peak jitter, which resulted to be limited below 1 ps. With the presented methodology it was possible to further investigate the origin of the jitter, identifying its main sources and contributions. Figure 7 reports the analysis of the IR-drop-induced clock jitter for a clock path to a certain pixel *N* in the matrix. On the left side the maximum difference in EIV over all simulation cycles is reported for every cell composing the clock path. On the right, the total clock jitter of pixel *N* is broken down into each cell contribution and it is reported together with the cumulated jitter. Not surprisingly, the digital standard-cells placed in the ASIC pixel matrix (highlighted in green in the picture), far from the voltage source PADs, show a larger difference in EIV with varying on-chip digital activity with respect to cells placed in the chip periphery (in red). The difference in power-supply-induced jitter for different types of standard cells can be also derived from 7.

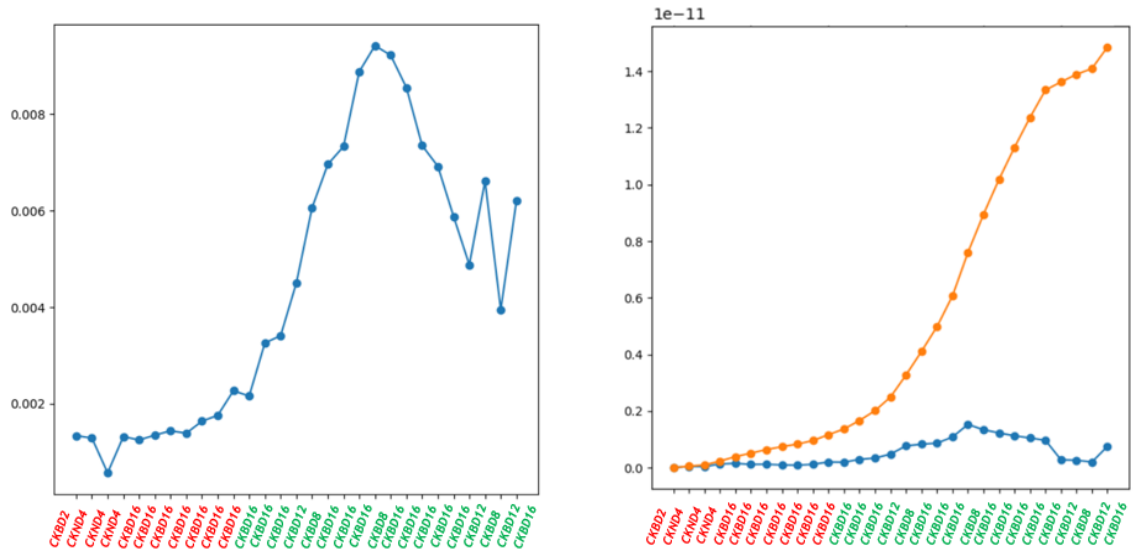

Figure 7. Jitter study for pixel N. Difference in EIV on the left in *V*, corresponding clock jitter contribution (blue) and total cumulated jitter (orange) on the right, in *s*. Instances in red are located in the periphery while instances in green are located in pixel matrix.

4 Conclusions

The presented simulation methodology, fully embedded within commercial Cadence EDA tools, provides the designer with a unique way to assess, before tapeout, the IR-drop-induced clock jitter for a Digital-On-Top implemented design. Different simulation scenarios and ASIC configurations can be explored and debugged, and the level of detail that can be reached allows for pre-silicon optimizations on floorplan and power grids. Power-supply-induced jitter analysis will be a fundamental signoff check for ps-resolution timing ASICs in the field of High Energy Physics.

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