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Digital processing and BLMASIC control prototype for the Beam Loss Monitor system in the SPS at CERN

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Abstract: The Beam Loss Monitoring system plays a crucial role in the CERN's Super Proton Synchrotron beam monitoring and machine protection. With the upcoming renovation of the system, the acquisition electronics can be based on an innovative ASIC designed by CERN. This paper presents the development of the control and digital processing electronics for this BLMASIC, reviews the architecture and design choices, discusses implementation details, including the controls and redundancy schemes, and highlights some preliminary results. The conclusion outlines the future development steps, and emphasises the interest of this simple and robust architecture using LpGBT and VTRx for critical systems.

Keywords: Beam-line instrumentation (beam position and profile monitors, beam-intensity monitors, bunch length monitors); Digital signal processing (DSP); Hardware and accelerator control systems; Radiation-hard electronics

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Contents

1 Introduction

The SPS is a versatile accelerator at CERN supporting a wide range of experiments, and a crucial component in the High-Luminosity LHC (HL-LHC) project. Its safe and reliable operation is essential for both experimental success and the protection of equipment. Its Beam Loss Monitor (BLM) system is a key element to protect the accelerator from damage by measuring beam losses. This study outlines the design and implementation of a prototype dedicated to the processing electronics and to the control of the acquisition. This development is undertaken in preparation for the modernisation of the BLM system within the SPS during the Long Shutdown 3 (LS3).

The current BLM system in the SPS, dating from the 1990s, employs around 410 Ionisation Chambers (IC) and 17 VME crates on the surface. The beam dump is triggered with millisecond latency by hardware comparators or software running-sums. After several decades of successful operation, as spare components become scarce, a complete renovation is planned for LS3. This upgraded electronics will also serve the LHC after LS4. It will include enhancements such as reduced beam dump request latency, 1 kGy radiation tolerance, 8-order magnitude input dynamic range, 10 µs acquisition period, and versatile real-time digital processing.

Figure 1 illustrates the anticipated architecture of the new SPS BLM system, which consists of about 450 new detectors covering all the critical loss locations around the ring, injection and extraction lines. Those ICs are cylindrical tubes filled with N2 and hosting electrodes polarised at 1.5 kV. They collect the charges generated by the passage of secondary particles created by protons lost from the beams [1]. The electrical current generated is acquired by a radiation-tolerant front-end crate (BLEACT) [2] situated in the accelerator tunnel area acquiring up to 8 input channels through coaxial cables. Measurements are digitised and optically transmitted every 10 µs. The Wiener VME64x back-end processing crate located at the surface contains up to 16 renovated Threshold Comparator (BLETC) based on a CERN standard VFC-HD platform which processes 16 channels each. Each channel value is integrated on 12 time windows ranging from 10 µs to 24 s, requesting a beam dump if they exceed predefined thresholds.

2024 JINST 19 C02052

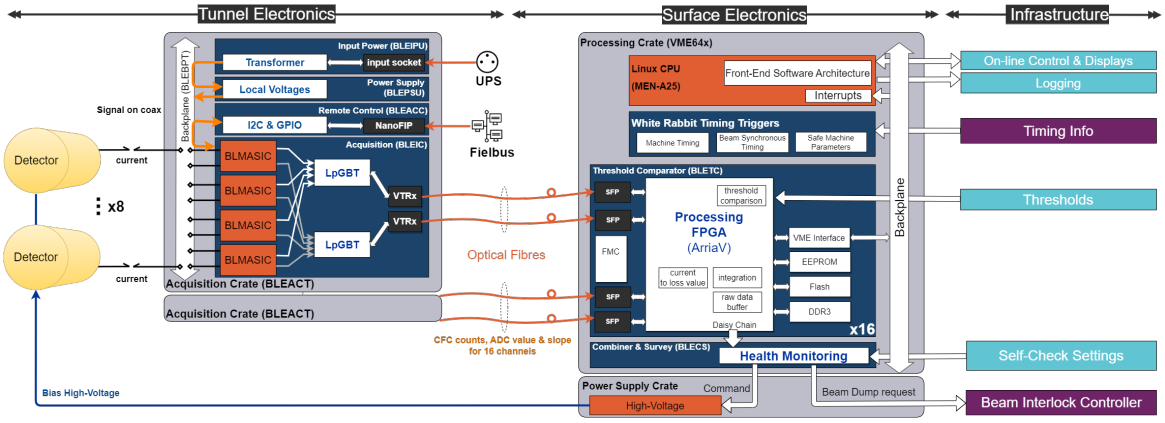

Figure 1. Projected Post-LS3 BLM System Architecture in the SPS.

As the system is subject to severe dependability constraints (<10^{-7} failure per hour) in a harsh environment, radiation mitigation techniques, rad-hard components, error correction and redundancy are used. For example, a redundant optical link is used to transmit measurements to the surface, as in the LHC BLM system [3], but operates in full-duplex mode, as in the BLM system [4] for the LHC injector chain, enabling remote control and configuration upstream.

2 BLM ASIC overview

The heart of this future BLM system's acquisition electronics, illustrated in figure 2, is planned to be the BLM Application Specific Integrated Circuit (BLMASIC), developed in cooperation with the EP-ESE Group at CERN. This specialized chip can withstand HL-LHC radiation doses of up to 500 kGy. This resilience allows positioning the electronics closer to the beam, reducing interference picked up by cables. Utilizing a Current to Frequency Converter (CFC) along with a Wilkinson ADC, this ASIC offers a sampling period of 10 µs. Results can then be propagated by redundant interfaces exploiting the Low Power Gigabit Transceiver (LpGBT) [5] serializer.

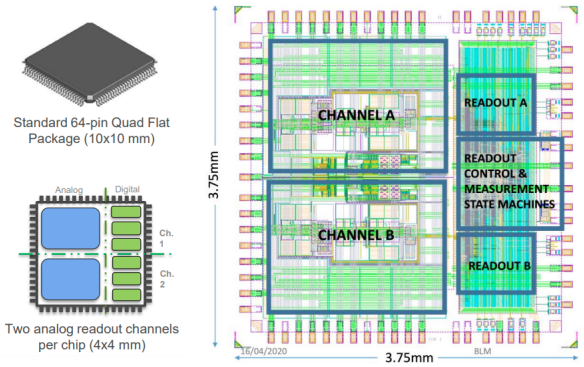

Figure 2. Overview of the BLMASIC chip layout.

To ensure the BLM reliability, a rigorous characterization [6] and validation [7] of this ASIC were carried out, including irradiation tests. They show that measurement performance is within specifications: a resolution of 1.5 pA for slow varying currents; an error <10% in the range of [60.1 µA; 1 mA] at the maximum sampling rate; and a deviation below 0.5% at 3 kGy TID [8].

2024 JINST 19 C02052

3 Acquisition electronics

To facilitate the LHC system upgrade in LS4, the new BLM SPS acquisition board (BLEIC), shown in figure 3, was made compatible with the BLECF board [9] currently used in the LHC.

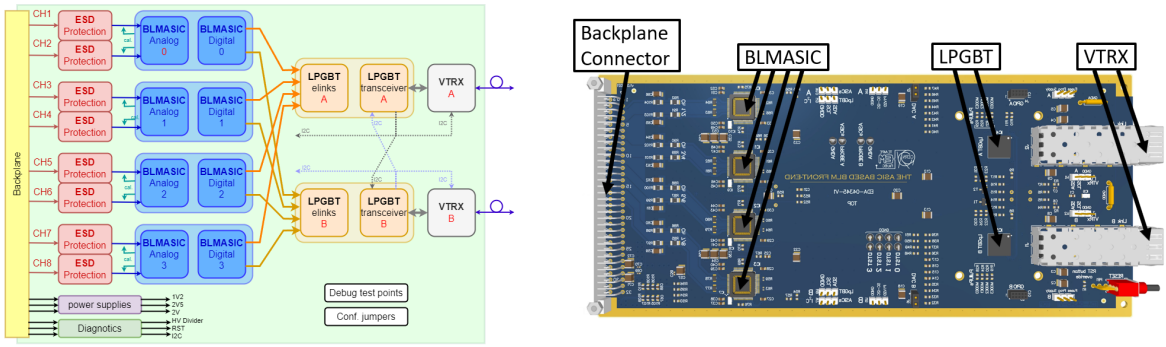

Figure 3. Architecture and Top View of the Acquisition Board (BLEIC).

Each input current channel provides an ESD protection and one calibration DAC located in the BLMASIC. One ASIC can sample 2 inputs and send the digital values at a rate of 80 MHz to both LpGBTs, which oversample the data at 320 MHz and transmit the packetised data by means of optical VTRx [10] transceivers. To achieve full remote control and monitoring, all components feature a local configuration I2C bus driven by the LpGBT, as master.

4 Processing electronics

The control and processing electronics is based on the standard VME board (VFC-HD) [11]. The embedded firmware remotely configures the acquisition front end via the optical link without the need for any CPU-oriented software.

The prototype's preliminary digital processing includes loss integration by running-sums over different timespan, threshold comparison and maximum values logging at 1 Hz. A typical configuration involves 12 running-sums of 64 bits with time windows from 10 µs to 24 s. This parameterized module will allow for tuning of settings by the SPS operators later in the development. Several other operational functions will be added, such as a raw data buffer called 'capture', and timing triggers to discriminate between losses when the beam is present or not.

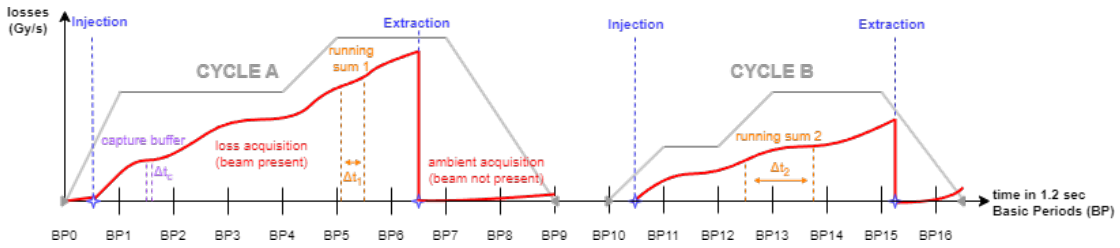

Figure 4. Example of Beam Loss Measurement over 2 SPS Cycles.

Figure 4 gives an example of the expected SPS BLM measurements. Beam losses are integrated from injection into several running-sums, and the capture buffer is filled on demand. The ambient background is measured when no beam is present. All measurements are logged only at cycle-end but are continuously compared to hardware thresholds to trigger a beam dump in real-time.

2024 JINST 19 C02052

Figure 5 shows the ArriaV FPGA architecture of the prototype implementation the reception of 2 redundant pairs of optical links and the data processing of 16 channels in 12 running-sums.

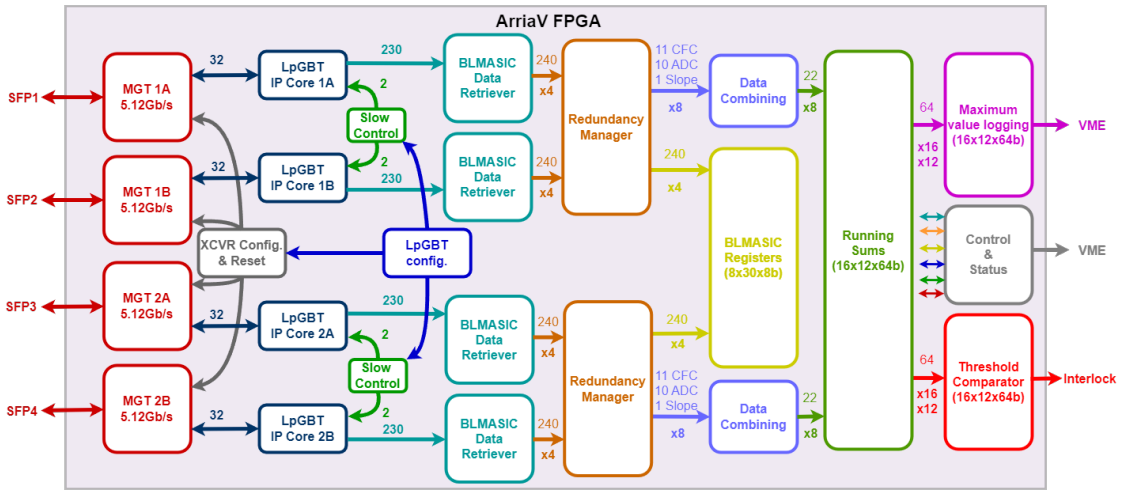

Figure 5. VFC-HD Back-end Processing Architecture.

The 5.20 Gpbs transceivers connect to the LpGBT uplink and downlink modules running at 160 MHz. A custom word aligner was used as the LpGBT example design is provided for Xilinx FPGAs only. The transmission PLL, configuration and reset of the 4 transceivers are shared. The BLMASIC data is decoded and the 3 measured values (CFC counts, Wilkinson ADC & slope) are retrieved and combined to get a 22-bit value per channel. Then the 192 (12×16) running sums of 64 bits are processed more slowly at 100 MHz to manage the FPGA timing closure. A monitoring module checks the reception quality to select the optimal link using the number of transmission errors detected and corrected, and can remotely reconfigure the front end in case of link failure.

A preliminary resource estimation shows that the data reception utilizes 15% of the FPGA logic. Meanwhile, the processing module accounts for around 10%, with plans to better meet the operator's requirements and add new features by using more BRAM and external memory. The 100 MHz operating frequency allows all channels to be processed in parallel in less than 10 µs. The total FPGA ALM's 26% occupancy is in line with expectations, leaving room for future additions.

5 Prototype testing

To quickly create a functional prototype, the approach centred only on data reception, processing and acquisition control. The development focused on the digital processing board within a 6U ELMA VME crate.

The first step was the development of an I2C link on the VFC-HD using a standard General Purpose Input/Output (GPIO) FPGA Mezzanine Card (FMC) to control the Integrated Circuit (BLEIC) board and its main components: BLMASIC, LpGBT and Versatile Transceiver (VTRx). The protocol and interface were implemented directly in the gateware, so the sequence of commands could be sent either on the VME bus by software (SW) or from an internal Read-Only Memory (ROM). Since the design provides access to a vast number of monitoring registers (100+ per reception line), such as error counters and synchronization flags, an automated tool was employed for generating FPGA registers, simulation testbench constants, and drivers. This approach ensures that the gateware interface remains always

2024 JINST 19 C02052

synchronized with the deployed software. Additionally, as no FrontEnd Software Architecture (FESA) class was yet available for this prototype, a highly beneficial Python GUI facilitated a rapid debugging.

This prototype was tested in the laboratory with optical attenuators to test the data transmission and current sources to emulate losses measured by IC. A temperature test of the entire system is also planned. To provide further analysis, more tests with cables several hundred meters long and real IC monitors will be carried out in SPS in 2024. For instance, it will help determine if a per-monitor calibration is needed, get statistics on the ADC range and assess optimum refresh rates. Figure 6 shows an example of real-time loss acquisition and optical link status with EDGEGUI, together with the complete laboratory setup. One can see the 6U ELMA processing crate and the acquisition crate integrated into a single flight-case to ease installation and portability. A NUC computer is also present in the box to locally save the raw data via UDP, and read it out through Wi-Fi. A second front-end crate was added to test the post-LS4 LHC configuration using 16 channels and 4 optical links.

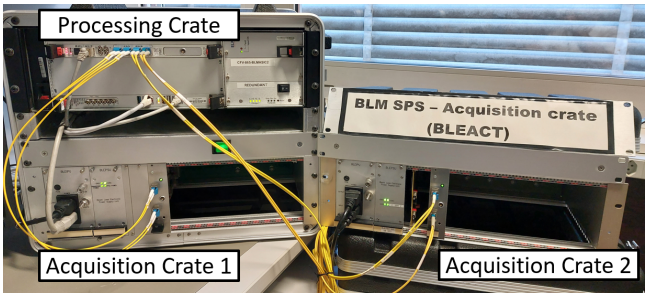

Figure 6. View of the Prototype Setup in the Laboratory.

6 Future developments

To further improve performance in terms of beam dump latency and data available to operators, the next development steps will involve extending the length of raw data buffers and running sums by using DDR3 memory instead of the small internal BRAMs, and increasing the refresh rate for long integrals by removing the cascaded shift registers and keeping just a single one. Next, SPS tests, using real monitors and beam, will enable the input channels to be calibrated and the ADC range to be optimized, in order to limit the impact of the operational environment noise.

The new and old systems will first operate in parallel after the LS3, enabling performance comparisons to be made while ensuring SPS availability. The BLM system's efficient self-diagnostic capability will facilitate preventive maintenance over its expected 20-year service life, given that the number of newly installed units will be around 450 ICs, connected to more than 50 tunnel front-ends, and 50 processing boards placed in 17 surface crates.

7 Conclusion

This paper presented the development of control and processing electronics for the future BLM system in SPS. A prototype front-end was built exploiting the BLMASIC as proof of concept of the foreseen architecture and to test performance in real working conditions. Tests of the overall data flow and processing chain, including LpGBT, VTRx and VFC-HD, have so far reported a reliable and deterministic behaviour, which is suitable for the integration in critical systems at CERN.

2024 JINST 19 C02052

References

[1] B. Dehning et al., *LHC Beam Loss Detector Design: Simulations and Measurements*, in the proceedings of the *2007 IEEE Particle Accelerator Conference (PAC)*, Albuquerque, NM, U.S.A. (2007), p. 4198–4200 [DOI:10.1109/PAC.2007.4439981].

[2] W. Viganò, *Beam Loss Electronic Tunnel Acquisition Crate Engineering Specification*, CERN EDMS (2023), https://edms.cern.ch/document/2996851/1.

[3] M. Saccani, E. Effinger, W. Viganò and C. Zamantzas, *The Beam Loss Monitoring System after LHC Long Shutdown 2 at CERN*, *JACoW* **IBIC2022** (2022) 220.

[4] M. Saccani, E. Calvo Giraldo, W. Viganò and C. Zamantzas, *The Beam Loss Monitoring System after LHC Injectors Upgrade at CERN*, *JACoW* **IBIC2021** (2021) 285.

[5] P. Rodrigues Simoes Moreira, *The LpGBT Project, Status and Overview*, in the proceedings of the *ACES 2016 — Fifth Common ATLAS CMS Electronics Workshop for LHC Upgrades*, CERN, Geneva, Switzerland (2016), https://cds.cern.ch/record/2137809.

[6] F. Martina et al., *Methodology, Characterisation and Results from the Prototype Beam Loss Monitoring ASIC at CERN*, *JACoW* **IBIC2021** (2021) 294.

[7] F. Martina et al., *Testbed Development for the Characterisation of an ASIC for Beam Loss Measurement Systems*, in the proceedings of the *9th International Beam Instrumentation Conference*, Santos, Brazil, 14–18 September 2020, p. THPP04 [DOI:10.18429/JACoW-IBIC2020-THPP04].

[8] F. Martina, *Radiation Tolerant Acquisition System for Beam Loss Monitoring at High Luminosity — LHC*, Ph.D. Thesis, Department of Electrical Engineering and Electronics, University of Liverpool, 9 Brownlow Hill, Liverpool, United Kingdom (2022).

[9] E. Effinger et al., *Single gain radiation tolerant LHC beam loss acquisition card*, in the proceedings of the *8th European Workshop on Beam Diagnostics and Instrumentation for Particle Accelerators (DIPAC 2007)*, Venice, Italy, 20–23 May 2007, p. 319–321.

[10] C. Scarcella et al., *Next generation of Radiation Tolerant Single-Mode Optical Links for Accelerator Instrumentation*, *PoS* **TWEPP2018** (2019) 151.

[11] A. Boccardi et al., *A Modular Approach to Acquisition Systems for Future CERN Beam Instrumentation Developments*, in the proceedings of the *15th International Conference on Accelerator and Large Experimental Physics Control Systems*, Melbourne, Australia, 17–23 October 2015, p. 1103–1106 [DOI:10.18429/JACoW-ICALEPCS2015-THHB2002].

2024 JINST 19 C02052