



The Compact Muon Solenoid Experiment

# Conference Report

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## Performance and test of the new CMS ECAL Barrel front-end electronics for HL-LHC

Cecilia Borca for the CMS Collaboration

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The CMS ECAL barrel is set to undergo a substantial upgrade to meet the new and more challenging requirements of the High-Luminosity LHC (HL-LHC) accelerator. This upgrade involves a comprehensive redesign of the on-detector readout electronics, introducing new faster ASICs. The upgraded readout architecture will consist of a fast trans-impedance amplifier, called CATIA, and a two-channels 12-bit 160 MS/s ADC and a data selection and compression ASIC, called LiTE-DTU. The output of each readout channel is a single 1.28 Gbps serial line, which is connected to an e-link of the lpGBT radiation tolerant transceiver. The data from all readout channels will be sent to an FPGA based data processor located outside the LHC cavern. Extensive testing has been carried out at both ASIC and system levels, demonstrating the readiness of all the prototypes and the systems ability to meet the time and energy resolution requirements, also in beam test settings. The highlights of these tests will be presented.

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## Performance and Test of the New CMS ECAL Barrel Front-end Electronics for HL-LHC

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The CMS ECAL barrel is set to undergo a substantial upgrade to meet the new and more challenging requirements of the High-Luminosity LHC (HL-LHC) accelerator. This upgrade involves a comprehensive redesign of the on-detector readout electronics, introducing new faster ASICs. The upgraded readout architecture will consist of a fast trans-impedance amplifier, called CATIA, and a two-channels 12-bit 160 MS/s ADC and a data selection and compression ASIC, called LiTE-DTU. The output of each readout channel is a single 1.28 Gbps serial line, which is connected to an e-link of the lpGBT radiation tolerant transceiver. The data from all readout channels will be sent to an FPGA based data processor located outside the LHC cavern. Extensive testing has been carried out at both ASIC and system levels, demonstrating the readiness of all the prototypes and the system's ability to meet the time and energy resolution requirements, also in beam test settings. The highlights of these tests will be presented.

*Keywords:* Beam Test, Calorimeters, CMS, Front-end Electronics, High-luminosity LHC, Readout Electronics

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### 1. Introduction

The Electromagnetic Calorimeter (ECAL) of the Compact Muon Solenoid (CMS) [1], a general-purpose detector at the Large Hadron Collider (LHC), is crucial for the physics program of the experiment, providing high-precision measurements of electron and photon energies. The ECAL comprises 75848 lead tungstate scintillating crystals, organized into a central barrel section (EB) and two endcaps (EEs).

With the transition to the High-Luminosity LHC (HL-LHC) [2], the luminosity will increase by a factor of 5, reaching  $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ . This increase will raise the number of proton-proton interactions per bunch crossing (pile-up) from 60 to 200 and create a more challenging radiation environment. Due to unsustainable radiation damage in the forward region, the EE will be replaced with a new detector. On the contrary, the 61200 EB crystals and the avalanche photo-diodes (APDs) will be kept and refurbished with new front-end and back-end boards.

The EB upgrade is driven by the new Level-1 trigger requirements – which include an increase in rate from 150 kHz to 750 kHz and an increase in latency from approximately 4  $\mu\text{s}$

to 12.5  $\mu\text{s}$  – and, most importantly, by the target time resolution of 50 ps for electron and photons above 50 GeV. Improved time resolution, in fact, will help mitigate the increased pile-up enabling better primary vertex identification and effective discrimination of the true scintillation signals from anomalous hits in the APDs (spikes), which have faster rise time.

### 2. The upgrade of the CMS ECAL for HL-LHC

The new ECAL front-end electronics will maintain the same geometry, shown in Figure 1, as the legacy system. This setup includes five very-front-end (VFE) boards, each with 5 channels, and a low voltage regulator. These boards connect to a motherboard on the crystal side and interface with the front-end (FE) board on the opposite side.

The new VFE cards embed five pair of two ASICs: one for amplifying APD signals and another for analog-to-digital conversion, data serialization, and transmission with minimal digital processing. The first ASIC, the calorimeter trans-impedance amplifier (CATIA) [3], features a 35 MHz bandwidth and is built using a 130 nm CMOS process. It includes two parallel voltage amplification stages providing gains of 1 and 10, ensuring optimal energy reconstruction across a range from 50 MeV to 2 TeV. The second ASIC, the Lisbon-Turin ECAL

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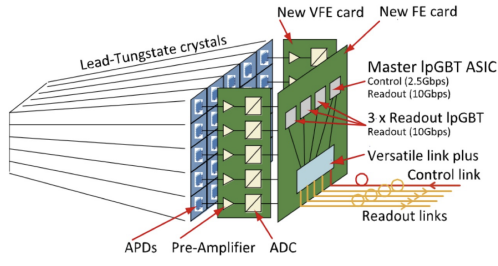


Figure 1: CMS ECAL upgraded front-end electronics schema

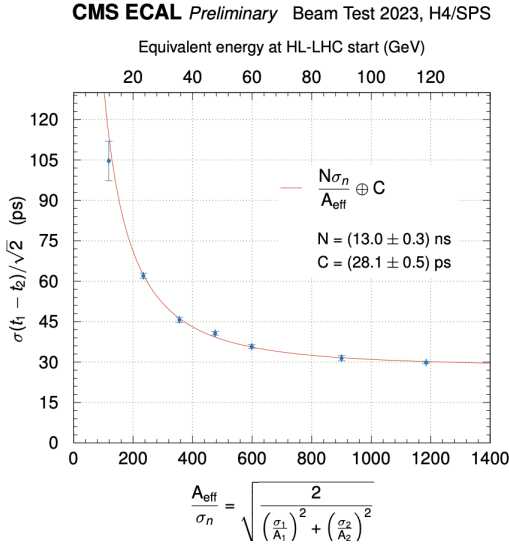


Figure 2: The measurement is done with the electron beam hitting two crystals (in two different readout units, read by two different back-end boards) simultaneously and computing the difference in time between the two

data transmission unit (LiTE-DTU) [4], integrates two 12-bit ADCs operating at  $160 \text{ MS}^{-1}$  to digitize signals from CATIA. A look-ahead algorithm selects the highest non-saturated sample to capture the optimal pulse shape, appending an additional bit to indicate the chosen gain. A loss-less data compression algorithm, a simplified Huffman encoding [5], allows data to fit the limited 1.28 Gbps bandwidth available per channel.

### 3. Beam test results

Several test beam campaigns have been conducted in recent years. Notably, in 2023, 250 crystals of a spare ECAL module were equipped and read out using the new back-end, generating a substantial amount of high-quality data at CERN's SPS. Data were collected at different energies, ranging from 20 to 300 GeV. The energy resolution is compatible with the current system and meets the specification of less than 1% for electrons and photons above 50 GeV. As shown in Figure 2, the data also confirm that the target time resolution is achieved, validating the complete readout chain.

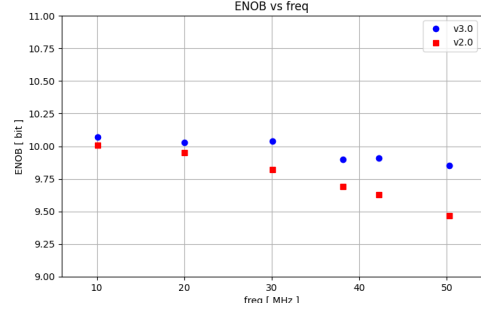


Figure 3: LiTE-DTU ENOB improvement in version 3.0

### 4. LiTE-DTU v3.0 performance improvement

The final iteration of the ASIC, LiTE-DTU v3.0, was submitted with several enhancements, the most significant of which concern the phase locked loop (PLL): the power supply was improved, and an auto-lock feature was implemented. Laboratory test results indicate a reduction in the clock jitter generated by the PLL, which is critical for timing performance. This improvement is highlighted in Figure 3, showing an increased effective number of bits (ENOB) compared to the previous version [6].

### 5. Conclusion

The upgrade of the CMS ECAL addresses the challenges of an increased luminosity. The new front-end electronics, featuring advanced ASICs, the CATIA and the LiTE-DTU, will ensure precise energy reconstruction and a remarkably improved time resolution of 40 ps (for energies above 50 GeV). Extensive testing, including beam tests and laboratory tests, has demonstrated that the new readout meets the requirements, allowing ECAL to maintain and improve its performance, crucial for the physics program of the CMS at HL-LHC.

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