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Dual use driver for high speed links transmitters in the future high energy physics experiments

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Abstract: The paper presents the **D**ual **U**se **D**riv**e**r (DUDE) for high speed links, a circuit designed for the Demonstrator ASIC for Radiation-Tolerant Transmitter in 28 nm CMOS (DART28) developed under the EP-R&D programme on technologies for future high energy physics experiments. The driver operates at 25.6 Gbps and it allows driving both 100 Ω transmission lines and optical Ring Modulators (RMs) integrated in a photonics integrated circuit (PIC). The driver includes configurable pre-emphasis. The device will allow to demonstrate the feasibility of wavelength division multiplexing (WDM) optical links operating with bandwidths in excess of 100 Gbps per fiber that are capable of sustaining total ionizing radiation doses up to 10 MGy.

Keywords: Analogue electronic circuits; Digital electronic circuits; Radiation-hard electronics

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Contents

1 Introduction

The Strategic EP-R&D Programme on Technologies for Future Experiments [1] develops technologies for the next generation of experiments. In an initial phase the ASIC developments, within the programme, aim at generic demonstrators and proof of concept prototype ASICs that will be later repurposed into specific HEP detector developments. The DART28 is developed as a part of work package 6 (WP6) — High Speed Links. One of the objectives of WP6 is to demonstrate WDM optical links which are capable of sustaining radiation with Total Ionizing Dose (TID) approaching 10 MGy with a bandwidth of 100 Gbps per fiber [2–4].

2 Architecture

The DART28 ASIC incorporates four transmitters to allow driving four RMs. Each transmitter consists of a data generator, scrambler, forward error correction, serializer, output driver and a phase-locked loop (PLL). Radiation tolerant design techniques were implemented in the DART28 design [5–7].

The DUDE is a multipurpose, modular unit that is capable of driving both 100 Ω transmission lines and RM. This approach allows not only silicon photonics (SiPh) co-integration but it extends the testability of the system. The DUDE is a pseudo-differential driver with two symmetric complementary outputs. It operates at 25.6 Gbps per lane and uses NRZ signaling.

The block diagram of the driver is presented in the figure 1. The architecture is based on the source-series-terminated (SST) transmitter [8–10]. The output stage is segmented to enable adjustment of the output current which is desirable in order to compensate for process voltage temperature (PVT) variations and adapt to various loads.

The driver consists of an input multiplexer which delivers signal to the n- and p-sections. Each section includes: main-cursor driver with 15 segments, pre-cursor driver with 7 segments, post-cursor driver with 7 segments. In total there are 29 segments which can be enabled and programmed individually. Each segment consists of a pre-driver and an output driver unit cell. The n- and p-sections can be programmed independently, which allows driving both symmetrical and asymmetrical loads.

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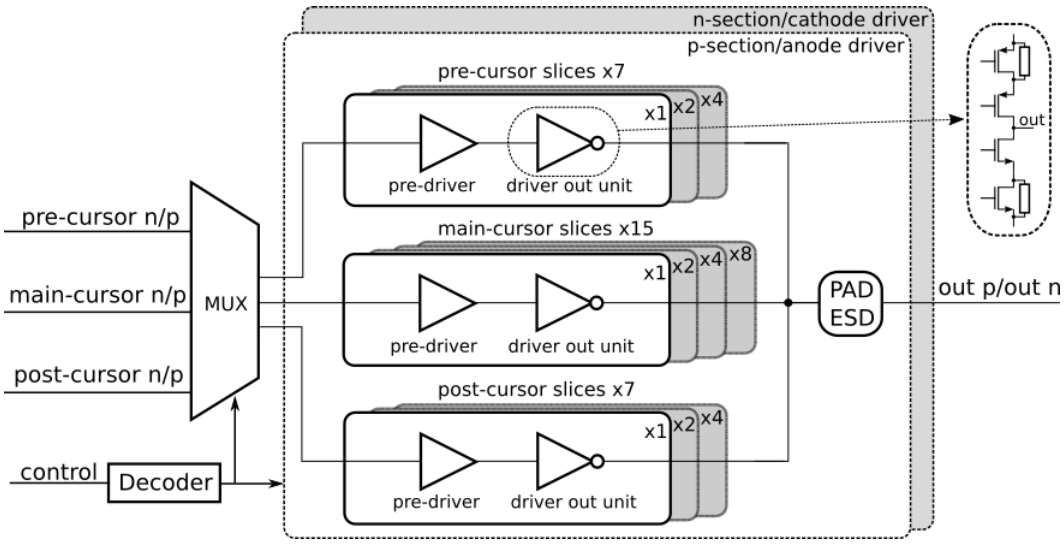

Figure 1. Dual Use Driver block diagram.

3 Modes of operation

The output unit cell consists of four transistors and two resistors figure 1. This structure allows programming the output driver in the following modes of operation: full swing driver, reduced swing driver, 100 Ω transmission line driver.

3.1 Full swing mode

The full swing mode is used to maximize the output amplitude. The diagram of the driver in full swing mode is presented in figure 2. The output load of the driver (Z_{load}) is driven pseudo differentially. Both n- and p-sections are programmed in the full swing mode. The driving strength is controlled by the number of enabled segments. The enabled segments work as an inverter — top PMOS and bottom NMOS are always turned on; data input is connected to the middle PMOS and NMOS. The disabled segments are configured in a high impedance state — both NMOSes and both PMOSes are off. The simulated eye diagram of the voltage measured over the load impedance is presented in figure 4(a). The load impedance is modeled as a differential 100 Ω transmission line with PCB's stray capacitance and an interconnect bond wire inductance between application specific integrated circuit (ASIC) and PCB.

3.2 Reduced swing mode

A particular challenge is driving SiPh RMs using the low supply voltages required for the 28 nm CMOS technologies. The thick-oxide devices that could support higher voltages should be avoided because they do not sustain high TIDs and are not recommended in the applications which have to withstand over 100 Mrad doses [11]. To overcome this limitation (and to maximize the driving amplitude) the RM is driven pseudo-differentially on both the anode and cathode terminals. This, however, can lead to the PN-junction of the RM being forward biased, which would result in degraded performance and thus must be avoided. To prevent that, the driver was designed to produce a reduced (and programmable) signal swing on the anode terminal.

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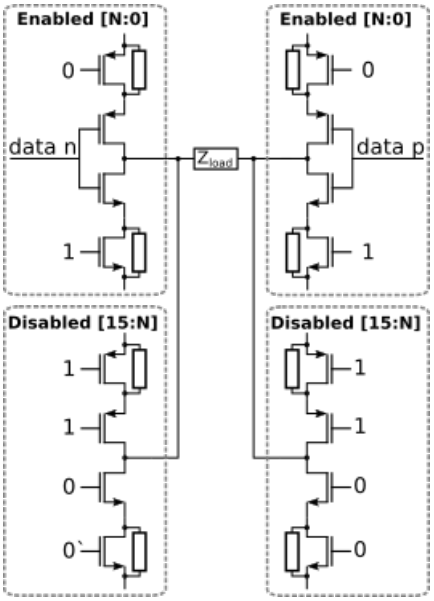


Figure 2. Block diagram of the driver in the full swing mode with n-section on the left side and p-section on the right side of the load impedance.

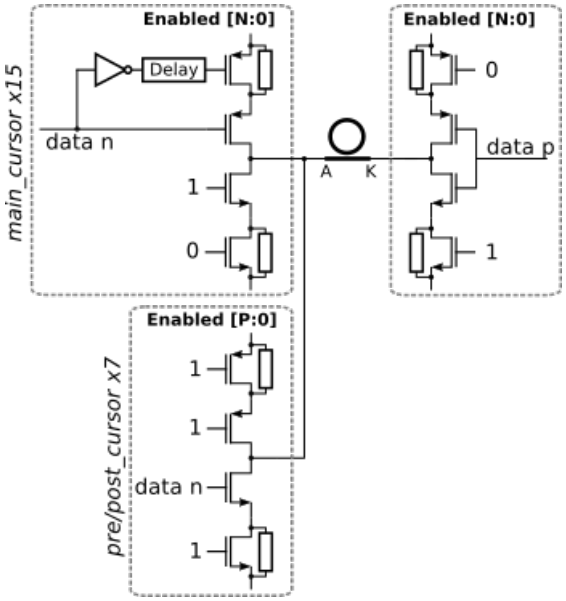
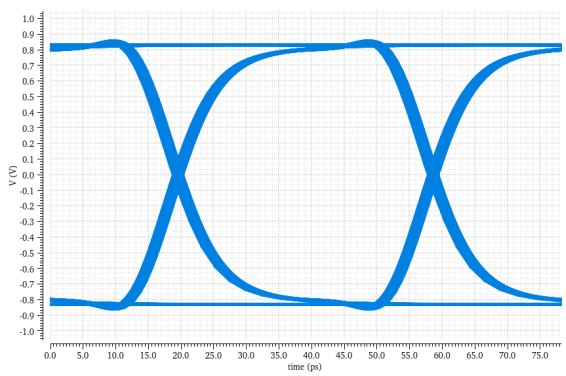
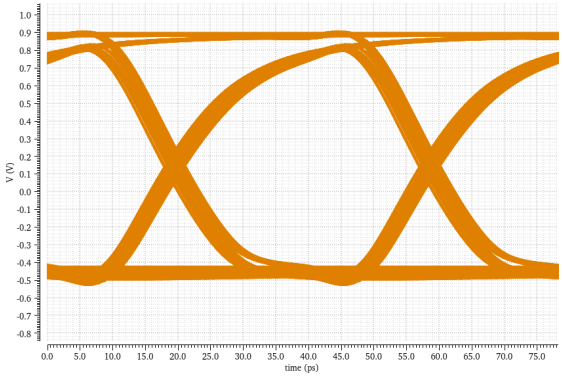


Figure 3. Block diagram of the driver with the RM load. The anode driver is programmed in the reduced swing mode, the cathode driver is programmed in the full swing mode.



(a) Full swing mode, 15 enabled segments, 100 Ω load.



(b) Reduced swing mode, 8 enabled segments, RM load.

Figure 4. Simulated eye diagrams of the driver with 25.6 Gbps PRBS7 input sequence.

The driver diagram in the reduced swing mode is presented in the figure 3. In this case, the anode driver is configured to produce a signal swing with limited amplitude and the cathode driver is set in full the swing mode.

The reduced swing mode uses the main-cursor and pre-cursor/post-cursor slices. When a logic 1 is set on the data_n input then on the anode the voltage level is equal to the ground level. During the falling transition of the input data_n signal, the output transition is boosted by the direct connection of the anode to the power rail by two PMOSes. This behaviour is obtained by the inverter with delay circuit in the main-cursor. When a logic 0 is present on the data_n input then the anode voltage level is set by the resistor voltage divider formed by the resistors in the main-cursor slice

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(middle PMOS and NMOS on and "external" PMOS and NMOS open). An example eye diagram for this mode is presented in figure 4(b) — the voltage over the RM is reduced to half of the power supply when the ring is forward biased.

3.3 Transmission line mode

This mode is used to drive a transmission line. The diagram of the driver in this mode is presented in the figure 5. The data input signal is connected to the middle PMOS and NMOS. The inverted and delayed data signal is connected to the top PMOS and bottom NMOS. This structure allows to increase the current supplied during signal transition and limits the current in a steady state.

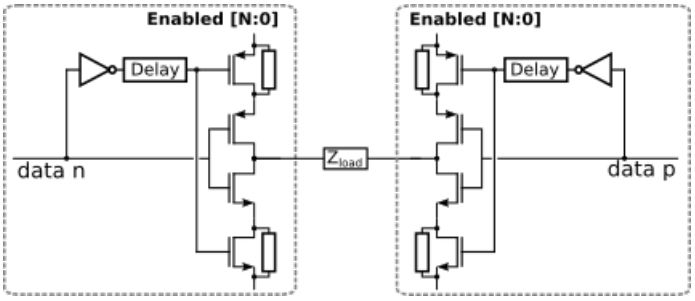

Figure 5. Block diagram of the driver in 100 Ω transmission line driver mode.

The DUDE includes a pre-emphasis circuit which is able to compensate for channel bandwidth limitations in order to minimize intersymbol interference (ISI). Two modes of pre-emphasis are implemented: edge pre-emphasis and three-tap feed-forward equalization (FFE) (bit-level pre-emphasis) [12, 13].

3.3.1 Edge pre-emphasis

Edge pre-emphasis is used to improve rise and fall times at the output nodes of the driver by providing more current to the load during signal transitions. Its strength can be modulated by changing the duration of the current impulse and the amount of additional current supplied. Its duration is controlled by a programmable delay circuit and the amplitude by changing the number of enabled segments. The delay circuit consists of a chain of multiplexers which deliver the programmable delay between delay of one and four inverter units. In the steady state, the output node is connected through the pull up or pull down resistor to the power rails, limiting the current flow through the load resistance.

3.3.2 Three-tap feed-forward equalization

FFE can be used when there is a significant bandwidth limitation in the transmission channel. It is implemented using the pre- and the post-cursor drivers. Their driving strength is individually programmable for optimal equalization of bandwidth-limited channels. The schematic of the FFE is presented in figure 6.

The simulated eye diagram shown in figure 7(a) presents the signal at the output of the bandwidth limited channel to 6.4 GHz while the bit rate is 25.6 Gbps. Without FFE, substantial eye closure can be observed. FFE allows recovering an open eye at the receiver, effectively overcoming the bandwidth limitation (figure 7(b)). It boosts the amplitude of signals with short duration and reduces amplitude of signals with long duration.

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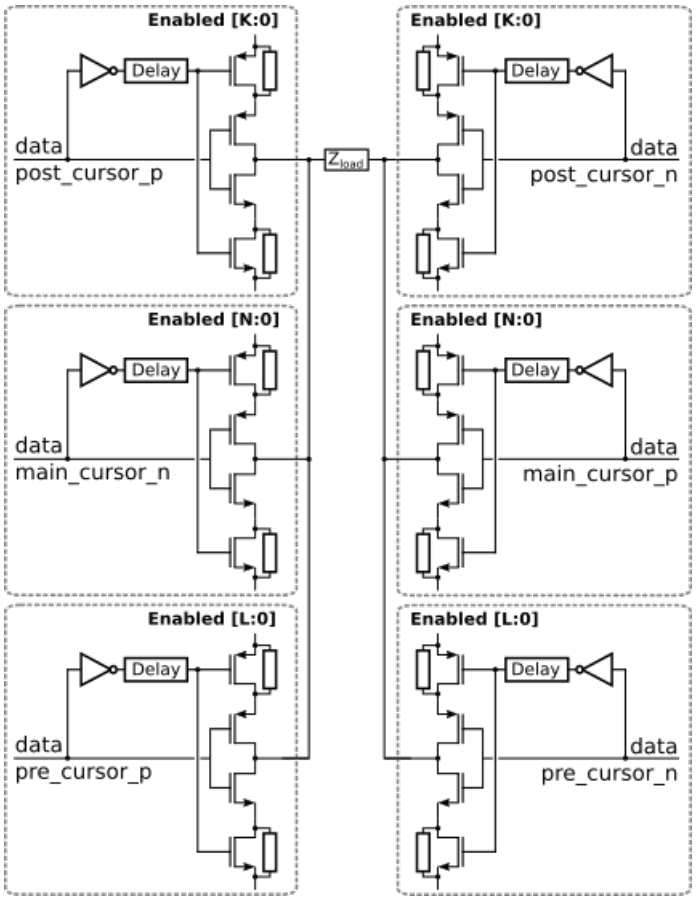
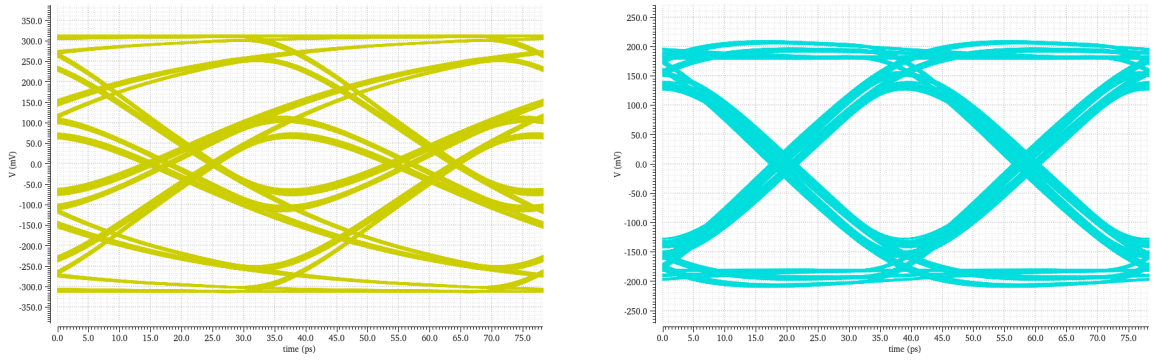


Figure 6. Block diagram of the driver in transmission line driver mode with FFE.



(a) without equalization

(b) with feed-forward equalization

Figure 7. Simulated eye diagram of the driver with 25.6 Gbps PRBS7 input sequence when the transmission channel bandwidth is limited to 6.4 GHz.

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4 Conclusions

This paper presents the output driver developed for the DART28 ASIC. It operates at a data rate of 25.6 Gbps using NRZ signaling. It uses a modular architecture providing different operating modes that allow driving various loads. The driver is capable of driving both resistive and capacitive loads such as transmission lines and optical RM. It was designed for co-integration with SiPh PICs and for radiation tolerance.

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