DRD 7: Proposal for an R&D Collaboration on: Electronics and On-Detector Processing

The DRD7 Collaboration

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1 Introduction

The undersigned institutes intend to form a new CERN DRD collaboration to develop future electronic systems and technologies for particle physics detectors. This intention was expressed in a Letter of Intent [1] submitted to the DRDC on 15 September 2023, and is now formalized in this proposal.

As documented in the ECFA R&D Roadmap [2], high-performance electronic systems are a key aspect of all future detector projects. The complexity and cost of the necessary developments are high and continue to increase. Delivery of new detectors will require a greater level of coordination and better ways of cooperative working within the field, and the new DRD7 collaboration will provide the platform to support this approach.

The collaboration's work will include development and demonstration of new hardware, firmware, and software concepts relevant to the requirements of medium- and long-term detector projects. The Technology Readiness Level (TRL) of the investigated themes will be low (typically 1 to 5), targeting in priority disruptive, transformative, far reaching goals. This will differentiate many electronics projects carried out in DRD7 from the higher TRL level components needed in the short term to perform detector developments in other DRDs . The collaboration will however also facilitate access to expertise, tools, and industry vendors in support of the entire DRD programme, and will act as a focal point for development of future common standards and approaches. It will support both specific technical goals in the area of electronics, and the general strategic recommendations of the Roadmap.

The collaboration will bind together the efforts of experts across a range of European and international institutes, ranging from large laboratories to individual researchers with particular expertise. Major electronic systems are now too complex for any single institute to implement alone, often requiring expertise in disparate technologies. Through adoption of open development practices and support for the sharing of IP, we will increase the efficiency and capability of all participants. The large laboratories will continue to facilitate access to advanced tools and technologies on behalf of the collaboration as a whole. The work of all DRD collaborations will be supported by adoption of common standards for IP integration and interfaces, and through well-supported workflows for electronic system and component simulation, design, and verification. The development of new detector electronic systems will therefore be a joint enterprise between this and other DRD collaborations, involving sharing of both people and resources.

2 Collaborating Institutes

68 Institues from 19 countries intend to collaborate to DRD7. They are listed in Fig 1 below.

Country	Institute	Email address
AT	Graz University of Technology, Institute of Electronics	alicja.michalowska@tugraz.at
BE	KU Leuven	levi.marien@kuleuven.be
CA	Sherbrooke University	serge.charlebois@usherbrooke.ca
Cern	CERN	francois.vasey@cern.ch
CH	EPFL	edoardo.charbon@epfl.ch
	University of Geneva, DPNC	anna.sfyrla@cern.ch
DE	Bergische Universitaet Wuppertal	wagner@uni-wuppertal.de
	Deutsches Elektronen-Synchrotron (DESY)	christian.reckleben@desy.de
	Fachhochschule Dortmund	michael.karagounis@fh-dortmund.de
	Forschungszentrum Jülich	A.Zambanini@fz-juelich.de
	Karlsruhe Institute of Technology (KIT)	frank.simon@kit.edu
	MPG HLL	lca@hll.mpg.de
	RWTH Aachen University, Physics Institute IB	feld@physik.rwth-aachen.de
EE	Tallinn University of Technology (TalTech)	andrii.chub@taltech.ee
ES	Centre for Energy, Environmental and Technological Research (CIEMAT)	cristina.fernandez@ciemat.es
	Galician Institute of High Energy Physics (IGFAE)	antonio.fernandez.prieto@cern.ch
	Instituto de Física Corpuscular (IFIC) Valencia	Arantza.Oyanguren@ific.uv.es
	Instituto de Física de Cantabria (IFCA)	ivan.vila@csic.es
	Instituto de Microelectrónica de Barcelona (IMB-CNM)	miguel.ullan@imb-cnm.csic.es
	Instituto Tecnológico de Aragón (ITAINNOVA)	farteche@itainnova.es
	Universidad de Oviedo	santiago.folgueras@cern.ch
	University of Barcelona-ICCUB	dgascon@fqa.ub.edu
FR	CEA-LETI	cedric.dehos@cea.fr
	Institut Polytechnique de Paris, CNRS-IN2P3, OMEGA	taille@in2p3.fr
	Laboratoire d'Annecy de Physique des Particules (LAPP)	Pierre.Delebecque@lapp.in2p3.fr
	Laboratoire de Physique de Clermont - LPC	lderamo@cern.ch
	Laboratoire de physique nucléaire et de hautes énergies (LPNHE)	giovanni.calderini@lpnhe.in2p3.fr
	Univeristy Grenoble Alpes, CNRS, LEGI	damien.colombet@univ-grenoble-alpes.fr
	Université Aix-Marseille, CNRS-IN2P3, CPPM	legac@cppm.in2p3.fr
	Université Claude Bernard Lyon 1, CNRS-IN2P3, IP2I	d.contardo@ipnl.in2p3.fr
	Université de Strasbourg, CNRS-IN2P3, IPHC	jerome.baudot@iphc.cnrs.fr
	Université Grenoble Alpes, CNRS-IN2P3, LPSC	fmalek@lpsc.in2p3.fr
	Université Paris-Saclay, CEA, IRFU	florent.bouyjou@cea.fr
	Université Paris-Saclay, CNRS-IN2P3, IJClab	daniel.charlet@ijclab.in2p3.fr
IL	Tel-Aviv University	Yan.Benhammou@cern.ch
IT	INFN Pisa	Fabrizio.Palla@cern.ch
	INFN Torino	darochar@to.infn.it
	INFN-Arcadia project, represented by INFN Torino	darochar@to.infn.it
	Scuola Superiore Sant'Anna Pisa	claudio.oton@santannapisa.it
	Università degli Studi di Milano and INFN Sezione di Milano	attilio.andreazza@mi.infn.it
	Università di Padova	piero.giubilato@unipd.it
	University of Bergamo / INFN Pavia / University of Pavia	luigi.gaioni@unibg.it
	University of Trento	philippe.velha@unitn.it
	University of Udine	stefano.saggini@uniud.it
JP	KEK, High Energy Accelerator Research Organization	kisisita@post.kek.jp
KR	Daegu Gyeongbuk Institute of Science and Technology (DGIST)	gain.kim@dgist.ac.kr
	Gangneung-Wonju National University (GWNU)	elizabeth.locci@cern.ch
NL	NIKHEF	r.kluit@nikhef.nl
NO	Norwegian Institutes (UiB, UiO, USN) represented by University of Bergen (Ui	johan.alme@uib.no
PL	University of Krakow AGH	Marek.Idzik@cern.ch
SE	University of Uppsala	richard.brenner@physics.uu.se
UK	Imperial College	g.iles@imperial.ac.uk
	Queen Mary University of London (QMUL)	m.bona@qmul.ac.uk
	UKRI-STFC Rutherford Appleton Laboratory (RAL)	mark.prydderch@stfc.ac.uk
	University College London (UCL)	a.korn@ucl.ac.uk
	University of Birmingham	S.J.Hillier@bham.ac.uk
	University of Bristol	David.Cussans@Bristol.ac.uk
	University of London Royal Holloway	veronique.boisvert@rhul.ac.uk
	University of Manchester	conor.fitzpatrick@cern.ch
	University of Oxford; Rutherford Appleton Laboratory	prof.jocelyn.monroe@gmail.com
	University of Warwick	karolos.potamianos@cern.ch
US	Argonne National Laboratory (ANL)	jinlong.zhang@cern.ch
	Brookhaven National Laboratory (BNL)	chc@bnl.gov
	Fermilab National Laboratory (FNAL)	dbraga@fnal.gov
	Ohio State University	gan.1@osu.edu
	SLAC National Accelerator Laboratory	lorenzor@slac.stanford.edu
	University of Boston	angelo.giacomo.zecchinelli@cern.ch
	University of Minnesota	rusack@umn.edu

Figure 1: Institutes collaborating to DRD7

3 Organisation of the Collaboration

The DRD7 collaboration was formed in a bottom-up process following community meetings soliciting input to its scientific program. The scientific organisation of the collaboration closely follows the Detector R&D Research Themes for electronics defined in the ECFA Detector R&D Roadmap, with some modifications accounting for items that have emerged during the community

meetings. The governing bodies of the collaboration have also emerged from the experience of the collaboration forming process. Both the scientific organisation and the governance of DRD7 are outlined in the following sections. This reflects an evolution from the ad-hoc structure in place during the proposal phase of the collaboration, and includes bodies typical for collaborations in high energy physics as well as DRD7-specific elements tailored to needs and working style of the community. It represents a proposal for the organisation at this point, the final structure of DRD7 will be decided by the Collaboration Board (see below) once DRD7 has been approved.

3.1 Scientific Organisation

The scientific work in the collaboration is organised in R&D projects, each with a well-defined scope defined for an initial duration of three years. The projects are grouped into six development areas (organized as Work Packages), complemented by a Working Group with a wider transversal role in coordination and support for which a mandate has been defined (WG7.7):

- Data density and power efficiency (WP 7.1)
- Intelligence on the detector (WP 7.2)
- 4D and 5D techniques (WP 7.3)
- Extreme environments (WP 7.4)
- Backend systems and commercial-off-the-shelf components (WP 7.5)
- Complex imaging ASICs and technologies (WP 7.6)
- Tools and Technologies (WG 7.7)

In the first six areas, a number of well-defined projects with clear development goals address the priority themes highlighted in the ECFA detector R&D roadmap. Currently, 15 projects are proposed. These projects will provide specific technical outputs, and act as pathfinders towards a new vision for future electronic systems based on multilateral cooperation in electronics developments. Resources to implement these projects are available, or will be sought from national funding agencies and large laboratories. For the seventh area (WG7.7), the working group will be tasked with proposing an implementation scheme according to the vision described in its mandate.

The Work Packages and associated projects are described in sections 5 to 10 below. 11 describes the transversal Working Group. The Collaboration will remain open to new projects and is intended to continue and evolve in the long-term. Regular calls for new projects and participants will be issued on a yearly basis. New project proposals will be first reviewed and pre-selected by the respective work package conveners and subsequently passed to the Steering Committee for final selection and proposal to the Collaboration Board. Changes to running projects (in scope or participating institutes) will be handled in a similar way.

3.2 Governance

The main governing bodies of the DRD7 collaboration are the **Collaboration Board**, the **Steering Committee**, with the chairperson and deputy chairperson of the Steering Committee as the main representatives of the collaboration, and the **Resources Board**. The scientific structure of the collaboration is represented by the Work Package (Working Group) Conveners. Note that in the following discussion often no explicit distinction is made between Work Package and Working Group in terms of governance, since the structure in that regard is identical. Work Package Conveners and Steering Committee come together in the **Technical Committee**. Collaboration membership is defined by contributions to one or several DRD7 projects.

Subsection 3.3 provides further context for the structure of the collaboration bodies and the composition of their membership in the proposal phase, and lays out the transition process after collaboration forming.

The structure of the DRD7 collaboration is sketched in figure 2, with details on the individual bodies given below.

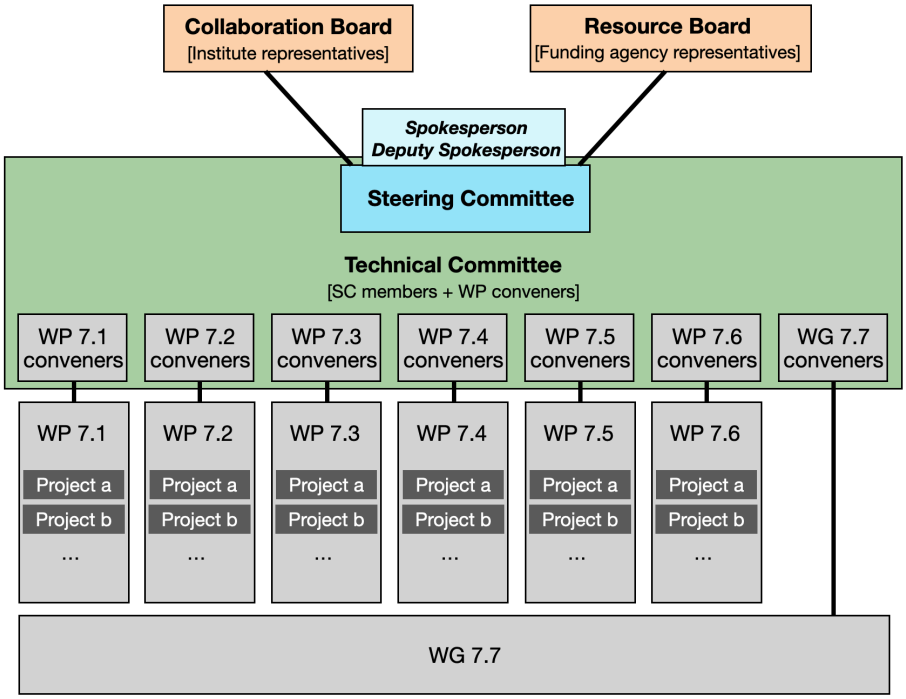

Figure 2: Structure of the DRD7 collaboration. Connections between projects and work packages are omitted for clarity.

- The **DRD7 collaborators** are the project contributors. They are regrouped into the Work Package corresponding to their project development area, as defined in the scientific structure of the collaboration.

- The **Work Packages** are led by **Conveners** (two or three per WP) who oversee the projects and animate regular forums where the specialists community is invited to exchange ideas and reflect. The forums are the place where collaboration members (the project contributors) meet their observing peers from other backgrounds or DRDs. Topics under discussion derive from the Work Package projects, but may also include material suggested by observing partners. The concrete scientific and technical work within the **Projects** is coordinated by self-organized structures, which are established in consultation with the corresponding WP conveners.
  In addition to forums, more formal links with other DRDs may be established if required, by for instance organizing periodic meetings between the DRD7 Technical Committee and the DRD-link-persons for electronics.
  Conveners also organize and chair the work package sessions during the periodic DRD7 collaboration workshops, and aggregate material for the annual DRD7 progress report.

- The transversal **Working Group** WG7.7 is organized analogous to the work packages described above, with the distinction that it does not host projects. Instead, it has a transverse mandate to propose an implementation solution for a hub-based structure in the HEP community.

- The **Steering Committee** guides the Collaboration and represents it to the outside world, in particular to the DRDC. The Steering Committee follows the progress and activities of the Work Packages. It updates the R&D vision of the Collaboration and calls regular DRD7 workshops to report publicly on the progress of the R&D effort. Each year, the Steering Committee issues the annual DRD7 progress report and presents it to the Collaboration Board. The Steering Committee nominates Work Package Conveners, to be approved by the Collaboration Board.

The Steering Committee proposes a Chairperson and a Deputy from its members for approval by the Collaboration Board. They jointly chair the committee and serve as the **Spokesperson** and **Deputy Spokesperson** of the collaboration, constituting the main representatives and contact points. The term of office is one year, and while extensions are possible, rotation among the members is desired.
The Steering Committee consists of four to eight members, ideally representing the scientific and regional diversity of the collaboration. The term of membership in the Steering Committee is three years, normally renewable once. To ensure continuity as well as changes in membership, each year up to two members of the Steering Committee will be replaced. Candidates are expected to be identified by an ad-hoc search committee mandated by the collaboration board, and are elected and appointed by the collaboration board.

- The Work Package Conveners and the Steering Committee collectively form the **Technical Committee** which tracks projects, organizes internal reviews and monitors progress. It is the Technical Committee which issues recommendations to the projects and drafts the annual DRD7 progress report. The Technical Committee will also oversee presentations and publications in the framework of DRD7. It is expected that concrete procedures will be worked out and documented in the initial phase of the collaboration.

- The DRD7 **Collaboration Board** is the scientific and technical representation of the collaborating institutions. Each contributing institute sends one representative to the Collaboration Board. The board meets at least once per year to discuss progress and vision, ideally at the time of the DRD7 workshop. It approves the annual DRD7 progress report, the eventual proposals for new projects, work packages and contributors, appoints the Steering Committee members and endorses the Spokesperson, Co-Spokesperson and the Work Package Conveners nominated by the Steering Committee.
  The Collaboration Board elects a chairperson from among its members, who will serve for a period of two years. A renewal is possible, but a rotation among institutes is desired.

- The DRD7 **Resources Board** represents the funding agencies supporting the projects in the collaboration. This representation can be through representatives of collaborating institutions, or delegated to a body acting on behalf of one or several institutions. The Resources Board meets at least annually, ideally at the time of the DRD7 workshop. It approves the annual DRD7 progress report and the eventual proposals for new projects and contributors.

3.3 Path towards forming the DRD7 Collaboration

During the collaboration forming phase, DRD7 has been guided by an ad-hoc Steering Committee with two co-chairs to be able to cover the intense workload of this phase in an effective and flexible manner. The membership of the Steering committee has evolved from the original membership of Task Force 7 of the ECFA Detector R&D Roadmap in place during the development of the roadmap, with the goal of achieving a broad representation of the relevant community while involving the main national laboratories in this strategic community-shaping exercise, and ensuring continuity with the roadmap recommendations.

The Steering Committee has appointed the Work Package Conveners, who in turn have guided the proposal phase for the first slate of projects of the collaboration. The selection of conveners has been driven by the requirement of a strong creation force for the formation of a new collaboration. The conveners were selected based on their recognized expert's status to drive the process with strength and credibility.

Once DRD7 is approved, the transition to the regular governance structure described in section 3.2 will be managed in a smooth way. As a first step, the Collaboration Board will be convened to elect its chair. The board members will then be asked for nominations of Steering Committee members, with the majority of current Steering Committee members expected to be willing to continue in their role for at least another year and being available as candidates. The Collaboration Board will then elect the members of the Steering Committee. Once in place, the Steering Committee will propose the Work Package Conveners, again with the expectation that the majority of those currently active in these roles will be willing to continue while being open to nominations,

rotation and increased diversity wherever possible. From the second year on, the rolling renewal of the Steering Committee will enter into effect, subject to Collaboration Board approval.

4 Description of the Work Packages, Working Group and Projects

The future R&D topics for electronics have been organised into a small number of coherent, but necessarily overlapping, themes. Each of these themes is developed in a Work Package through projects proposed by a set of institutes wishing to collaborate on a specific topic. Projects are thus proposed bottom-up according to the expertise, ambition and resources of the collaborating partners. They do not result in an exhaustive line of R&D for a given theme, but are representative of what the community can achieve at a given point in time.

The following six sections give an overview of the projects proposed in the six Work Packages of DRD7 as listed in 3.1 above. The last section 11 describes a model for future ASICs developments which WG7.7 is invited to reflect on and propose an implementation for. Comparing with the ECFA R&D Roadmap for electronics, the development themes which were not explicitly picked up by projects are: intelligent power management; advanced data reduction techniques (AI/ML); novel on-chip architectures; and reliability, fault tolerance and detector control. In this proposal, cooling is considered part of WP7.4 (extreme environments); depending on the evolution of the forming DRD8 Collaboration, some cooling-related projects may be best integrated in DRD8. If necessary, this will be fine tuned in due-time to best match the needs of the projects.

The resource information is provided in two complementary ways: first, integrated for each WP on a yearly basis, and second, project-by-project with average yearly numbers over the first three years of the collaboration. It is split into two categories, the available resources representing personnel and funds available at the participating institutes, and additional resources needed. The latter is the estimated additional requirement to achieve the full planned scope of the respective project. These additional resources are expected to be acquired through funding applications of the project partners, with the corresponding uncertainties.

To summarize, the projects and their work packages are listed in Table 1 below. Full details are available in Appendix B (public information) and Appendix C (confidential information). The detailed list of contributors to projects and working groups is in Appendix A.

Table 1: DRD7 work packages, working group and projects

WP7.1	**PROJECTS**
Data density and power efficiency	**7.1a** Silicon Photonics transceiver development **7.1b** Powering next generation detector systems **7.1c** Wireless Data And Power Transmission (WADAPT)
WP7.2	
Intelligence on the detector	**7.2b** Radiation tolerant RISC-V SoC **7.2c** Virtual electronic system prototyping
WP7.3	
4D and 5D techniques	**7.3a** High performance TDC and ADC blocks at ultra-low power **7.3b1** Strategies for characterizing and calibrating sources impacting time measurements **7.3b2** Timing distribution techniques
WP7.4	
Extreme environments	**7.4a** Device modelling and development of cryogenic CMOS PDKs and IP **7.4b** Radiation resistance of advanced CMOS nodes **7.4c** Cooling and cooling plates
WP7.5	
Backend systems and COTS components	**7.5a** DAQOverflow **7.5b** From FE to BE with 100GbE
WP7.6	
Complex imaging ASICs and technologies	**7.6a** Common access to selected imaging technologies **7.6b** Shared access to 3D integration
WG7.7	
Tools and Technologies	**7.7** A Hub-based structure for ASICs developments

5 Work Package 7.1: Data density and power efficiency

More channels and more bits per sample require higher data rates inside and out of the front-end ASICs. Novel link technologies must be developed to cope with higher data rates, to connect neighbouring detector layers for advanced data reduction techniques, and to do so with reduced mass and power. Critical technologies include radiation-hard optical links, wireline, wireless, and free-space optics;

Low-power design techniques are needed at the front-end, including novel architectures. Efficient power distribution, power converter and regulator devices, and protection circuits are required to minimise detector mass and heating. Efficient readout controllers must work in concert with DAQ to optimally aggregate, buffer and transmit data to maximise the utilisation factor of very high bandwidth off-detector links.

The institutes contributing to WP7.1 and the aggregated Work Package resources are shown in figures 3 and 4 below. The Projects supported by WP7.1 are summarized in sections 5.1, 5.2 and 5.3.

Institutes	WP7.1a	WP7.1b	WP7.1c	Projects
AT		**1**		**1**
Graz University of Technology, Institute of Electronics		1		1
CA	**1**			**1**
Sherbrooke University	1			1
Cern	**1**	**1**		**2**
CERN	1	1		2
DE	**3**	**2**		**5**
Bergische Universitaet Wuppertal	1			1
Deutsches Elektronen-Synchrotron (DESY)	1			1
Fachhochschule Dortmund		1		1
Karlsruhe Institute of Technology (KIT)	1			1
RWTH Aachen University, Physics Institute IB		1		1
EE		**1**		**1**
Tallinn University of Technology (TalTech)		1		1
ES	**1**	**1**		**2**
Galician Institute of High Energy Physics (IGFAE)	1			1
Instituto Tecnológico de Aragón (ITAINNOVA)		1		1
FR			**2**	**2**
CEA-LETI			1	1
Université Grenoble Alpes, CNRS-IN2P3, LPSC			1	1
IL			**1**	**1**
Tel-Aviv University			1	1
IT	**4**	**2**	**2**	**8**
INFN Pisa	1		1	2
Scuola Superiore Sant'Anna Pisa	1		1	2
Università degli Studi di Milano and INFN Sezione di Milano	1	1		2
University of Trento	1			1
University of Udine		1		1
KR			**1**	**1**
Gangneung-Wonju National University (GWNU)			1	1
SE			**1**	**1**
University of Uppsala			1	1
UK	**2**			**2**
Imperial College	1			1
University of Birmingham	1			1
US	**2**		**1**	**3**
Argonne National Laboratory (ANL)	1			1
Fermilab National Laboratory (FNAL)	1			1
Ohio State University			1	1
Projects	**14**	**8**	**8**	**30**

Figure 3: Institutes contributing to WP 7.1

7.x.y		FTE available				add. FTE needed				funds available [kEUR]				add. funds needed [kEUR]			
x	y	2024	2025	2026	>2026	2024	2025	2026	>2026	2024	2025	2026	>2026	2024	2025	2026	>2026
1	a	25.7	25.7	25.7	25.7	8.0	8.0	8.0	8.0	440.0	440.0	440.0	440.0	250.0	250.0	250.0	250.0
1	b	6.4	5.1	4.2	4.6	4.2	5.4	6.9	6.4	100.0	140.0	20.0	95.0	63.0	88.0	153.0	125.0
1	c	6.4	4.9	3.9	1.0	5.3	8.4	8.7	1.0	343.0	180.0	0.0	0.0	335.0	590.0	575.0	130.0
	total 7.1	**38.5**	**35.7**	**33.8**	**31.3**	**17.5**	**21.8**	**23.6**	**15.4**	**883.0**	**760.0**	**460.0**	**535.0**	**648.0**	**928.0**	**978.0**	**505.0**

Figure 4: Resources overview of WP 7.1

5.1 Project 7.1a

This project aims to develop high-speed optical transceivers based on Silicon Photonics technology for use in a wide range of future particle physics applications from low-temperature neutrino detectors to high-radiation environment HL-HLC pixel detectors.

Project Name	Silicon Photonics Transceiver Development (WP7.1a)
Project Description	Develop high-speed optical transceivers based on Silicon Photonics technology. Duration 4-5 years.
Innovative/strategic vision	First opportunity to design and operate custom optical data transmission systems in HEP detectors.
Performance Target	100 Gb/s per fibre optical readout with 2.5 Gb/s control optical link operating at a BER of 10^{-12}. Radiation tolerance up to 1×10^{16} particles/cm^2 and 10 MGy and power consumption of 250 mW. Cryogenic temperature operation for some lower-speed variants.
Milestones and Deliverables	**M7.1a.1** (M12) Cryogenic test of SiPh PIC **M7.1a.2** (M12) Submission of Ring Modulator Driver **D7.1a.1** (M12) Delivery of WDM test PIC **M7.1a.3** (M24) Radiation test of WDM PIC **D7.1a.2** (M24) Delivery of packaged WDM PIC **M7.1a.4** (M30) Submission of photodiode TIA **M7.1a.5** (M36) System test of WDM PIC with Driver
Multi-disciplinary, cross-WP content	Silicon Photonics combines data-density, timing distribution, Back-end, as well as 2.5/3D integration, with the need for foundry access to specialist processes.
Contributors	CA: Sherbrooke CERN DE: DESY, KIT, Wuppertal ES: IGFAE UK: Birmingham, Imperial IT: INFN Milano, INFN Pisa, Sant'Anna, Uni. Trento US: Argonne, Fermilab
Available resources	25.7 FTE/yr 440k/yr
Addt'l resource need	8 FTE/yr 250k/yr

5.2 Project 7.1b

This project aims to develop power distribution schemes and their voltage/current regulators and converters for use in a wide range of future particle physics applications, from low-temperature neutrino detectors to high-radiation environment HL-HLC pixel detectors and beyond (future collider experiments)

Project Name	Powering Next Generation Detector Systems (WP7.1b)
Project Description	Develop power distribution schemes and their voltage/current regulators. Duration 4-5 years.
Innovative/strategic vision	Develop very efficient converters (at least 90% at high load, 10A), and at unprecedented radiation hardness up to 1×10^{16} particles/cm^2 and 10 MGy . New technologies as CMOS High voltage 0.18um will be used along with new Gallium Nitride (GaN).
Performance Target	High-efficiency (at least 90% at high load) converters for serial and parallel powering schemes for high voltage conversion and around 75% for fully integrated DCDC in 28nm technology. Radiation tolerance up to 1×10^{16} particles/cm^2 and 10 MGy
Milestones and Deliverables, see Appendix B.1.2 for details of activities.	**M7.1b.2** (M12) Test results on first prototypes of a linear regulator and a resonant converter in 28nm technology **M7.1b.1,3,4,5** (M24) Tests on parallel and serial GaN DCDC converter prototypes with custom air core inductors **D7.1b.1,3,4,6** (M36) Delivery of a report on high voltage (48V) DC-DC converter for serial and parallel powering schemes
Multi-disciplinary, cross-WP content	Power distribution scheme combines connection with Back-end power supplies and integration of the on-chip regulation in the front-end ASICs (Pixel, strips and monolithic)
Contributors	AT: TU Graz CERN DE: FH Dortmund, RWTH Aachen University EE: Tallinn University of Technology (TalTech) ES: ITAINNOVA IT: INFN Milan, University of Udine (UNIUD), University of Milan (UNIMI)
Available resources	5.2 FTE/yr 87k/yr
Addt'l resource need	5.4 FTE/yr 101k/yr

5.3 Project 7.1c

This project aims to develop wireless technology based on a millimeter wave (mmw) transceiver IC as well as on Free Space Optics to connect neighboring detector layers, providing increased data rates, high power efficiency and high density of data links, with the aim of reducing mass and power consumption.

Project Name	WADAPT (WP7.1c)
Project Description	Develop millimeter wave Wireless technology together with Free Space Optics technology to connect neighboring detector layers with the aim of reducing mass and power consumption. Wireless power transmission will also be explored.
Innovative/strategic vision	First attempt to provide a promising alternative to cables and optical links that would revolutionize the detector design. Removing partly or totally cables would be a major advance in reducing the amount of spurious matter spoiling the measurement of the particle parameters. In addition wireless technology allows efficient partitioning of detectors in topological regions of interest, with the possibility of adding intelligence on the detector to perform four-dimensional reconstruction of the tracks and vertices online.
Performance Target	Radial wireless readout for pixel detectors. Data from detector front-end modules can be serialized as channels up to 10 Gb/s and be aggregated across detector layers (25 to 100 Gb/s). Commercially available technology has demonstrated radiation hardness amply sufficient for envisaged lepton colliders. Radiation hard transceivers will be developed in order to match radiation levels expected at future hadron colliders, maximum fluence at HL-LHC is 2×10^{16} particles/cm^2 and at FCC-hh is 6×10^{16} particles/cm^2.
Milestones and Deliverables	**M7.1c.1,2,3** (M12,24,36) Intermediate annual reports **D7.1c.4** (M24) Delivery of report summarising a proof of principle demonstration of multi-hop RF data transmission using commercial ICs **D7.1c.7** (M24) Delivery of a design of an optimized RF transceiver IC **D7.1c.10** (M36) Delivery of a test report demonstrating FSO data transmission, integration, radiation hardness **M7.1c.4** (M36) Demonstrators made available and training organized.
Multi-disciplinary, cross-WP content	mmw technology and FSO technology will as much as possible aim at developing common tools as common interfaces and common test benches in order to ease performance comparison in a given context and provide the users with adapted solutions. After proof of principle, the ultimate goal would be to generalize the use of wireless data-links to other detectors, with the potential of adding on-detector intelligence. This is however beyond the scope of this 3-years project and further system and implementation analysis will then be required. Some collaborations with group developing radiation hard ICs, 4D and monolothic techniques could be envisaged.
Contributors	FR: CEA-Leti, LPSC IL: Tel-Aviv IT: INFN Pisa, Scuola Superiore Sant'Anna KR: GWNU SE: Uppsala US: Ohio State University
Available resources	5 FTE /yr; 174k /yr
Add. resource need	7.5 FTE /yr; 500k /yr

6 Work Package 7.2: Intelligence on the detector

Front-end programmability, modularity and configurability must be vastly enhanced in order to allow fewer, more versatile front-end electronics to be developed;
Radiation-tolerant processors and programmable logic elements with common interfaces and protocols will allow re-use of shared developments;
High level system modelling will enable optimizing the overall readout chain efficiency for a given power and bandwidth budget, while providing a robust specification and verification framework for the hardware design phase.

The institutes contributing to WP7.2 and the aggregated Work Package resources are shown in figures 5 and 6 below. The Projects supported by WP7.2 are summarized in sections 6.1 and 6.2. Project 7.2a (e-FPGA) is not yet ready for launch and will be added to the Work Package portfolio in a future round.

Institutes	WP7.2b	WP7.2c	Projects
BE	**1**		**1**
KU Leuven	1		1
Cern	**1**	**1**	**2**
CERN	1	1	2
DE	**1**		**1**
Fachhochschule Dortmund	1		1
FR		**1**	**1**
Université de Strasbourg, CNRS-IN2P3, IPHC		1	1
UK	**4**		**4**
UKRI-STFC Rutherford Appleton Laboratory (RAL)	1		1
University of Bristol	1		1
University of London Royal Holloway	1		1
University of Warwick	1		1
US	**1**		**1**
Fermilab National Laboratory (FNAL)	1		1
Projects	**8**	**2**	**10**

Figure 5: Institutes contributing to WP 7.2

7.x.y		FTE available				add. FTE needed				funds available [kEUR]				add. funds needed [kEUR]			
x	y	2024	2025	2026	>2026	2024	2025	2026	>2026	2024	2025	2026	>2026	2024	2025	2026	>2026
2	a	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
2	b	6.7	6.2	5.7	5.5	7.2	8.2	8.2	8.2	20.0	50.0	50.0	100.0	5.0	20.0	40.0	20.0
2	c	3.0	3.0	3.0	3.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
	total 7.2	**9.7**	**9.2**	**8.7**	**8.5**	**7.2**	**8.2**	**8.2**	**8.2**	**20.0**	**50.0**	**50.0**	**100.0**	**5.0**	**20.0**	**40.0**	**20.0**

Figure 6: Resources overview of WP 7.2

6.1 Project 7.2b

The project aims to develop a radiation-hardened System-On-Chip (SoC) based on the RISC-V ISA standard.

Project Name	Radiation Tolerant RISC-V System-On-Chip (WP7.2b)
Project Description	Develop a radiation-hardened SoC based on the RISC-V ISA standard according to the roadmap defined in M7.2b.1. Topics: 1- SoC architectures 2- Radiation Tolerance design methodology, 3- Verification methodology, 4- SoC generator toolchain. Duration 5-6 years.
Innovative/strategic vision	Develop a technology and a design platform to anticipate and adapt the challenges and opportunities of the future Electronic systems and IC design.
Performance Target	The following targets will be defined in M7.2b.2: Processing Speed Power Consumption Radiation Tolerance Memory and Storage Communication Interfaces Scalability and Flexibility Verification and Testing
Milestones and Deliverables	**M7.2b.1** (M12) Rad-Tol RISC-V SoC roadmap **M7.2b.2** (M24) SoC architectures proposal **D7.2b.3** (M36) Delivery of Rad-Tol SoC building block test chip
Multi-disciplinary, cross-WP content	Electronics Engineering - Digital Design Computer Science - Embedded Systems Systems Engineering - Integration and Testing
Contributors	DE: FH Dortmund BE: KU Leuven CERN UK: UKRI-STFC RAL UK: Royal Holloway University Of London UK: University of Warwick UK: University of Bristol US: Fermilab
Available resources	6.15 FTE/year 40 kEUR/year
Addt'l resource need	7.9 FTE/year 21.7 kEUR/year

6.2 Project 7.2c

The project aims to develop a simulation of the readout chain of a particle detector at a high level modelling the essential components and processes that occur from the moment particles interact with the detector to the digital readout of the collected data.

Project Name	Virtual Electronic System Prototyping (WP7.2c)
Project Description	Develop frameworks for high-level simulation of particle detectors. **Topics:** **1-** Signal generation in detector elements **2-** Digitization and Signal Processing **3-** Data readout architecture Topics 1. and 3. aim to create independent frameworks that can be used as a single toolchain. Topic 2. will be better defined during the project and might converge in one of the two frameworks or represent a third framework of the chain. Duration 3-4 years.
Innovative/strategic vision	Develop a toolchain for virtual prototyping to: **1-** model detector at high-level **2-** perform architectural studies **3-** provide a reference model for the verification
Performance Target	**Topic 1:** Cluster multiplicity: 1-10 Position resolution: <10 μm Time resolution: 10 ps to 100 ns **Topic 2:** to be defined in M7.2c.2 **Topic 3:** Accuracy: Event/Cycle-level Speed: hundred thousand transactions per second Scalability: readout components library Verification: integrate in verification environment User-Friendly: docs & support for user-only roles
Milestones and Deliverables	**D7.2c.1** (M12) Delivery of a release of the PixESL framework **M7.2c.2** (M12) Target/methodology for Topic 2 **M7.2c.3** (M18) Model Common interface ASIC **D7.2c.4** (M24) Delivery of a release of the detector simulation tool-chain.
Multi-disciplinary, cross-WP content	**Detector Technologies:** support various detector technologies **Particle Physics Models:** integration of comprehensive particle physics models **Geometric Configurations:** ability to define and customize the geometry **Data Formats:** support for common data formats **Monte Carlo Techniques:** implementation of Monte Carlo methods for simulating particle interactions and energy depositions, **Electronics Simulation:** accurate modeling of the readout electronics **Readout Architectures:** support triggered and data-driven systems
Contributors	CERN FR: IPHC Strasbourg *USER:* PSI (CH), UK Cons., INFN Cagliari (IT)
Available resources	3.0 FTE/year 0 kEUR/year
Addt'l resource need	0.0 FTE/year 0 kEUR/year

7 Work Package 7.3: 4D and 5D techniques

High 4D-(timing as well as spatial) resolution requires developing solutions to improve the noise-speed-resolution trade-offs in advanced technologies with low supply voltage and high transistor density, along with achieving an unprecedented precision for the distribution of frequency and time references. Combination with accurate measurement of the energy deposited gives the additional possibility of "5D"-capabilities.
For High-performance sampling (TDC, ADC), high-4D resolution requires a solution to the difficult noise-speed-resolution trade-offs in advanced technologies with low supply voltage and high transistor density;
For High-precision timing, distribution of precise frequency and time references remains vital for all readout systems. The performance of these systems will be pushed to unprecedented levels by 4D sensors, for which distribution is a limiting factor. There are no ready-made solutions at hand, and the challenge is even bigger in radiation environments.

The institutes contributing to WP7.3 and the aggregated Work Package resources are shown in figures 7 and 8 below. The Projects supported by WP7.3 are summarized in sections 7.1, 7.2 and 7.3.

Institutes	WP7.3a	WP7.3b1	WP7.3b2	Projects
AT	**1**			**1**
Graz University of Technology, Institute of Electronics	1			1
Cern		**1**	**1**	**2**
CERN		1	1	2
ES	**1**		**4**	**5**
Centre for Energy, Environmental and Technological Research (CIEMAT)			1	1
Instituto de Física de Cantabria (IFCA)			1	1
Instituto de Microelectrónica de Barcelona (IMB-CNM)			1	1
Instituto Tecnológico de Aragón (ITAINNOVA)			1	1
University of Barcelona-ICCUB	1			1
FR	**4**	**1**	**2**	**7**
Institut Polytechnique de Paris, CNRS-IN2P3, OMEGA	1			1
Laboratoire de Physique de Clermont - LPC		1		1
Université Aix-Marseille, CNRS-IN2P3, CPPM	1		1	2
Université Claude Bernard Lyon 1, CNRS-IN2P3, IP2I	1			1
Université Paris-Saclay, CEA, IRFU	1			1
Université Paris-Saclay, CNRS-IN2P3, IJClab			1	1
KR	**1**			**1**
Daegu Gyeongbuk Institute of Science and Technology (DGIST)	1			1
NL			**1**	**1**
NIKHEF			1	1
PL	**1**			**1**
University of Krakow AGH	1			1
UK			**1**	**1**
University of Bristol			1	1
US	**1**	**1**	**1**	**3**
SLAC National Accelerator Laboratory	1			1
University of Boston		1		1
University of Minnesota			1	1
Projects	**9**	**3**	**10**	**22**

Figure 7: Institutes contributing to WP 7.3

		FTE available				add. FTE needed				funds available [kEUR]				add. funds needed [kEUR]			
7.x.y		2024	2025	2026	>2026	2024	2025	2026	>2026	2024	2025	2026	>2026	2024	2025	2026	>2026
3	a	7.5	7.2	7.2	1.5	6.0	8.0	8.0	4.0	520.0	520.0	435.0	0.0	250.0	265.0	325.0	280.0
3	b1	1.5	1.5	1.5	1.5	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
3	b2	7.2	6.8	4.7	3.6	2.0	3.0	5.6	7.1	162.5	117.5	30.0	10.0	50.0	170.0	265.0	265.0
	total 7.3	**16.2**	**15.5**	**13.4**	**6.6**	**8.0**	**11.0**	**13.6**	**11.1**	**682.5**	**637.5**	**465.0**	**10.0**	**300.0**	**435.0**	**590.0**	**545.0**

Figure 8: Resources overview of WP 7.3

7.1 Project 7.3a

This project aims to develop ultra-low power high performance TDC and ADC blocks for use in a wide range of future particle physics experiments.

Project Name	High performance TDC and ADC blocks at ultra-low power (WP7.3a)
Project Description	Development of high performance, ultra-low power TDC and ADC blocks. Duration 3 years. A further extension is planned after 3 years.
Innovative/strategic vision	Develop high-performance, ultra-low power TDC and ADC blocks in advanced CMOS technologies, ready to be deployed as key components of SoC readout ASICs for a variety of future particle detectors.
Performance Target	High resolution ($\sim$ 10ps) TDC and medium-high resolution (10-14 bits) fast sampling (>40 MSps) ADC blocks. High performance, especially ultra-low power consumption, should be confirmed with a very good Figure of Merit, compared to the state-of-the-art solutions obtained using the same CMOS technology and characterized by similar parameters
Milestones and Deliverables	**M7.3a.1** (M12) Report on design of ADCs and related blocks **M7.3a.2** (M12) Report on design of TDCs and related blocks **M7.3a.3** (M24) Progress report on development of ADCs and related blocks **M7.3a.4** (M24) Progress report on development of TDCs and related blocks **D7.3a.1** (M36) Delivery of prototype ASICs of ADCs and related blocks **D7.3a.2** (M36) Delivery of prototype ASICs of TDCs and related blocks.
Multi-disciplinary, cross-WP content	TDCs and ADCs are common blocks of readout ASICs for wide range of detector systems.
Contributors	AT: TU Graz ES: ICCUB FR: CEA IRFU, CPPM, IP2I, OMEGA KR: DGIST PL: AGH US: SLAC
Available resources	7.3 FTE/yr 500k/yr
Addt'l resource need	7.3 FTE/yr 280k/yr

7.2 Project 7.3b1

This project aims to study and propose generic data-driven calibration strategies for the time measurements in detectors requiring high precision timing. These include simulation, impact studies and data-based calibration strategies of phase variations in all or part of the detector timing distribution tree (for example jumps due to resets in the electronics system and or temperature dependent phase drift), as well as the calibration of the front-end TDC timewalk and non-linearities.

Project Name	Strategies for characterizing and calibrating sources impacting time measurements (WP7.3b1)
Project Description	Generic data-driven impact studies and calibration strategies of phase variations for timing detectors. Duration 3 years.
Innovative/strategic vision	First opportunity to have a common strategy between the different experiments for data-driven timing studies.
Performance Target	Design of a protocol of measurement. Development of simulation tools in the different experiments. Definition of common figures of merit. Measurement of the properties in test facilities to compare with the predictions. Design of calibration chain inside the different experiments.
Milestones and Deliverables	**D7.3b1.1** (M12) Delivery of a report summarising common metrics and description of the effects for simulation **M7.3b1.1** (M24) Implementation of measurements on realistic DAQ chain **D7.3b1.2** (M36) Delivery of a report summarising the items (hardware or software) to be improved for the next generation of experiments.
Multi-disciplinary, cross-WP content	Concerns all state-of-the-art timing detectors and therefore requires a unified approach which is proposed by this project. Reciprocal reports with DRD7.3a & 7.3b2
Contributors	CERN: ATLAS HGTD, CMS HGCAL FR: Université Clermont Auvergne. CNRS-IN2P3, LPCA (ATLAS HGTD) US: Boston University (CMS ETL)
Available resources	1.5 FTE/yr (ATLAS & CMS core funds) 0 kEUR[1]
Addt'l resource need	0 FTE 0 kEUR[1]

[1] The teams will have full access to simulation processors, detector simulation data & test-benches

7.3 Project 7.3b2

This project aims to study and propose strategies to optimize and assess ultimate precision and determinism of timing distribution systems for future detectors. The precision target of upcoming timing detectors is now enforcing new figures of merit to be taken into account in addition to the traditional random jitter, such as clock phase stability and determinism (at picosecond level). Such metrics are systems- and COTS-specific and need to be carefully assessed. In addition, generic solutions shall be provided to mitigate the various kinds of instabilities brought by the selected components. This project will be carried out in tight collaboration with its counterpart project based on simulation (7.3b1): Strategies for characterizing and calibrating sources impacting time measurements.

Project Name	Timing Distribution Techniques (WP7.3b2)	
Project Description	Bench-marking of the performance of COTS- or custom-based solutions to assess achievable timing precision and determinism. Investigation of generic solutions to mitigate the observed limitations.	
Innovative/strategic vision	Common effort of the community to explore limits of COTS and reach ambitious timing precision not targeted by commercially available solutions	
Performance Target	Develop and compare implementations on different COTS and custom platforms. Studies and implementation of FPGA-agnostic or ground-breaking solutions to improve phase stability.	
Milestones and Deliverables	**M7.3b2.1** (M12) Specification for a light-weight timing and synchronization protocol also capable of passing fixed latency messages **D7.3b2.2** (M18) Deliver a report comparing the phase determinism of various FPGAs (PolarFire, Agilex, Versal) and potential mitigation mechanisms **D7.3b2.3** (M18) Delivery of first demonstrators of the light-weight protocol, and of a generic deterministic link based on AMD FPGAs and DDMTD + DCPS ASICs from University of Minnesota **M7.3b2.2** (M18) Submission of a unique chip for Phase Monitoring and Phase Shifting (PMPS) **D7.3b2.4** (M24) Delivery of a report on White Rabbit for 4D detectors and for Agilex FPGA **D7.3b2.5** (M36) Delivery of a report summarising a proof of concept demonstration of a FPGA-Agnostic Cascaded Link (FACL) with PMPS ASIC.	
Multi-disciplinary, cross-WP content	Distribution is critical and universal to all detectors requiring timing. DRD7.3b1 and 7.3b2 will feed each other with simulation and assessed figures	
Contributors	CERN: HPTD team ES: CIEMAT, ITAINNOVA, CSIC (IFCA & IMB-CNM) FR: IN2P3 (CPPM, IJCLab) UK: Bristol University NL: Nikhef USA: The University of Minnesota	
Available resources	18.7 FTE over 3 years	310 kEUR over 3 years
Addt'l resource need	10.6 FTE over 3 years	485 kEUR over 3 years

8 Work Package 7.4: Extreme environments

Future technologies will need to cope with extreme environments and required longevity:
Cryogenic conditions: Cryogenic detectors offer high sensitivity and resolution for future neutrino and dark matter experiments, but are challenging for the operation of microelectronics. Readout of new sensor types (some operating at mK) requires thorough characterisation and modelling of ASIC technologies, exploration of new data transfer concepts, development of multiplexing technologies, and novel readout and control;
Radiation-hardness: In future particle physics experiments, particularly at energy-frontier colliders, particle fluences are extreme. ASICs, optoelectronics, powering devices, and on- or near-detector FPGAs must be designed and qualified for radiation-hardness;
Cooling: Sub-detector systems may consume tens or hundreds of kilowatts, predominantly in the front-end ASICs. At the same time sensors must be cooled to minimise leakage current and noise and to avoid thermal runaway. Critical technologies are micro-channels in silicon and novel heat-conducting materials.

The institutes contributing to WP7.4 and the aggregated Work Package resources are shown in figures 9 and 10 below. The Projects supported by WP7.4 are summarized in sections 8.1, 8.2 and 8.3.

Institutes	WP7.4a	WP7.4b	WP7.4c	Projects
AT	**1**	**1**		**2**
Graz University of Technology, Institute of Electronics	1	1		2
CA	**1**			**1**
Sherbrooke University	1			1
Cern		**1**		**1**
CERN		1		1
CH	**1**			**1**
EPFL	1			1
DE	**1**		**1**	**2**
Deutsches Elektronen-Synchrotron (DESY)			1	1
Forschungszentrum Jülich	1			1
ES	**1**		**2**	**3**
Instituto de Física Corpuscular (IFIC) Valencia			1	1
Instituto de Microelectrónica de Barcelona (IMB-CNM)			1	1
University of Barcelona-ICCUB	1			1
FR		**1**	**5**	**6**
Laboratoire d'Annecy de Physique des Particules (LAPP)			1	1
Laboratoire de physique nucléaire et de hautes énergies (LPNHE)			1	1
Univeristy Grenoble Alpes, CNRS, LEGI			1	1
Université Aix-Marseille, CNRS-IN2P3, CPPM		1	1	2
Université Grenoble Alpes, CNRS-IN2P3, LPSC			1	1
IT	**1**	**2**		**3**
INFN Torino	1			1
Università di Padova		1		1
University of Bergamo / INFN Pavia / University of Pavia		1		1
JP	**1**			**1**
KEK, High Energy Accelerator Research Organization	1			1
UK	**2**		**1**	**3**
University of London Royal Holloway	1			1
University of Manchester			1	1
University of Oxford; Rutherford Appleton Laboratory	1			1
US	**1**			**1**
Fermilab National Laboratory (FNAL)	1			1
Projects	**10**	**5**	**9**	**24**

Figure 9: Institutes contributing to WP 7.4

7.x.y		FTE available				add. FTE needed				funds available [kEUR]				add. funds needed [kEUR]			
x	y	2024	2025	2026	>2026	2024	2025	2026	>2026	2024	2025	2026	>2026	2024	2025	2026	>2026
4	a	6.6	5.1	4.6	3.0	4.0	7.5	7.5	7.5	48.0	50.0	40.0	20.0	110.0	191.0	251.0	140.0
4	b	4.1	3.4	2.0	1.5	2.0	2.0	3.3	3.3	124.0	169.0	20.0	50.0	45.0	65.0	205.0	205.0
4	c	7.7	6.1	5.1	1.0	0.5	4.0	7.0	4.5	102.0	83.0	0.0	0.0	90.0	205.0	275.0	240.0
	total 7.4	**18.4**	**14.6**	**11.7**	**5.5**	**6.5**	**13.5**	**17.8**	**15.3**	**274.0**	**302.0**	**60.0**	**70.0**	**245.0**	**461.0**	**731.0**	**585.0**

Figure 10: Resources overview of WP 7.4

8.1 Project 7.4a

The project will focus on cryogenic device modelling from selected CMOS technology nodes, the development of "cold" Process Design Kits (PDKs) and mixed-signal CMOS IP blocks and mixed-signal demonstrator chips for cryogenic operation.

Project Name	Device modelling and Development of Cryogenic CMOS PDKs and IP (WP7.4a)
Project Description	Device modelling from selected CMOS technology nodes, development of "cold" Process Design Kits (PDKs), design and characterisation of mixed-signal CMOS IP blocks and demonstrator chips for photon detection in (LAr, LXe) noble liquid experiments, quantum computing interface and sensing.
Innovative/strategic vision	The aggregation of the international research teams will create the critical mass needed for the construction of infrastructures and tools, needed for device characterisation and modelling , towards the development of cold PDKs and cold-IP blocks. These will be made available to a wider community working towards the construction of frontier particle and photon cryogenic detectors.
Performance Target	cold PDK for a deep sub-micron CMOS technology, with temperature corners at 165-87-77-4K, cold IP blocks demonstrated on board of a multi-channel mixed-mode demonstrator chip.
Milestones and Deliverables	**D7.4a.1** (M9) Deliever a specification and requirements document for a full-chip demonstrator. **M7.4a.2** (M18) Cold-PDK for TSMC28nm complete **M7.4a.3** (M26) Tapeout of full-demonstrator chip **D7.4a.4** (M38) Deliver a report of full-demonstrator silicon chip characterisation.
Multi-disciplinary, cross-WP content	The availability of reliable device models and PDKs for advanced CMOS technology nodes, qualified for operation at cryogenic temperatures, will pave the way for the development of cryo-qualified CMOS IP blocks suitable for integration on complex mixed-signal ASICs for DRD2 and DRD5.
Contributors	Graz University of Technology (Austria) University of Sherbrooke (Canada) Forschungszentrum Jülich (Germany) INFN (Italy) KEK (Japan) ICCUB, University of Barcelona (Spain) EPFL (Switzerland) RHUL (UK) University of Oxford (UK) Fermilab (US)
Available resources	5.4 FTE/yr 46k/yr
Addt'l resource need	6.3 FTE/yr 184k/yr

8.2 Project 7.4b

This project investigates the radiation response of CMOS technologies from the 28nm node onward for use in the next generations of ASICs for particle detectors.

Project Name	Radiation Resistance of Advanced CMOS Nodes (WP7.4b)
Project Description	This project aims to evaluate the radiation response (total ionizing dose TID, single event effects SEE, and displacement damage DD) of commercial CMOS technologies more advanced than the 65nm node for use in the next generations of ASICs for particle detectors. Duration 4-5 years.
Innovative/strategic vision	Understanding the effects of radiation on CMOS technologies is essential for the design of ASICs used in particle detectors. This project represents a first and crucial step in evaluating the performance of advanced CMOS nodes for the unique environment of particle detectors.
Performance Target	Deepen the knowledge of the radiation response of 40nm and 28nm technologies and begin to study finFETs technologies.
Milestones and Deliverables	**D7.4b.1** (M12) Deliver a 28nm CMOS front-end (FE) circuits for pixel sensors prototype; TID test of IP-blocks in 28nm node **D7.4b.2** (M18) Deliver a chip in 28nm CMOS including matrices of FE channels for readout of pixel sensors **M7.4b.3** (M24) Radiation test of FE structures; Design and testing of rad-hard memory elements in 28nm node **D7.4b.4** (M36) Deliver a prototype in FinFET technology including IP blocks for pixel readout circuits.
Multi-disciplinary, cross-WP content	In order to ensure the success of projects involving ASIC design for particle detectors, it is imperative to consider the radiation resistance of the technologies used. On the other hand, the definition of radiation qualification would greatly benefit from the input of the designer. For example, ASICs developed in WP7.3a must be radiation tolerant and could also serve as valuable test vehicles to evaluate radiation effects.
Contributors	CERN AT: TU Graz IT: INFN Pavia, Uni. Bergamo, Uni. Padova, Uni. Pavia FR: CPPM
Available resources	3.2 FTE/yr 104k/yr
Addt'l resource need	2.4 FTE/yr 105k/yr

8.3 Project 7.4c

This project focuses on the development of the next generation of cooling plates for front-end electronics and sensors based on different materials/techniques. The main goal is to explore manufacturing techniques while improving electronics integration with a cost-effective solution.

Note that depending on the evolution of the forming DRD8 Collaboration, some cooling-related projects may be best integrated in DRD8. This will be fine tuned in due-time to best match the needs of the projects.

Project Name	Cooling and cooling plates (WP7.4c)
Project Description	Development of the general purpose next generation of microchannels cooling structures to deliver excellent cooling performance, minimal material budget, and better electronics integration. Duration about 2+ years.
Innovative/strategic vision	Better integration of electronics features to the cooling plates especially in dense electronics applications. Better scalability considering alternative manufacturing techniques (more cost-effective). Thermal performance numerical simulation tools for new applications.
Performance Target	Different topics will explore different combinations of the following parameters: power dissipation (up to $2\mathrm{W/cm}^2$), material budget ($\leq 0.5\%X_0$), integration and/or cost. Different experiments will be able to profit from the portfolio created and optimize those solutions for their final application. The progress will be tracked via public reports in the form of presentations, public notes and/or papers.
Milestones and Deliverables	**D7.4c.3** (M15) Deliver a feasibility public note or paper (topic 3) **M7.4c.6** (M24) 3D printing public note or paper (topic 4) **D7.4c.5** (M27) Deliver a report summarising fluidic and thermal tests of demonstrators public note or paper (topic 1) **M7.4c.7** (M36) Bi-phase CO2 Thermo-fluidic models developed for microchannel, nuclear and annular flows, and thermal heat exchanger characterization and interconnection (topic 2).
Multi-disciplinary, cross-WP content	Communication with DRD8 (Mechanics) and DRD3 (Semiconductor detectors) via liaisons and workshops (e. g.: Forum on tracking mechanics) and 7.6b project (common access 3D and advanced integration) within the DRD7.
Contributors	CA: Sherbrooke CERN DE: DESY ES: IMB-CNM, IFIC-Valencia UK: Manchester FR: CPPM, LAPP, LEGI, LPNHE, LPSC
Available resources	7.7 FTE/yr (First year), 102k/yr (First year)
Addt'l resource need	7.0/yr (Largest, on 2026), 275k/yr (Largest, on 2026)

9 Work Package 7.5: Backend systems and commercial-off-the-shelf components

Keeping pace with, adapting, and interfacing with COTS is mandatory when developing the back-end of a state of the art electronic system: COTS computing (CPUs, GPGPUs, FPGAs, AI accelerators) and networking equipment increases performance at breathtaking pace. Since it is targeted mostly at cloud data centres, use in HEP requires adaptation and integration both at the hardware and software level. This is challenging work which needs to be repeated for every new generation of COTS;
With the trend of developing more intelligent front-ends, a possibility opens up to configure front-end ASICs to interface directly with COTS hardware at the backend. This new paradigm must be carefully investigated and compared to the traditional development of custom backend boards.

The institutes contributing to WP7.5 and the aggregated Work Package resources are shown in figures 11 and 12 below. The Projects supported by WP7.5 are summarized in sections 9.1, and 9.2. Project 7.5c (generic backend) is not yet ready for submission and may be added to the portolio in a future round.

Institutes	WP7.5a	WP7.5b	Projects
Cern		**1**	**1**
CERN		1	1
CH	**1**		**1**
University of Geneva, DPNC	1		1
ES	**3**		**3**
Centre for Energy, Environmental and Technological Research (CIEMAT)	1		1
Instituto de Física Corpuscular (IFIC) Valencia	1		1
Universidad de Oviedo	1		1
FR		**1**	**1**
Université Aix-Marseille, CNRS-IN2P3, CPPM		1	1
NL		**1**	**1**
NIKHEF		1	1
UK	**6**	**3**	**9**
Imperial College		1	1
Queen Mary University of London (QMUL)	1		1
UKRI-STFC Rutherford Appleton Laboratory (RAL)	1	1	2
University College London (UCL)	1		1
University of Birmingham	1		1
University of Bristol	1	1	2
University of Manchester	1		1
US		**1**	**1**
Brookhaven National Laboratory (BNL)		1	1
Projects	**10**	**7**	**17**

Figure 11: Institutes contributing to WP 7.5

7.x.y		FTE available				add. FTE needed				funds available [kEUR]				add. funds needed [kEUR]			
x	y	2024	2025	2026	>2026	2024	2025	2026	>2026	2024	2025	2026	>2026	2024	2025	2026	>2026
5	a	6.7	6.9	5.9	0.0	1.8	2.3	3.3	0.0	33.0	33.0	33.0	0.0	123.0	123.0	123.0	0.0
5	b	3.9	3.4	2.4	1.0	3.5	5.0	5.5	7.5	37.5	32.5	0.0	0.0	10.0	95.0	80.0	80.0
5	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	total 7.5	**10.6**	**10.3**	**8.3**	**1.0**	**5.3**	**7.3**	**8.8**	**7.5**	**70.5**	**65.5**	**33.0**	**0.0**	**133.0**	**218.0**	**203.0**	**80.0**

Figure 12: Resources overview of WP 7.5

9.1 Project 7.5a

The DAQOverflow project aims to provide a benchmark of heterogeneous COTs architectures alongside a open-access, repository-hosted infrastructure and set of commonly used tools and algorithms that will keep pace with evolving COTs technologies (GPU, CPU and FPGA coprocessor farms) for the purpose of cost- and performance considered near-detector, near-real-time backend processing for HEP experiments.

Project Name	DAQOverflow (WP7.5a)
Project Description	Benchmarking of heterogeneous COTs architectures and development of TDAQ tools and algorithms distributed via a common repository that are up-to-date with evolving COTs technologies for cost- and performance-considered near-detector/real-time backend processing.
Innovative/strategic vision	Identify experiment-agnostic common TDAQ activities, define generic benchmarks to allow easy comparison of cost/energy efficiency for various compute architectures for the purposes of backend/trigger processing. Make generic algorithms / tools available for various architectures as a repository of 'best practice'.
Performance Target	Cost- and performance-evaluated figures of merit (cost/energy per unit of work), mutil-disciplinary deliverables (kept up-to-date for newer generations of hardware) and distributed reference implementations and examples through a documented common repository of firmware and software. The target after three years is a community-driven, growing project of development with appropriate funding mechanism from the work package and interested users to re-benchmark for new hardwares/technologies when needed.
Milestones and Deliverables	**D7.5a.1** (M9) Delivery of first reference implementations of workflows on simpler platforms **D7.5a.2** (M12) Delivery of a repository and documentation with format agreed upon, reference implementations hosted **D7.5a.3** (M24) Delivery of reference implementations of workflows for a full suite of ASIC/CPU/GPU delivered **D7.5a.4** (M30) Delivery of the benchmarking for full suite, documented and published **D7.5a.5** (M33) Delivery of any followup benchmarks using improved algorithms on existing hardware and first benchmarks on next-gen hardware **D7.5a.6** (M36) Delivery of any comparative performance studies between previous and current generation hardware published.
Multi-disciplinary, cross-WP content	Commodity TDAQ hardware is cross-experiment in nature. The outcomes will be transverse to much of the DRD program for specific DAQ considerations.
Contributors	Instituto de Física Corpuscular (IFIC) Valencia, University College London, University of Birmingham, University of Bristol, Rutherford Appleton Laboratory, University of Geneva, Universidad de Oviedo, University of Manchester
Available resources	$\sim$ 6.5 FTE/yr $\sim$ 30kEUR/yr
Addt'l resource need	$\sim$ 2.5 FTE/yr $\sim$ 125kEUR/yr

9.2 Project 7.5b

The perspective of future HEP experiments with lower radiation levels than typically seen at LHC opens the door to increasing the complexity of Front-End electronics, implementing for example RISC-V based processors and SoC in the Front-End. In this context, high throughput 100GbE-based data readout link can reasonably be envisaged. This is a new paradigm which will be investigated in this DRD7.5 Project. It will be tightly linked to other Working Groups like DRD7.2/RISC-V or DRD7.1/links activities.

Project Name	From Front-End to Back-End with 100GbE (WP7.5b)
Project Description	Develop full 100Gb Ethernet-based solutions for Data Readout links from Front-End to DAQ.
Innovative/strategic vision	Lower radiation levels and higher data throughput in future detectors open the door to envisage and investigate 100GbE-based data readout links.
Performance Target	Design and performance comparison between network demonstrators of 100GbE networks based on specific protocol designs, configurations of COTS and potentially customized switches.
Milestones and Deliverables	**M7.5b.1** (M12) Delivery of a report on generic implementation of standard 100GbE on current custom Back-End boards **D7.5b.1** (M12) Delivery of a demonstrator of a FEC-based asymmetric 100GbE link with lpGBT **M7.5b.2** (M18) Specifications for a Macrocell for potential future 100GbEFront-End ASICs **D7.5b.2** (M18) Delivery of smart switch specifications (document) and prototype, including a paper submission and a gitlab repository - Theme 2 **D7.5b.3** (M24) Delivery of demonstrators of a full 100GbE system **D7.5b.4** (M24) Delivery of first prototype test ASIC including protocol IPs and test report. **M7.5b.3** (M36) Full report with conclusion on feasibility of 100GbE-based readout links for Front-End of future detectors
Multi-disciplinary, cross-WP content	Universal across HEP for detectors requiring high/concentrated data readout bandwidth. Tightly linked to other WP like DRD7.2/RISC-V or DRD7.1/links activities
Contributors	CERN FR: CPPM CNRS/IN2P3 NL: Nikhef UK: Bristol University[1], Imperial College, Rutherford Lab US: Brookhaven National Lab[1]
Available resources	9.7 FTE over 3 years 70k over 3 years
Addt'l resource need	14 FTE over 3 years 185k over 3 years

[1] The participation of this institute in the project depends on the success of the request for funds made at the end of 2023.

10 Work Package 7.6: Complex imaging ASICs and technologies

Working Group 6 deals with complex technologies merging multiple functionalities such as sensor and processing, or multi-tier (2.5D and 3D) assemblies. Accessing and mastering these processes is typically beyond the reach of individual institutes, and only a collaborative effort will enable harnessing their benefits.

The institutes contributing to WP7.6 and the aggregated Work Package resources are shown in figures 13 and 14 below. The Projects supported by WP7.6 are summarized in sections 10.1, and 10.2.

Institutes	WP7.6a	WP7.6b	Projects
CA		**1**	**1**
Sherbrooke University		1	1
Cern	**1**		**1**
CERN	1		1
DE		**3**	**3**
Fachhochschule Dortmund		1	1
Karlsruhe Institute of Technology (KIT)		1	1
MPG HLL		1	1
FR	**4**		**4**
Laboratoire de physique nucléaire et de hautes énergies (LPNHE)	1		1
Université Aix-Marseille, CNRS-IN2P3, CPPM	1		1
Université Claude Bernard Lyon 1, CNRS-IN2P3, IP2I	1		1
Université de Strasbourg, CNRS-IN2P3, IPHC	1		1
IT	**1**		**1**
INFN-Arcadia project, represented by INFN Torino	1		1
NL	**1**		**1**
NIKHEF	1		1
NO	**1**	**1**	**2**
Norwegian Institutes (UiB, UiO, USN) represented by University of Bergen (UiB)	1	1	2
UK	**1**		**1**
UKRI-STFC Rutherford Appleton Laboratory (RAL)	1		1
US	**1**		**1**
SLAC National Accelerator Laboratory	1		1
Projects	**10**	**5**	**15**

Figure 13: Institutes contributing to WP 7.6

7.x.y		FTE available				add. FTE needed				funds available [kEUR]				add. funds needed [kEUR]			
x	y	2024	2025	2026	>2026	2024	2025	2026	>2026	2024	2025	2026	>2026	2024	2025	2026	>2026
6	a	21.5	21.5	21.5	21.0	6.5	6.5	6.5	6.5	80.0	700.0	230.0	595.0	0.0	0.0	0.0	0.0
6	b	5.5	5.5	5.5	5.5	3.0	3.0	3.0	3.0	374.6	393.3	393.3	393.3	68.0	68.0	68.0	68.0
	total 7.6	**27.0**	**27.0**	**27.0**	**26.5**	**9.5**	**9.5**	**9.5**	**9.5**	**454.6**	**1093.3**	**623.3**	**988.3**	**68.0**	**68.0**	**68.0**	**68.0**

Figure 14: Resources overview of WP 7.6

10.1 Project 7.6a

This project aims to provide common access to advanced imaging technologies through the organization of common fabrication runs. These are initially envisaged for the TowerJazz 180 nm, TPSCo 65 nm ISC, and the LFoundry 110 nm CMOS imaging technologies. These will be accessible for different clients in the community, among which the other DRDs like DRD3, experiments and projects in HEP. Assembly of the reticle for the different runs is foreseen, as well as design support for the PDK, development of special design rules, TCAD support for sensor optimization and interfacing to the foundry. IP development is also foreseen to accelerate and streamline the design effort. Continuation of this common access beyond the initial three years is expected. Synergy with the 7.6b 3D development will be explored possibly with already existing chips or chiplets. Full 3D-stacked runs, offered in all three technologies, may possibly be pursued later.

Project Name	Common Access to Selected Imaging Technologies (WP7.6a)
Project Description	Provide common access and centralized support for selected CMOS imaging technologies, including specific IP development to accelerate the design effort. Duration 3 years, expected to be extended.
Innovative/strategic vision	Potential of monolithic technologies, confirmed by successful ALICE ITS2 tracker and the widespread community interest. Efficient and affordable technology access requires concentration of the resources in the community.
Performance Target	Organize common runs and efficient and cost-effective access to selected technologies.
Milestones and Deliverables	***TPSCo 65 nm ISC:*** **M7.6a.1a** (M12) Completion of IP specifications **M7.6a.2a** (M18) First version of IP complete **D7.6a.1a** (M24) Delivery of a report summarising a foundry submission Q4 2025 **M7.6a.3a** (M36) Documentation of IP for common use ***TJ 180 nm (submissions subject to demand):*** **M7.6a.1b** (M12) Completion of IP specifications **M7.6a.2b** (M18) First version of IP complete **D7.6a.1b** (M24) Delivery of a report summarising a foundry submission Q4 2025 **M7.6a.3b** (M36) Documentation of IP for common use ***LF110 nm:*** **D7.6a.1c** (M24) Delivery of a report summarising a foundry submission Q4 2025 **D7.6a.2c** (M36) Delivery of a report summarising a foundry submission Q2 2026
Multi-disciplinary, cross-WP content	Concerns several detectors types, calorimeters, tracking, etc. Serves other DRDs like DRD3 and DRD6, experiments and projects in HEP. Strong connection with 7.6b (e.g. 3D integration of chiplets). Requires expertise in analog and digital IC design, device design and technology, and significant testing effort.
Contributors	CH: CERN FR: IN2P3: CPPM, IPHC, IP2I + others IT: INFN(TO, TIFPA, MI, BO, PD, PV, PG, PI) NL: NIKHEF NO: UiB, UiO and USN UK: STFC US: TBC, SLAC already doing effort
Available resources	TPSCo 65nm 12 FTE/yr 290k/yr TJ 180 nm 1.5 FTE/yr 20k/yr LF 110 nm is 8 FTE/yr 100 k/yr
Addt'l resource need	6.5FTE/yr 410k/yr (TBD)

10.2 Project 7.6b

This project aims to develop essential technologies for both 2.5D and 3D integration that can be quickly transposed to wafer-to-wafer 3D integration for a wide range of future particle physics applications, ranging from low-temperature neutrino detectors to high-radiation environment HL-HLC pixel detectors. Synergy with the 7.6a will be explored by employing either already existing chips or dedicated test structures. Furthermore, 3D-integration technologies are evolving quickly in industry. Therefore, exploring concrete connections with industrial partners is a key mission of the project.

Project Name	Shared Access to 3D Integration (WP7.6b)
Project Description	Develop advanced chiplet and 3D integration technologies, including the integration of SiPh chips on detector, by in-house infrastructures and third-party vendors. Initial duration of 3 years with potential for further prolongation beyond.
Innovative/strategic vision	Potential of silicon interposer and chiplet technologies. In-house infrastructure for quick production of prototypes/demonstrators and test vehicles, by employing bump-bonding and detector packaging technologies already available. To establish a concrete connection with the industrial partners.
Performance Target	Shared competences/experiences and infrastructures/processes. Build up and maintain the capability for a quickly transposed to 3D integration. Keeping a cost-effective access to selected technologies.
Milestones and Deliverables	**M7.6b.1** (M18) Establish TSVs process on Si interposer and dummy wafers **M7.6b.2** (M24) Establish RDL process on Si dummy structures **D7.6b.1** (M30) Delivery of report summarasing the integration of SiPh on detector by 2.5D interposer/chiplet technologies **D7.6b.2** (M30) Delivery of a report on W2W bonding by industrial partners **D7.6b.3** (M36) Deliver documentation of the process for the common use.
Multi-disciplinary, cross-WP content	Strong connection with 7.1 for the integration of SiPh chip and optical fiber on detector module. Strong connection with 7.6a (e.g. 3D integration/chiplets).
Contributors	CA: Sherbrooke DE: MPG-HLL, FH Dortm. KIT NO: Norwegian Institutes (Uni. of Bergen (UiB), Uni. of Oslo (UiO), and Uni. of Southeast Norway (USN)) US: Fermilab (TBC)
Available resources	5.5 FTE/yr 390k/yr
Addt'l resource need	3 FTE/yr 68 k/yr

11 Working Group 7.7: Tools and technologies

The efficient delivery of the common technical goals in the area of electronics, and the strategic recommendations of the Road-map both demand that the community collectively conform to a portfolio of practices, standards and tools to enable professional and efficient collaboration.

This need is particularly acute for micro-electronics technologies, where the complexity and cost of development are extremely high and continue to increase for every new generation. The issue has been highlighted in recent years where several critical path ASIC developments for experiments have not delivered as expected. This has delayed upgrades and escalated costs with systems often requiring multiple additional foundry cycles. The particle physics community need to address this and ensure as far as is practicable that production ASIC developments deliver solutions that are robust and ready for manufacture whilst also harnessing the full potential of the wider community.

With the current deep submicron technologies, ASIC development is now a major endeavour requiring a wide skillset that many small design groups cannot deliver alone. This has left many projects exposed to greater risk of design failures than in the past. Given the number of projects and the breadth of the R&D programme taking shape under the auspices of the DRD collaborations, taking such a risk in the future is now unaffordable and unacceptable: for new large and complex ASIC developments, smaller groups will need to partner with experienced centres that possess, or have access to, the necessary expertise and tools to ensure successful submissions.

The access to semiconductor technologies that is required for future projects is also subject to strict legal control measures that are rigorously enforced by both the semiconductor manufacturers and the EDA software tool providers in a way that's intended to protect their business interests. These controls, along with strict end-use restrictions, export controls and taxation issues further complicate the situation. While these restrictions have not prevented ASIC design collaborative work and IP sharing with the right agreements in place, the community will benefit from making this process as lightweight and efficient as possible for the future.

In response to the above concerns, and in order to manage ASIC-related design risks in our distributed community, the Steering Committee invites Conveners of WG7.7 to create and steer a task force that will propose an **implementation solution for a Hub-based structure for ASICs developments in the HEP community**.

The Terms Of Reference for the task force will be:

- To establish and maintain access, for the DRD community, to state-of-the art microelectronics technologies and EDA software tools through regional collaboration and coordination (the Hubs)
- To ensure a professional approach to prototyping and production fabrication cycles by delivering best practice in design, verification and foundry submission
- To facilitate collaborative work across distributed design teams establishing the necessary infrastructure for IP block sharing, and
- To ensure that projects follow rigorous project review and submission processes to manage risks and control changes in projects

The ambition will be to be as inclusive as possible, the scope of the EDA tool provision will build on the successful Europractice model. It's extension will be evaluated on a case-by-case basis taking into account existing agreements and other possible restrictions.

More details on the proposed hub-based model can be found in appendix B.

References

[1] DRD7 steering committee. Letter of Intent DRD7: R&D Collaboration for Electronic Systems. Technical report, Geneva, September 2023.

[2] ECFA Detector R&D Roadmap Process Group. The 2021 ECFA detector research and development roadmap. Technical report, Geneva, 2020.

A Appendix A: Detailed list of contributors to work packages and projects, per country and institute

Country	Institute	Email address	1			1 Total	2		2 Total	3			3 Total	4			4 Total	5		5 Total	6		6 Total	Grand Total
			WP7.1a	WP7.1b	WP7.1c		WP7.2b	WP7.2c		WP7.3a	WP7.3b1	WP7.3b2		WP7.4a	WP7.4b	WP7.4c		WP7.5a	WP7.5b		WP7.6a	WP7.6b		
AT	Graz University of Technology, Institute of Electronics	alicja.michalowska@tugraz.at		1		1				1			1	1	1		2							4
AT Total				1		1				1			1	1	1		2							4
BE	KU Leuven	levi.marien@kuleuven.be					1		1															1
BE Total							1		1															1
CA	Sherbrooke University	serge.charlebois@usherbrooke.ca	1			1								1			1					1	1	3
CA Total			1			1								1			1					1	1	3
Cern	CERN	francois.vasey@cern.ch	1	1		2	1	1	2		1	1	2		1		1		1	1	1		1	9
Cern Total			1	1		2	1	1	2		1	1	2		1		1		1	1	1		1	9
CH	EPFL	edoardo.charbon@epfl.ch												1			1							1
	University of Geneva, DPNC	anna.sfyrla@cern.ch																1		1				1
CH Total														1			1	1		1				2
DE	Bergische Universitaet Wuppertal	wagner@uni-wuppertal.de	1			1																		1
	Deutsches Elektronen-Synchrotron (DESY)	christian.reckleben@desy.de	1			1										1	1							2
	Fachhochschule Dortmund	michael.karagounis@fh-dortmund.de		1		1	1		1													1	1	3
	Forschungszentrum Jülich	A.Zambanini@fz-juelich.de												1			1							1
	Karlsruhe Institute of Technology (KIT)	frank.simon@kit.edu	1			1																1	1	2
	MPG HLL	lca@hll.mpg.de																				1	1	1
	RWTH Aachen University, Physics Institute IB	feld@physik.rwth-aachen.de		1		1																		1
DE Total			3	2		5	1		1					1		1	2					3	3	11
EE	Tallinn University of Technology (TalTech)	andrii.chub@taltech.ee		1		1																		1
EE Total				1		1																		1
ES	Centre for Energy, Environmental and Technological Research (CIEMAT)	cristina.fernandez@ciemat.es										1	1					1		1				2
	Galician Institute of High Energy Physics (IGFAE)	antonio.fernandez.prieto@cern.ch	1			1																		1
	Instituto de Física Corpuscular (IFIC) Valencia	Arantza.Oyanguren@ific.uv.es														1	1	1		1				2
	Instituto de Física de Cantabria (IFCA)	ivan.vila@csic.es										1	1											1
	Instituto de Microelectrónica de Barcelona (IMB-CNM)	miguel.ullan@imb-cnm.csic.es										1	1			1	1							2
	Instituto Tecnológico de Aragón (ITAINNOVA)	farteche@itainnova.es		1		1						1	1											2
	Universidad de Oviedo	santiago.folgueras@cern.ch																1		1				1
	University of Barcelona-ICCUB	dgascon@fqa.ub.edu								1			1	1			1							2
ES Total			1	1		2				1		4	5	1		2	3	3		3				13
FR	CEA-LETI	cedric.dehos@cea.fr			1	1																		1
	Institut Polytechnique de Paris, CNRS-IN2P3, OMEGA	taille@in2p3.fr								1			1											1
	Laboratoire d'Annecy de Physique des Particules (LAPP)	Pierre.Delebecque@lapp.in2p3.fr														1	1							1
	Laboratoire de Physique de Clermont - LPC	lderamo@cern.ch									1		1											1
	Laboratoire de physique nucléaire et de hautes énergies (LPNHE)	giovanni.calderini@lpnhe.in2p3.fr														1	1				1		1	2
	Univeristy Grenoble Alpes, CNRS, LEGI	damien.colombet@univ-grenoble-alpes.fr														1	1							1
	Université Aix-Marseille, CNRS-IN2P3, CPPM	legac@cppm.in2p3.fr								1		1	2		1	1	2		1	1	1		1	6
	Université Claude Bernard Lyon 1, CNRS-IN2P3, IP2I	d.contardo@ipnl.in2p3.fr								1			1								1		1	2
	Université de Strasbourg, CNRS-IN2P3, IPHC	jerome.baudot@iphc.cnrs.fr						1	1												1		1	2
	Université Grenoble Alpes, CNRS-IN2P3, LPSC	fmalek@lpsc.in2p3.fr			1	1										1	1							2
	Université Paris-Saclay, CEA, IRFU	florent.bouyjou@cea.fr								1			1											1
	Université Paris-Saclay, CNRS-IN2P3, IJCLab	daniel.charlet@ijclab.in2p3.fr										1	1											1
FR Total					2	2		1	1	4	1	2	7		1	5	6		1	1	4		4	21
IL	Tel-Aviv University	Yan.Benhammou@cern.ch			1	1																		1
IL Total					1	1																		1
IT	INFN Pisa	Fabrizio.Palla@cern.ch	1		1	2																		2
	INFN Torino	darochar@to.infn.it												1			1							1
	INFN-Arcadia project, represented by INFN Torino	darochar@to.infn.it																			1		1	1
	Scuola Superiore Sant'Anna Pisa	claudio.oton@santannapisa.it	1		1	2																		2
	Università degli Studi di Milano and INFN Sezione di Milano	attilio.andreazza@mi.infn.it	1	1		2																		2
	Università di Padova	piero.giubilato@unipd.it													1		1							1
	University of Bergamo / INFN Pavia / University of Pavia	luigi.gaioni@unibg.it													1		1							1
	University of Trento	philippe.velha@unitn.it	1			1																		1
	University of Udine	stefano.saggini@uniud.it		1		1																		1
IT Total			4	2	2	8								1	2		3				1		1	12
JP	KEK, High Energy Accelerator Research Organization	kisisita@post.kek.jp												1			1							1
JP Total														1			1							1

Figure 15: Contributors to DRD7 (part 1 of 2)

Country	Institute	Email address	1			1 Total	2		2 Total	3			3 Total	4			4 Total	5		5 Total	6		6 Total	Grand Total
			WP7.1a	WP7.1b	WP7.1c		WP7.2b	WP7.2c		WP7.3a	WP7.3b1	WP7.3b2		WP7.4a	WP7.4b	WP7.4c		WP7.5a	WP7.5b		WP7.6a	WP7.6b		
KR	Daegu Gyeongbuk Institute of Science and Technology (DGIST)	gain.kim@dgist.ac.kr								1			1											1
	Gangneung-Wonju National University (GWNU)	elizabeth.locci@cern.ch			1	1																		1
KR Total					1	1				1			1											2
NL	NIKHEF	r.kluit@nikhef.nl										1	1						1	1	1		1	3
NL Total												1	1						1	1	1		1	3
NO	Norwegian Institutes (UiB, UiO, USN) represented by University of Bergen (UiB)	johan.alme@uib.no																			1	1	2	2
NO Total																					1	1	2	2
PL	University of Krakow AGH	Marek.ldzik@cern.ch								1			1											1
PL Total										1			1											1
SE	University of Uppsala	richard.brenner@physics.uu.se			1	1																		1
SE Total					1	1																		1
UK	Imperial College	g.iles@imperial.ac.uk	1			1													1	1				2
	Queen Mary University of London (QMUL)	m.bona@qmul.ac.uk																1		1				1
	UKRI-STFC Rutherford Appleton Laboratory (RAL)	mark.prydderch@stfc.ac.uk					1		1									1	1	2	1		1	4
	University College London (UCL)	a.korn@ucl.ac.uk																1		1				1
	University of Birmingham	S.J.Hillier@bham.ac.uk	1			1												1		1				2
	University of Bristol	David.Cussans@Bristol.ac.uk					1		1			1	1					1	1	2				4
	University of London Royal Holloway	veronique.boisvert@rhul.ac.uk					1		1					1			1							2
	University of Manchester	conor.fitzpatrick@cern.ch														1	1	1		1				2
	University of Oxford; Rutherford Appleton Laboratory	prof.jocelyn.monroe@gmail.com												1			1							1
	University of Warwick	karolos.potamianos@cern.ch					1		1															1
UK Total			2			2	4		4			1	1	2		1	3	6	3	9	1		1	20
US	Argonne National Laboratory (ANL)	jinlong.zhang@cern.ch	1			1																		1
	Brookhaven National Laboratory (BNL)	chc@bnl.gov																	1	1				1
	Fermilab National Laboratory (FNAL)	dbraga@fnal.gov	1			1	1		1					1			1							3
	Ohio State University	gan.1@osu.edu			1	1																		1
	SLAC National Accelerator Laboratory	lorenzor@slac.stanford.edu								1			1								1		1	2
	University of Boston	angelo.giacomo.zecchinelli@cern.ch									1		1											1
	University of Minnesota	rusack@umn.edu										1	1											1
US Total			2		1	3	1		1	1	1	1	3	1			1		1	1	1		1	10
Grand Total			14	8	8	30	8	2	10	9	3	10	22	10	5	9	24	10	7	17	10	5	15	118

Figure 16: Contributors to DRD7 (continued, part 2 of 2)

B Appendix B: Projects Description

B.1 Work Package 7.1: Data density and power efficiency

B.1.1 Project 7.1a: Silicon Photonics Transceiver Development

This project aims to develop high-speed optical transceivers based on Silicon Photonics technology for use in a wide range of future particle physics applications from low-temperature neutrino detectors to high-radiation environment HL-HLC pixel detectors.

Project Name	Silicon Photonics Transceiver Development (WG7.1a)
Project Description	Develop high-speed optical transceivers based on Silicon Photonics technology. Duration 4-5 years.
Innovative/strategic vision	First opportunity to design and operate custom optical data transmission systems in HEP detectors.
Performance Target	100 Gb/s per fibre optical readout with 2.5 Gb/s control optical link operating at a BER of 10^{-12}. Radiation tolerance up to 1×10^{16} particles/cm^2 and 10 MGy and power consumption of 250 mW. Cryogenic temperature operation for some lower-speed variants.
Milestones and Deliverables	**M7.1a.1** (M12) Cryogenic test of SiPh PIC **M7.1a.2** (M12) Submission of Ring Modulator Driver **D7.1a.1** (M12) Delivery of WDM test PIC **M7.1a.3** (M24) Radiation test of WDM PIC **D7.1a.2** (M24) Delivery of packaged WDM PIC **M7.1a.4** (M30) Submission of photodiode TIA **M7.1a.5** (M36) System test of WDM PIC with Driver
Multi-disciplinary, cross-WG content	Silicon Photonics combines data-density, timing distribution, Back-end, as well as 2.5/3D integration, with the need for foundry access to specialist processes.
Contributors	CA: Sherbrooke CERN DE: DESY, KIT, Wuppertal ES: IGFAE GB: Birmingham, Imperial IT: INFN Milano, INFN Pisa, Sant'Anna, Uni. Trento US: Argonne, Fermilab
Available resources	25.7 FTE/yr 440k/yr
Addt'l resource need	8 FTE/yr 250k/yr

Project Description

Optical data transmission has become ubiquitous in modern high energy physics detector readout and control systems as it offers high transmission bandwidth, low mass, electro-magnetic interference immunity, and radiation tolerance. Future detectors will continue to rely on this technology and will require different as-yet unproven characteristics depending on the target application. These include: enhanced radiation tolerance for HL-LHC detector upgrades; ultra-low mass, perhaps achieved with unprecedented levels of integration between front-end electronics and photonics; as well as cryogenic operation in neutrino detectors. This project brings together groups across national boundaries in order to address the wide range of potential applications through the use of Silicon Photonics (SiPh) technology. SiPh uses CMOS foundry processes to pattern light-manipulating structures onto SOI wafers. A growing number of commercially-available MPW services offer the HEP community the possibility to custom-design photonic devices and circuits to best address the wide variety of potential applications.

The project will feature various topics to be addressed by different collaborators in order to build a complete picture of the full potential offered by the SiPh technology. These are:

1. Silicon Photonic Integrated Circuit (PIC) design,
2. Silicon Photonics modulator driver design,
3. Silicon Photonics photodiode TIA design,
4. Silicon Photonics device environmental effects (Temperature, Radiation),
5. Silicon Photonics packaging,
6. Silicon Photonics system integration and testing.

Performance Target

The overall goal of this project is to design, fabricate and assemble SiPh-based transceivers targeted at different applications. Examples include: high-speed variants, allowing the transmission of 4x 25 Gbps channels on four wavelengths multiplexed onto a single optical fibre; and low-speed variants for cryogenic applications. The high-speed variants might target high-radiation applications like HL-LHC detector upgrades where radiation-levels will exceed 1×10^{16} particles/cm^2 and 10 MGy, or lower radiation levels where size, mass, and power are the most important metrics. Achieving the ultimate levels of integration requires the development of packaging technologies to tightly co-package the photonics circuits with the detector front-end electronics as well as IP blocks for modulator drivers and TIAs that can be integrated directly into the front-end ASICs.

Milestones and Deliverables

M7.1a.1 (M12) Cryogenic test of SiPh PIC: testing of a PIC will be carried out at cryogenic temperatures to establish feasibility and/or determine areas of future work.

M7.1a.2 (M12) Submission of Ring Modulator Driver: the design of a Ring Modulator driver will be submitted for fabrication.

D7.1a.1 (M12) Delivery of WDM test PIC: a PIC that demonstrates the use of 4-channel Wavelength Division Multiplexing (WDM) to transmit multiple Gb/s datastreams onto one optical fibre.

M7.1a.3 (M24) Radiation test of WDM PIC: radiation testing (at multiple sources) will be carried out to show the feasibility of the various WDM components and system to operate in radiation environments.

D7.1a.2 (M24) Delivery of packaged WDM PIC: a PIC will have optical fibres attached to it with minimal loss, ready for integration into larger systems.

M7.1a.4 (M30) Submission of photodiode TIA: the design of a TIA for use with SiPh photodiodes will be submitted for fabrication.

M7.1a.5 (M36) System test of WDM PIC with Driver: a high-level system test of a WDM PIC integrated with a driver ASIC will be carried out.

Multi-disciplinary, transversal content

Building, testing, and qualifying a full SiPh optical transceiver that can be used in a large number of final applications requires expertise in a very wide range of domains. Collaborators skilled in photonic device physics, ASIC design, PCB design, FPGA design, radiation effects, cryogenics, and photonic device physics are all needed. The technology developed will find use across the full range of detector systems being considered by the 2021 ECFA Detector R&D Roadmap.

Contributors and areas of competence

- **Argonne**: has experience in electronics design and testing and has worked with several industry partners on understanding and modifying silicon photonics devices for radiation hardness.
- **University of Birmingham**: Experience in the integration of detector readout systems. Wire-bonding equipment is available, along with access to neutron- proton irradiation beamlines.
- **CERN**: has designed several SiPh PICs as well as driver and TIA circuits, has carried out system and radiation testing, and has developed fibre attachment processes for PICs. Electronic and Photonic circuit and chip design software is available, along with the necessary electronic and photonic test equipment for testing up to 30 Gb/s. Wire-bonding and fibre-attach equipment is also available. Access is available to X-ray irradiators and a proton-irradiation beamline.
- **DESY**: has designed a monolithic 50-Gb/s SiPh EPIC transceiver in CMOS technology. Electronic and photonic circuit and chip design software is available, along with the necessary electronic and photonic test equipment for testing Tx up to 12 Gb/s and Rx up to 40 Gb/s. In-house processes for bump-bonding as well as chip-and-wire are available.
- **Fermilab**: is currently developing low-power, high bandwidth photonic links for the readout of pixel detector and front end chips. The activity currently includes the development of driver circuits integrated in front end ASICs, wirebonded and co-packaged with a micro ring modulators in a photonic integrated circuit (PIC). Electronic and Photonic circuit and chip design software is available.
- **IGFAE**: has participated actively in the low-temperature vacuum environment qualification of front-end components of the LHCb VELO. Lab equipment is available for operating custom electronics in such environments.
- **Imperial College**: has designed several Readout and Control boards for HEP detectors. Board and FPGA design software is available, along with the necessary electronic and photonic test equipment for testing up to 53.125 Gbaud PAM4.
- **KIT**: has designed several SiPh PICs as well as driver circuits. Electronic and Photonic circuit and chip design software is available, along with the necessary electronic and photonic test equipment for testing up to 28 Gb/s digital and 40 GHz analog. Wire-bonding and fibre-attach equipment is also available.
- **INFN Milano**: has designed and characterised many electronic ASICs. Electronic and Photonic circuit and chip design software is available.
- **INFN Pisa**: has designed and characterised several SiPh PICs as well as driver circuits, and has carried out radiation testing. Electronic and Photonic circuit and chip design software is available. Wire-bonding equipment and access to an X-ray irradiator is also available.
- **Scuola Superiore Sant'Anna**: has designed several SiPh PICs. Electronic and Photonic circuit and chip design software is available, along with the necessary electronic and photonic test equipment for testing up to 50 Gb/s.
- **Université de Sherbrooke**: has designed several SiPh PICs as well as driver circuits. Electronic and Photonic circuit and chip design software is available, along with electronic and photonic test equipment. Cryogenic test chambers are available, and access for device packaging is available via an external provider.
- **Universitá di Trento**: has designed and characterised several PICs as well as driver circuits. Electronic and Photonic circuit and chip design software is available with access to HPC servers. Access is available to X-ray and proton sources as well as to facilities at Fondazione Bruno Kessler (FBK).

- **Bergische Universität Wuppertal**: Experience in the integration of pixel detectors to high-speed FPGAs(off-detector). Programming of firmware and software layers.

Project Contact person: Jan Troska (CERN).

Available resources, existing funding and frameworks

Table 2 shows the manpower and funding currently assured in participating institutes from the relevant funding framework for an initial three-year project duration. The values are given as averaged annual amounts.

Table 2: Available resources and areas of contribution numbered as in Section B.1.1.

Institute	**Framework**	**Areas of Contribution**
Argonne	DOE	1,4,6
Birmingham	–	4,6
CERN	EP R&D	All
DESY	Helmholtz	All
Fermilab	DOE	All
IGFAE	–	4,6
Imperial	institute	6
KIT	Helmholtz	1,2,5,6
Milano	FALAPHEL/IGNITE	2
Pisa	FALAPHEL/IGNITE	1,2,4
Sant'Anna	institute	1,4
Sherbrooke	NSERC	1,2,4,(5)
Trento	institute	1,2,4,6
Wuppertal	BMBF (Si-D consortium)	6
	FTE/yr	**Annual Funding** [EUR]
Total available	25.7	440k

Estimate of to be requested resources

Table 3 shows the manpower and funding foreseen to be requested by participating institutes from the relevant funding framework. Not all aspirations are available at this time.

Table 3: Resources to be requested. One should consider that requests will be answered in the year following submission.

Institute	**Framework**	**Request submission year**
Argonne	DOE	2024
Birmingham	UK R&D	2023
CERN	–	–
DESY	Helmholtz	2023
Fermilab	DOE	2023
IGFAE	–	–
Imperial	UK R&D	2023
KIT	BMBF	2023
Milano	–	–
Pisa	–	–
Sant'Anna	Internal	2024
Sherbrooke	NSERC	2024
Trento	–	–
Wuppertal	BMBF (Si-D consortium)	2023
	FTE/yr	**Annual Funding** [EUR]
Total to be requested	8	250k

B.1.2 Project 7.1b: Powering Next Generation Detector Systems

This project aims to develop power distribution schemes and their voltage/current regulators and converters for use in a wide range of future particle physics applications, from low-temperature neutrino detectors to high-radiation environment HL-HLC pixel detectors and beyond (future collider's experiments)

Project Name	Powering Next Generation Detector Systems (WG7.1b)
Project Description	Develop power distribution schemes and their voltage/current regulators. Duration 4-5 years.
Innovative/strategic vision	Develop very efficient converters (at least 90% at high load, 10A), and at unprecedented radiation hardness up to 1×10^{16} particles/cm^2 and 10 MGy . New technologies as CMOS High voltage 0.18um will be used along with new Gallium Nitride (GaN).
Performance Target	High-efficiency (at least 90% at high load) converters for serial and parallel powering schemes for high voltage conversion and around 75% for fully integrated DCDC in 28nm technology. Radiation tolerance up to 1×10^{16} particles/cm^2 and 10 MGy
Milestones and Deliverables, activity number attached to milestone described in Table 4	**M7.1b.2** (M12) Test results on first prototypes of a linear regulator and a resonant converter in 28nm technology **M7.1b.1,3,4,5** (M24) Tests on parallel and serial GaN DCDC converter prototypes with custom air core inductors **D7.1b.1,3,4,6** (M36) Delivery of a report on high voltage (48V) DC-DC converter for serial and parallel powering schemes **D7.1b.2** (M48) Delivery of a report on low voltage on-chip regulation in 28nm technology.
Multi-disciplinary, cross-WG content	Power distribution scheme combines connection with Back-end power supplies and integration of the on-chip regulation in the front-end ASICs (Pixel, strips and monolithic)
Contributors	AT: TU Graz CERN DE: FH Dortmund, RWTH Aachen University EE: Tallinn University of Technology (TalTech) ES: ITAINNOVA IT: INFN Milan, University of Udine (UNIUD), University of Milan (UNIMI)
Available resources	5.2 FTE/yr 87k/yr
Addt'l resource need	5.4 FTE/yr 101k/yr

Project Description

Next-generation, large-area, high-granularity particle detectors consume significantly more power at reduced voltages compared to current systems. This project aims to improve the power efficiency of detector systems at a reduced material budget. For this purpose, parallel and serial powering options will be investigated: DC-DC converters with high conversion factor and innovative hybrid architectures, such as fully integrated resonant and 3-level buck converters, along with LDO voltage regulators with high PSRR and shunt regulators with improved efficiency, will be studied. Prototype powering modules will be developed and characterized.

The aim of this project is to improve the overall power efficiency of detector systems, reducing the material budget and improving the local voltage regulation, compensating the voltage drops along cables and hybrids. For this purpose, both parallel and serial powering schemes will be investigated. For the first option, a power scheme based on a two-stage DC-DC voltage conversion

is under design. The power is distributed at 48V to stage-1, where it is converted to 5V by a commercial off-the-shelf (COTS) GaN power stage controlled by a radiation hard controller chip. For stage 2, a resonant converter will be implemented in 28nm CMOS technology to convert the supply voltage further down to 0.9-1.0V. The resonant converter will be fully integrated with no external components and will consist of thin gate-oxide transistors only to achieve a very high TID. In addition, a 3-step buck converter architecture will be investigated for a minimum of factor two down conversion in a 28nm CMOS technology. A critical block for sensitive front-end electronics is a low-drop linear voltage regulator, which will be designed fully integrated in 28nm CMOS technology. For the serial powering option, a constant current source based on a radiation tolerant and magnetic field resistant GaN DC-DC converter will be developed. Significant emphasis will be given to design implication related to high-switching frequencies, small size magnetic components, PCB EMI filter design and modularity. In addition, the Shunt-LDO regulator will be ported to 28nm CMOS technology, and a switching shunt element will be investigated to improve the efficiency of the regulator. Prototype power modules will be developed and intensively characterized. Summarizing the project will feature various topics to be addressed by different collaborators in order to build a complete picture of the power distribution scheme. These are summarised in Table 4.

Table 4: DRD 7.1b list of main activities and given number

Topic number	**Activity**
1	48V rad-hard ASIC DC-DC converter design.
2	On-chip 28nm rad-hard voltage regulation (DC-DC, LDO, ShuntLDO).
3	48V DC-DC converter design for serial power applications.
4	DC-DC converter module design, PCB optimisation.
5	Design of optimised air-core inductors.
6	DC-DC converter system integration and testing.
7	Development of Serial power systems.

Performance Target

- **GaN DC-DC Converter**: conversion factor 10 from Vin=48V, load current 10A, switching frequency 1 MHz, efficiency 95%, composed by a GaN COTS power stage and a controller ASIC
- **Resonant Converter**: conversion factor 5 from Vin=5V, load current 500mA, switching frequency 30 MHz, efficiency 75 % designed in 28nm technology as an IP block,
- **3-level Buck Converter**: conversion factor 5-2 from Vin=5V or Vin=2V, load current 500mA, switching-frequency 30 MHz, efficiency 75 %
- **Capless-LDO**: input voltage 1.1-1.2V, output voltage 0.9V, load current 200mA, designed in 28nm technology as an IP block
- **GaN DC-DC Current Source**: input voltage 48V/24V, – current output 10A, output power 200W, switching frequency 2 MHz
- **SLDO**: input voltage 1.4V-2V, output voltage 0.9V-1.2V, load current 1A, shunt current 1A

Milestones and Deliverables

Milestones and Deliverables for the full project are presented in Table 5. The activities in the "Milestones ref" and "Deliverables Ref" columns are numbered as in Table 4. These milestones and deliverables depend on the funding of several institutes which are relying on their funding agency. In case of missed funding, milestones and deliverables will be updated year by year.

Table 5: DRD 7.1b Full project milestones and deliverables

Target Date	Milestones Ref	Deliverable Ref	Description
(M12)	**M7.1b.2**		Test results on first prototypes of a linear regulator and a resonant converter and simulation results of SLDO with efficient shunt-element in 28nm.
(M24)	**M7.1b.1,3,4,5**		Tests on parallel and serial GaN DCDC converter prototypes with custom air core inductors. Pre/Post irradiation test results of SLDO protoytpe in 28nm.
(M36)		**D7.1b.1,3,4,6**	Delivery of a report on high voltage (48V) DC-DC converter for serial and parallel powering schemes. Test results on optimized SLDO prototype.
(M48)		D7.1b.2	Delivery of a report on IP-block in 28nm technology for FE on-chip local regulation and integrated smart powering
(M60)		D7.1b 1,3,4,6,7	Delivery of a report on High Voltage powering solutions for future HEP experiments, module integration and system test results

Multi-disciplinary, transversal content

Power distribution in modern HEP experiments is a complex task because it merges power electronics, radiation hardness, system integration and interface with commercial power supply from one side and front-end electronics on the other side. It is a multidisciplinary eco-system that requires knowledge on a variety of design, testing and reliability aspects that are present in this working group. This also implies an interface with other working groups, in particular with DRD7.4, focusing on Radiation Tolerance, Longevity and operation in Extreme Environments.

Contributors and areas of competence

- **RWTH Aachen University**: One focus is the deep characterization of DC-DC converter chips and modules developed by CERN and FH Dortmund, in terms of efficiency, line and load regulation, and conducted and radiated noise. The DC-DC converter boards provided by CERN will also be interfaced to a CMS Phase-2 strip module. The DC-DC chips will eventually be integrated onto a modified version of the CMS service hybrid. This will then allow a detailed assessment of the performance of a real realistic strip module with a conversion ratio of 40, and the feasibility of such an approach for future silicon detector modules allowing to benchmark the new proposed powering schemes against the ones implemented for HL-LHC.

- **TU Graz**: linear regulator design and reliability studies. At TU Graz, the Institute of Electronics is strategically focused on robust electronics systems. The competencies include electromagnetic compatibility testing with all necessary lab resources (immunity - EMI and emissions - EME) at PCB and IC level. Further TU Graz has also an in-house facility for total ionizing dose testing (TID), allowing for stress up to 1 Grad and with calibration methodology as used in the HEP community. The group has been intensely involved in IC design and reliability characterization of devices and circuits in 28 nm CMOS technology since 2018.

- **ITAINNOVA**: Current source development and DC-DC module prototyping & characterization (PCB design - Embedded components, EMI emissions control and Modular/multiphase design)

- **FH Dortmund**: Shunt regulator and high-frequency buck converter design

- **CERN**: High conversion rate ASIC DC-DC converter design and fully integrated DC-DC in 28nm technology. In the team we merge ASIC design knowledge with highly integrated PCB

module design, developed in order to ensure power integrity, reliability, low EMI emission, low mass and reduced cost.

- **UNIUD**: innovative architecture converter design, air core inductor optimisation in PCB board and in 28nm ASIC
- **INFN Milano and Università di Milano**: Integration of DC-DC converters in calorimeter and tracking systems, mechanical integration, testing for reliability and operational performance in hostile environments (magnetic field, radiation, low temperature). Investigation of serial powering implementation in silicon tracking systems.
- **Tallinn University of Technology (TalTech)**: technology of coupled-inductor-based step-down DC-DC converters compatible with controller ASIC being developed by CERN. This work will yield a scalable approach for high step-down converters with high efficiency. Integration of coupled inductors with a non-magnetic core into printed circuit boards will be addressed to achieve low profile designs.

The two coordinators and therefore contact persons of the DRD7.1b project are Stefano Michelis from CERN (stefano.michelis@cern.ch) and Michael Karagounis from FH-Dortmund (michael.karagounis@fh-dortmund.de)

Available resources, existing funding and frameworks

Table 6 shows the manpower and funding currently assured in participating institutes from the relevant funding framework for an initial three-year project duration. The values are given as averaged annual amounts. Only three institutes have considerable funding available. The other institutes can provide little support and rely on their funding agency for joining the project and provide more FTE and monetary funds. Therefore if the institutes will not receive funds from their funding agency, the milestones and deliverables will be revised year by year.

Table 6: Available resources and areas of contribution numbered as in Table 4

Institute	**Framework**	**Contrib. area**	**FTE/Funds(EUR)**
CERN	EP R&D	1,2,4,5	1.7/35k
FH Dortmund	BMBF (05H21PRCA9, 05H21PRRD1)	2,7	0.8/6.7k
ITAINNOVA	GaNCap4CMS, PC Fisica-MMR and AIDAinnova	3,6,7	0.8/26.7k
RWTH Aachen	Institute	6	0.4/0
TU Graz	Institute	2,6	0.3/0
UNIUD	Institute	1,2	0.5/0
INFN and UNIMI	Institute	6,7	0.3/1.7k
Taltech	RVTT3, Estonian Research Council	4,5	0.3/16.7k
	FTE/yr	**Annual Funding** [EUR]	
Total available	5.2	87k	

Estimate of resources to be requested

Table 7 shows the manpower and funding foreseen to be requested by participating institutes from the relevant funding framework. Not all aspirations are available at this time.

Table 7: Resources to be requested. One should consider that requests will be answered in the year following submission.

Institute	**Framework**	**Request submission year**
CERN –	–	
FH Dortmund	transnational funding agencies	2023
ITAINNOVA	Spanish funding agencies	2024
RWTH Aachen	BMBF	2023
TU Graz	Austrian Science Fund FWF	2023
UNIUD	INFN	2024
INFN and UNIMI	INFN	2024
Taltech	Department/University Internal Funding	2024
	FTE/yr	**Annual Funding** [EUR]
Total to be requested	5.4	101k

B.1.3 Project 7.1c: WADAPT (Wireless Allowing Data and Power Transmission)

This project aims to develop wireless technology based on a millimeter wave (mmw) transceiver IC as well as on Free Space Optics to connect neighboring detector layers, providing increased data rates, high power efficiency and high density of data links, with the aim of reducing mass and power consumption.

Project Name	WADAPT (WG7.1c)
Project Description	Develop millimeter wave Wireless technology together with Free Space Optics technology to connect neighbouring detector layers with the aim of reducing mass and power consumption. Wireless power transmission will also be explored.
Innovative/strategic vision	First attempt to provide a promising alternative to cables and optical links that would revolutionize the detector design. Removing partly or totally cables would be a major advance in reducing the amount of spurious matter spoiling the measurement of the particle parameters. In addition wireless technology allows efficient partitioning of detectors in topological regions of interest, with the possibility of adding intelligence on the detector to perform 4D reconstruction of the tracks and vertices online.
Performance Target	Radial wireless readout for pixel detectors. Data from detector front-end modules can be serialized as channels up to 10 Gb/s and be aggregated across detector layers (25 to 100 Gb/s). Commercially available technology has demonstrated radiation hardness amply sufficient for envisaged lepton colliders. Radiation hard transceivers will be developed in order to match maximum radiation fluence expected at future hadron colliders; HL-LHC: 2×10^{16} particles/cm^2 and FCC-hh: 6×10^{16} particles/cm^2.
Milestones and Deliverables	**M7.1c.1,2,3** (M12,24,36) Intermediate annual reports **D7.1c.4** (M24) Delivery of report summarising a proof of principle demonstration of multi-hop RF data transmission using commercial ICs **D7.1c.7** (M24) Delivery of a design of an optimized RF transceiver IC **D7.1c.10** (M36) Delivery of a test report demonstrating FSO data transmission, integration, radiation hardness **M7.1c.4** (M36) Demonstrators made available and training organized.
Multi-disciplinary, cross-WG content	mmw technology and FSO technology will as much as possible aim at developing common tools as common interfaces and common test benches in order to ease performance comparison in a given context and provide the users with adapted solutions. After proof of principle, the ultimate goal would be to generalize the use of wireless data-links to other detectors, with the potential of adding on-detector intelligence. This is however beyond the scope of this 3-years project and further system and implementation analysis will then be required. Some collaboration with groups developing radiation hard ICs, 4D and monolothic could be envisaged.
Contributors	FR: CEA-Leti, LPSC IL: Tel-Aviv IT: INFN Pisa, Scuola Superiore Sant'Anna KR: GWNU SE: Uppsala US: Ohio State University
Available resources	5 FTE, 174 kEUR /yr
Addt'l resource need	7.5 FTE /yr, 500kEUR /yr

Project Description

High Energy Physics (HEP) experiments have always employed wired data transmission lines. Low mass twisted pairs are good compromises for data transmission in harsh environments allowing to reach bands of O(1 Gb/s) up to about one meter distance. When radiation doses decrease, plastic fibers can have one order of magnitude larger bandwidths over several hundred meters. One of the main drawbacks of those systems is their material budget, deviating the trajectories of charged particles, or provoking photon conversions. Wireless data transmission allows to overcome these problems, so that a coherent wireless, cost-effective wired optical or plastic fiber [1] network can be envisaged to export data to off detector boards and PCs. Among wireless technologies two are of main interest: a millimeter wave (RF) carrier based one, and an optical based Free Space Optics (FSO) one.

Wireless technology based on millimeter wave (mmw) transceiver IC has been proposed by the WADAPT consortium to ECFA as a key technology to connect neighboring detector layers, providing increased data rates, high power efficiency and high density of data links, with the aim of reducing mass and power consumption. The millimeter wave technologies are compatible and complementary to wireless optical technologies (Si-Photonics and Free Space Optics) and wired standards (Ethernet, PCI-e, USB3, etc) since they provide comparable data rate and Quality of Service, and share modulation scheme. Wireless applications encompass HEP experiments at high-energy colliders, neutrino physics experiments, astroparticle-physics experiments and low energy experiments at the intensity frontier. Regarding high-energy colliders, [2] proposes the following radial wireless readout for pixel detector. Data from detector front-end modules can be serialized as channels of 1 to 10 Gb/s. Data are transmitted by a wireless multi-hop network between detector layers. For limited distances, energy efficiency may be optimized by the use of non-coherent transceiver chips. At the higher layer level, the data are collected and aggregated. Feasibility studies regarding the integration of the 60 GHz wireless technologies in silicon tracking detector were performed [3]. Several aspects relevant for the implementation of 60 GHz links were studied: transmission losses, interference effects, absorbing materials and the influence of the antenna design and directivity, power consumption. More recently, tests have been successfully conducted using non-coherent transceiver prototypes from STMicroelectronics, especially for latency, connectivity and radiation hardness. A full description of the technology and of the tests can be found in [4]. Free space optics (FSO) demonstrated being able to reach similar data rates up to a few meters [5]. Past R&D [6] on using commercial VCSEL demonstrated their radiation hardness up to few hundred Mrad. Radiation hardening shall however be considered on C65SPACE (with includes libraries with hardened cells, tested up to 0.3 Mrad dose but could handle higher radiations) or more advanced SOI technology for the highest radiation levels expected at future colliders such as HL-LHC or FCC-hh.

Both technologies (mmw and FSO) will be developed together in order to provide the HEP community with the most relevant solution for the considered application.

The following work packages can be proposed:

1. **Readout system level definition, including new link technologies** Objectives: reduction of cable mass, power consumption, more network flexibility, improved overall bandwidths and data rates, increasing the network synchronization, taking into account the environmental constrains of HEP.

2. **System level analysis, signal integrity** Objectives: assess the key performances of the proposed network, give global specifications for the different components, building of a system level simulator to evaluate the signal integrity in a multi-hop scenario with interferers from cross talks, throughout the different nodes of the network.

3. **Millimeter integrated circuit, packaging and antenna development** Objectives: Use the system analysis and signal integrity simulator to define the millimeter wave integrated circuit architecture and its components, the type of chip assembly, the packaging and antenna scheme.

4. **Proof of concept demonstrator with commercial products** Objectives: a proof of concept by building and interconnecting a three (or four) layer silicon detector, based on

commercial ICs (with reduced performance) and custom on board antennas. This mock-up of a central tracker will be equipped with the transceiver chip in BGA package. This will allow studying the added noise and data transmission quality (impact on eye diagram, Jitter, Bit Error Rate) over the different layers. The setup will be interfaced with detectors to check the readout capabilities while using multi-hop wireless link. Eventually a multilink scenario will be considered to check if the isolation between channels is sufficient for the considered application. This would bring us closer to the full-scale implementation and would help specify and integrate the future wireless systems in detectors at future colliders.

5. **Design of custom Millimeter Wave Integrated Circuit** Objectives: design of a dedicated radiation hardened millimeter-wave transceiver IP in advanced technology node, to be integrated either as a companion chip or as an IP within the silicon trackers. The transceiver shall reach high energy efficiency, while providing enough margin and robustness to operate during a long period in harsh environment, particularly under high radiation level as in future hadron colliders.

6. **Design of an integrated multi-channel readout electronics for interfacing RF mmw technology** Objectives: design of an integrated multi-channel readout electronics in 65nm or 28 nm CMOS technology (TSMC) for data digitising and for interfacing the multi gigabit wireless data transmission module with the detectors with a capacitance of 10pF. The radiation hardness of this interface will have to match that of the transceiver.

7. **Dissemination, training on RF/mmw technologies** Objectives: organization of workshop and training on RF/mmw technologies. The training will use the proof-of-concept demonstrator to feel the physical behavior of the wireless propagation.

8. **Realize and test a FSO system solution for a FCC-ee tracker** Objectives: maximum data rate as a function of distance, signal integrity and latency, material budget and power reduction compared to a plastic fiber solution.

9. **Exploration of wireless power transmission** Objectives: selection of power transmission means, building of demonstrators

All these work packages are not at the same level of advancement and funding. For example, the objectives defined in the AIDAInnova proposal (WP4) are fully funded and the project already started. After 2 years the scope of the AIDA-Innova project should be reached and will need extra-funding to build a new demonstrator with eventually a full sector of a micro-vertex detector during the third year and beyond. This project will benefit from additional contribution from Tel-Aviv University. This project uses commercially-available transceivers, which have reduced performance with respect to dedicated transceivers. WP3 aims at designing a dedicated transceiver with increased performance, which will be tested for radiation hardness. WP5 aims at increasing radiation hardness by advanced technologies. The goal of WP6 is to design an interface between the transceiver and the detector; the radiation hardness of this interface will be assessed. WP6 is partially funded (3 years engineering through apprenticeship). WP1,2,3 are necessary for system definition and analysis, packaging. WP8 explores FSO as an alternative to RF with the goal of providing the user with the most adapted solution to the considered application. WP7 aims at providing the potential user with teaching and training. There is total synergy between these working points. It is therefore highly desirable to conduct them together. WP9 explores wireless powering with the goal of eventually removing remaining cables. Some funding request have already been submitted. For each working point the leading Institute is mentioned and other Institutes may punctually collaborate to some working points and associate to other Institutes in order to increase their participation by their common search for funds. For all packages we wish to collaborate with colleagues in other domains.

Performance targets

For the RF system bit-rates of 25 Gb/s can be targeted for low power non coherent links at D-band. For the coherent D-band RF with channel aggregation 100 Gb/s can be targeted, see (Leti) report

D-band link at 84 Gb/s in RFIC 2023 [7] and submit a paper with a Rx achieving 112 Gb/s in RFIC 2024.

The power dissipation will mainly depend on the range and data rate. Commercial transceivers consume less than 50 mW for 6 Gb/s at 4 cm range. Going to 20 cm range and 6 Gb/s would mean increasing the output power and power consumption to about 150-200 mW.

The radiation tolerance of the SMT transceiver has been tested up to 1.4×10^{14} Neq/cm^2 without significant degradation. The maximum fluence at HL-LHC is 2×10^{16} particles/cm^2 and at FCC-hh is 6×10^{17} particles/cm^2. The first demonstrator would use transceivers that would be suitable for FCC-ee and we aim at developing transceivers which radiation hardness would be increased by 2 orders of magnitude for HL-LHC provided that we obtain the resources we required. Then 2 extra orders of magnitudes would be required FCC-hh, this is beyond the scope of the three years of the project but may be envisaged in the future. This work can be conducted in a collaboration with people developing radiation hard ASICS.

For the proposed FSO system targeting FCC-ee the bit rate goal is 10 Gb/s over 1 meter with a power dissipation of less than 500 mW. The radiation tolerance target is up to 500 Mrad and 1×10^{14} Neq/cm^2.

Project achievements timeline

(M12) Integrated circuit, packaging, antenna specification and demonstrator specification

(M12) Design report on mmw transmitter test chip

(M12) Study of free space optical (FSO) system requirements and system level design

(M24) Proof of Concept Demonstrator

(M24) Test report on mmw transmitter test chip

(M24) Qualification of transmitter hardness

(M24) FSO System level design and test report

(M24) Laser photo voltaic (PV) cell integration characteristics

(M36) Wireless communication strategies

(M36) Test/characterization report on mmw transceiver integrated circuit, along with recommendations for further improvement

(M36) System integration complete

(M36) Characterization of integration of PV board

Multi-disciplinary, transversal content

mmw technology and FSO technology will as much as possible aim at developing common tools as common interfaces and common test benches in order to ease performance comparison in a given context and provide the users with adapted solutions. After proof of principle, the ultimate goal would be to generalize the use of wireless data-links to other detectors, with the potential of adding on-detector intelligence. This is however beyond the scope of this 3-years project and further system and implementation analysis will then be required. Some collaborations with group developing radiation hard ICs, 4D and monolothic techniques could be envisaged.

Contributors and areas of competence

- **CEA-Leti**: RF system and ASIC design
- **GWNU**: wireless data transmission system testing
- **INFN-Pisa**: ASIC design, experience with the design and implementation of FSO systems

- **LPSC**: ASIC design
- **Scuola Superiore S Anna di Pisa**: Experience with the design, implementation, and testing of FSO systems
- **TAU**: wireless data transmission system testing, power over fibre systems
- **Ohio State University**: ASIC design
- **Uppsala University**: wireless data transmission-system demonstrator building and testing

Contact person: Elizabeth Locci, GWNU

Available resources, existing funding and frameworks

Table 8 shows the manpower and funding currently assured in participating institutes from the relevant funding framework for an initial three-year project duration. The values are given as averaged annual amounts.

Table 8: Available resources and areas of contribution numbered as in Section B.1.3.

Institute	**Framework**	**Areas of Contribution**
CEA-Leti	IN2P3	1, 2, 5, 7
GWNU	institute	4,
INFN-Pisa	INFN	7, 8
LPSC	IN2P3	6
Scuola Superiore S Anna di Pisa	institute	7, 8
TAU	institute	4, 9
Ohio State University	DOE	5
Uppsala University	AIDAinnova	3, 4
	FTE/yr	**Annual Funding** [EUR]
Total available	5	174k

Estimate of to be requested resources

Table 9 shows the manpower and funding foreseen to be requested by participating institutes from the relevant funding framework. Not all aspirations are available at this time.

Table 9: Resources to be requested. One should consider that requests will be answered in the year following submission.

Institute	**Framework**	**Request submission year**
CEA-Leti	–	–
GWNU	–	–
INFN-Pisa	INFN	2024
LPSC	IN2P3	2024
Scuola Superiore S Anna di Pisa	institute	2024
TAU	institute	2024
Ohio State University	DOE	2023
Uppsala University	–	–
	FTE/yr	**Annual Funding** [EUR]
Total to be requested	7.5	500k

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[4] R. Brenner, C. Dehos, and E. Locci. Multi gigabit wireless data transfer in detectors at future colliders. *Frontiers in Physics*, 10, 2022.

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[6] A. Messa et al. Optical wireless systems for high energy physics: Design and characterization. In *2019 21st International Conference on Transparent Optical Networks (ICTON)*, pages 1–4, 2019.

[7] CEA-Leti Jose Luis Gonzalez-Jimenez. A channel aggregation architecture tx-rx in d-band with 84 gb/s data-rate in rfsoi process. In *RFIC 2023*, pages 1–4, 2023.

B.2 Work Package 7.2: Intelligence on the detector

Note: Project 7.2a (e-FPGA) is not yet ready to be launched and will be added to the work package portfolio in a future round.

B.2.1 Project 7.2b: Radiation Tolerant RISC-V System-On-Chip

The project aims to develop a radiation-hardened System-On-Chip (SoC) based on the RISC-V ISA standard.

Project Name	Radiation Tolerant RISC-V System-On-Chip (WG7.2b)
Project Description	Develop a radiation-hardened SoC based on the RISC-V ISA standard according to the roadmap defined in M7.2b.1. Topics: 1- SoC architectures 2- Radiation Tolerance design methodology, 3- Verification methodology, 4- SoC generator toolchain. Duration 5-6 years.
Innovative/strategic vision	Develop a technology and a design platform to anticipate and adapt the challenges and opportunities of the future Electronic systems and IC design.
Performance Target	The following targets will be defined in M7.2b.2: Processing Speed Power Consumption Radiation Tolerance Memory and Storage Communication Interfaces Scalability and Flexibility Verification and Testing
Milestones and Deliverables	**M7.2b.1** (M12) Rad-Tol RISC-V SoC roadmap **M7.2b.2** (M24) SoC architectures proposal **D7.2b.3** (M36) Delivery of Rad-Tol SoC building block test chip
Multi-disciplinary, cross-WG content	Electronics Engineering - Digital Design Computer Science - Embedded Systems Systems Engineering - Integration and Testing
Contributors	DE: FH Dortmund BE: KU Leuven CERN UK: UKRI-STFC RAL UK: Royal Holloway University Of London UK: University of Warwick UK: University of Bristol US: Fermilab
Available resources	6.15 FTE/year 40 kEUR/year
Addt'l resource need	7.9 FTE/year 21.7 kEUR/year

Project Description

The development of a radiation-tolerant RISC-V SoC is a cutting-edge project aimed at creating a reliable and resilient central processing unit (CPU) for High Energy Physics applications. This SoC will be based on the open-source RISC-V architecture and designed to withstand the adverse effects of ionizing radiation, which can cause soft errors in electronic components. The project can be divided into different topics:

1. **SoC architectures**: Defining the specifications for a RISC-V SoC involves documenting the key characteristics, capabilities, and requirements that the processor should meet. These specifications serve as a reference for the design and development process. They should include at least RISC-V ISA variant (e.g., RV32I, RV64G), instruction set and operations, word size and addressing, number of registers, pipeline depth, and memory hierarchy. The project might also propose to pursue more than one set of specifications to satisfy different applications.

2. **Radiation Tolerance design methodology**: Developing a radiation-tolerant RISC-V SoC requires a robust methodology to ensure the processor can operate reliably in high-radiation environments. Several techniques are available to mitigate radiation-induced errors, from triple modular redundancy (TMR), spatial and temporal redundancy, and built-in self-repair mechanisms. In addition, Radiation-Hardened components, such as memories, register's bank and interconnects, must be designed and integrated into the system.

3. **Verification methodology**: Proper verification of a CPU design and associated instruction set architecture (ISA) is one of the most challenging activities that a CPU core engineering group must tackle. Adding a radiation tolerance feature, the verification methodologies must ensure the processor's functionality and robustness in the face of ionizing radiation.

4. **SoC generator toolchain**: System-on-Chip (SoC) generation tools are software applications and frameworks that facilitate the design, development, and testing of SoCs. These tools play a critical role in the process of creating complex integrated circuits that incorporate multiple hardware and software components into a single chip. SoC generation tools support various stages of SoC development, including design, verification, synthesis, simulation, and integration.

These topics will be addressed following the Radiation Tolerant RISC-V SoC roadmap (M7.2b.1).

Performance Target

When setting performance targets for a Radiation-Tolerant RISC-V System-On-Chip (SoC), it is important to balance the unique requirements of HEP (and space applications) with the need for reliable and efficient processing. Here are some key performance targets to consider:

- *Processing Speed:* Define the target clock frequency and processing speed based on the specific mission requirements.

- *Power Consumption:* Establish power consumption targets to ensure the SoC operates within the available power budget.

- *Radiation Tolerance:* Specify the level of radiation tolerance required, indicating the types and doses of radiation the SoC should withstand without experiencing critical failures.

- *Memory and Storage:* Define the capacity and speed of on-chip memory (RAM) and storage (non-volatile memory) to support data processing and storage needs.

- *Communication Interfaces:* Determine the required communication interfaces (e.g., UART, SPI, I2C) and specify their data transfer rates.

- *Scalability and Flexibility:* Consider designing the SoC to be scalable for future upgrades or modifications and flexible enough to accommodate different requirements without significant redesign.

- *Verification and Testing:* Establish comprehensive verification and testing protocols to validate the performance and radiation tolerance of the SoC under simulated conditions.

These performance targets will be defined in the SoC architecture and core choice proposals (M7.2b.2).

Milestones and Deliverables

- **M7.2b.1** Radiation Tolerant RISC-V SoC roadmap, target 12M.
  The target specification of the Radiation-Tolernat System-On-Chip hardware will be defined and a development roadmap will be outlined, addressing the topic #1 described in B.2.1 and Milestones and Deliverables will be stipulated.

- **M7.2b.2** SoC architecture and core choice proposals, target 24M.
  System-On-Chip topologies, including selected processing cores, will be proposed for implementation and Radiation-Tolerant design and verification methodologies will be established, as described in the topic #2 of B.2.1.

- **D7.2b.3** Delivery of Rad-Tol SoC building block test chip, target 36M.
  Silicon prototyping of the SoC building blocks (processing cores, memories, interconnects, peripherals, auxiliary IP blocks). The SoC prototype test chip will make use of the SoC generator toolchain as described in #4 of B.2.1.

Multi-disciplinary, transversal content

The development of a Radiation-Tolerant RISC-V System-On-Chip (SoC) involves collaboration across various disciplines to address the unique challenges posed by harsh environments like High Energy Physics or space. The multidisciplinary and transversal aspects are:

- *Electronics Engineering - Digital Design:* Designing the RISC-V processor and other digital components to ensure efficient and reliable operation in the presence of radiation.

- *Computer Science - Embedded Systems Programming:* Developing software that can efficiently run on the RISC-V architecture and optimizing code for the specific constraints and features of the SoC. As well as implementing algorithms that can detect and recover from errors induced by radiation, ensuring the reliability of computations.

- *Systems Engineering - Integration and Testing:* Bringing together various components and subsystems, and testing the integrated system under simulated space conditions to validate its performance and radiation tolerance.

The success of creating a radiation-tolerant RISC-V SoC depends on collaboration between experts in various fields to overcome challenges associated with radiation harsh environments.

Contributors and areas of competence

- **FH Dortmund** has hands-on experience in:
  - **Design & Implementation** – Implementation RISC-V processor on silicon.
  - **Verification methodology** – Verify of core functionality and SEE mitigation measures.
  - **Radiation Tolerance methodology** – Validate TID hardness by X-ray and SEE tolerance by heavy ion irradiation.

- **KU Leuven**:
  - **Radiation Tolerance methodology** – Assessing and implementation of radiation tolerance methodologies in RISC-V CPUs.
  - **Radiation Tolerance methodology** – Assessing and implementation of radiation-hardened subcomponents of an SoC, such as memories, register banks, interconnects and other peripherals.
  - **Verification methodology** – Verification of RISC-V Processors and it's associated Instruction Set Architecture (ISA).

  - **Verification methodology** – Verification of radiation tolerance methodologies used in RISC-V CPUs and subcomponents of the SoC. Both in simulation and emulation (FPGA implementation for assessing Single-Event Upsets (SEUs)).

- **CERN**: In the CERN EP R&D framework, the institute has research activities on:
  - **Radiation Tolerance methodology** – Design of a fully radiation-tolerant RISC-V based SoC (System-On-Chip) for control and monitoring.
  - **SoC generation** – Development of a System-On-Chip Radiation-Tolerant EcoSystem. The EcoSystem will be based on standardized interconnect technologies employing radiation tolerant techniques as well as the preparation of the specifications and interconnects.

- **UKRI-STFC RAL ASIC Group**:
  - **Radiation Tolerance methodology** – Investigate strategies such as Watchdog circuits for SEU tolerant processors and SoC blocks (DMA, memory, etc).
  - **SoC generation** – Evaluate the SoC methodology promoted by CERN and provide feedback.The participating UK institutes aim to develop a Common interface ASIC for a 'No Backend' approach as in DRD7.5. This will provide a good target for evaluating the SoC methodology.

- **UKRI-STFC RAL Particle Physics Department**:
  - **SoC specifications** – Verify RISC-V operation from User perspective and feedback into SoC specifications.

- **Royal Holloway University Of London**:
  - **SoC specifications** – Verify RISC-V operation from User perspective and feedback into SoC specifications.

- **University Of Warwick**:
  - **SoC specifications** – Verify RISC-V operation from User perspective and feedback into SoC specifications.

- **University Of Bristol**:
  - **SoC specifications** – Verify RISC-V operation from User perspective and feedback into SoC specifications.
  - **SoC generation** - interest and experience in developing software applications for predominantly Back-End systems but see synergies in development in 7.2b, 7.5a and 7.5b. Also have interest and experience of integrting SoC with timing and synchronisation systems.

- **Fermilab**
  - **SoC generation** – Evaluate Embedded Scalable Platform (ESP) from Columbia University. ESP is an open-source research platform for heterogeneous system-on-chip design that combines a scalable tile-based architecture and a flexible system-level design methodology.
  - **Radiation Tolerance methodology** – Investigate strategies such as triple-modular redundancy (TMR) for radiation-hardened micro-controllers, ESP network-on-chip, and custom-hardware accelerators designed either at more traditional RTL or at system level with high-level synthesis.

Contact persons:

- Kostas Kloukinas [kostas.kloukinas@cern.ch] - CERN
- Levi Marien [levi.marien@kuleuven.be] - KU Leuven

Available resources, existing funding and frameworks

Table 10 shows the staff and funding currently assured in participating institutes from the relevant funding framework for an initial three-year project duration. The values are given as averaged annual amounts.

Table 10: Available resources and areas of contribution numbered as in Section B.2.1.

Institute	**Framework**	**Areas of Contribution**
FH Dortmund	BMBF	1. and 3.
KU Leuven		2. and 3.
CERN	EP R&D	2. and 4.
RAL ASIC group	UK R&D	2. and 4.
RAL PPD	UK R&D	1.
Royal Holloway University Of London	UK R&D	1.
University of Warwick	UK R&D	1.
University of Bristol	UK R&D	1. and 3.
Total available per year	**FTE/yr**	**Annual Funding** [EUR]
2024	6.7	20
2025	6.2	50
2026	5.7	50
$\gg$ 2026	5.5	100

Estimate of to be requested resources

Table 11 shows the staff and funding foreseen to be requested by participating institutes from the relevant funding framework. Not all aspirations are available at this time.

Table 11: Resources to be requested. One should consider that requests will be answered in the year following submission.

Institute	**Framework**	**Request submission year**
FH Dortmund	BMBF	2023
KU Leuven		2024
CERN	EP R&D	2023
RAL ASIC group	UK R&D	2024
RAL PPD	UK R&D	2024
Royal Holloway University Of London	UK R&D	2024
University of Warwick	UK R&D	2024
University of Bristol	UK R&D	2024
Total available per year	**FTE/yr**	**Annual Funding** [EUR]
2024	7.2	5
2025	8.2	20
2026	8.2	40
$\gg$ 2026	8.2	20

B.2.2 Project 7.2c: Virtual Electronic System Prototyping

The project aims to develop a simulation of the readout chain of a particle detector at a high level, modeling the essential components and processes that occur from the moment particles interact with the detector to the digital readout of the collected data.

Project Name	Virtual Electronic System Prototyping (WG7.2c)
Project Description	Develop frameworks for high-level simulation of particle detectors. **Topics:** **1-** Signal generation in detector elements **2-** Digitization and Signal Processing **3-** Data readout architecture Topics 1. and 3. aim to create independent frameworks that can be used as a single toolchain. Topic 2. will be better defined during the project and might converge in one of the two frameworks or represent a third framework of the chain. Duration 3-4 years.
Innovative/strategic vision	Develop a toolchain for virtual prototyping to: - model detector at high-level - perform architectural studies - provide a reference model for the verification
Performance Target	**Topic 1:** Cluster multiplicity: 1-10 Position resolution: <10 μm Time resolution: 10 ps to 100 ns **Topic 2:** to be defined in M7.2c.2 **Topic 3:** Accuracy: Event/Cycle-level Speed: hundred thousand transactions per second Scalability: readout components library Verification: integrate in verification environment User-Friendly: docs & support for user-only roles
Milestones and Deliverables	**D7.2c.1** (M12) Delivery of a release of the PixESL framework **M7.2c.2** (M12) Target/methodology for Topic 2 **M7.2c.3** (M18) Model Common interface ASIC **D7.2c.4** (M24) Delivery of a release of the detector simulation tool-chain.
Multi-disciplinary, cross-WG content	**Detector Technologies:** support various detector technologies **Particle Physics Models:** integration of comprehensive particle physics models **Geometric Configurations:** ability to define and customize the geometry **Data Formats:** support for common data formats **Monte Carlo Techniques:** implementation of Monte Carlo methods for simulating particle interactions and energy depositions, **Electronics Simulation:** accurate modeling of the readout electronics **Readout Architectures:** support triggered and data-driven systems
Contributors	CERN FR: IPHC Strasbourg *USER:* PSI (CH), UK Consortium, INFN Cagliari (IT)
Available resources	3.0 FTE/year, 0 kEUR/year
Addt'l resource need	0.0 FTE/year, 0 kEUR/year

Project Description

Simulating the readout chain in a High Energy Physics (HEP) detector at a high level involves modeling the essential components and processes that occur from when particles interact with the detector to the digital readout of the collected data.

The project can be divided into different topics:

1. **Signal generation in detector elements (before conditioning and processing)**: Simulate the detector physics using specialized tools (e.g. Sentaurus TCAD). Geometry and energy deposition data (obtained by Monte Carlo techniques) are required as input from particle physics simulation teams. In simple cases the signal generation can be also provided by these teams, however the lack of proper modelling of semiconductor physics in standard tools (e.g. GEANT4, Allpix2) may require the use of TCAD software.

2. **Digitization and Signal Processing**: Simulate the readout electronics that collect signals from the detector elements. This includes pre-amplifiers, shaping amplifiers, analog-to-digital converters (ADCs), and other electronics components. Model the noise and electronics response characteristics such as gain, shaping time, and filtering. Digitize the continuous signals into discrete digital samples.

3. **Data readout architecture**: Simulate the readout architecture and data acquisition system that collects, stores, and transmits data from the detector to a computing facility for analysis. Implement a trigger system that decides whether an event should be recorded based on criteria like transverse energy, missing energy, or specific particle signatures.

In addition to the development topics listed above, the project provides a USER role that can use the toolchain to model and simulate any detector during the development phase for debugging and refining the framework.

Performance Target

Performance targets for a High Energy Physics (HEP) detector readout chain simulation framework are crucial to ensure that the simulated data accurately represents the behavior of the actual detector and meets the needs of the experimental physicists. Here are some key performance targets per topic:

Topic 1:

- *Accurate model of signal generation before conditioning.*
  The model of signal generation based on TCAD simulation in vertex detectors and trackers is vital for estimation of charge collection dynamics in order to provide:
  - better estimation of cluster multiplicity, vary from 1 to ~ 10 depending on technology and geometry, impact on readout electronics, speed, buffering.
  - proper position reconstruction and precise resolution estimation ($<10\ \mu m$) based on realistic carrier dynamics, optimisation of detector performances.
  - evaluation of subsequent signal conditioning with fast electronics, taking into account signal development time, typically from 100 ps to $\sim$100 ns.

- *Incorporation of model into framework.*
  The model should serve as a link between particle physics generated data and the input for simulation of readout electronics.

Topic 2:

The target and the methodology for the *Digitization and Signal Processing* topic will be defined as part of the milestone M7.2c.2.

Topic 3:

- *Accuracy: event/cycle-level.*
  Simulated data should closely match real data with well-characterized discrepancies. The systematic uncertainties introduced by the simulation should be well-understood and quantifiable.

- *Speed: hundred thousand transactions per second.*
  The framework should be computationally efficient to handle a large number of simulated events and particle interactions, enabling rapid exploration of physics scenarios.

- *Scalability & Flexibility: readout components library*
  The simulation should scale effectively with the complexity of the detector and experimental requirements, allowing for simulations of increasingly larger detectors and more events. In addition, the framework should be adaptable to various detector technologies and configurations, accommodating a wide range of experiments in the HEP field. In order to achieve this target, the framework shall include a library of high-level models of the readout architecture components.

- *Verification: integration in the verification environment.*
  The framework should produce a model that can be used as a reference for the verification environment.

- *User-Friendly Interface: documentation and support for user-only roles.*
  The framework should have an intuitive and well-documented user interface to facilitate its adoption by experimental physicists and researchers with comprehensive documentation and user support resources to assist users in setting up, running, and troubleshooting the simulation.

Meeting these performance targets ensures that the simulation framework is a valuable and reliable tool for experimental physicists in the HEP community, aiding in the design, optimization, and analysis of detector systems in high-energy physics experiments.

Milestones and Deliverables

- **D7.2c.1** (M12) Delivery of a release of the PixESL framework
  The first release should support data-driven and triggered readout architecture, be open source, and be well-documented to be re-usable by the community.

- **M7.2c.2** (M12) Target/methodology for Topic 2
  Define target and methodology for the Digitization and Signal Processing topic, target M12.

- **M7.2c.3** (M18) Model Common interface ASIC
  A milestone where the common interface ASIC modelling is effective.

- **D7.2c.4** (M24) Delivery of a release of the detector simulation tool-chain.
  A simulation tool-chain will consist of a Verilog-A macro-model of a pixel matrix with an interface to the PixESL framework. The macro-model will use the data obtained from the semiconductor simulation tools (TCAD and Allpix Squared) and integrate into the IC design flow.

Multi-disciplinary, transversal content

Multi-disciplinary, transversal content for a High Energy Physics (HEP) detector readout chain simulation framework refers to components, features, and considerations that cut across various scientific and technical domains to ensure the framework's versatility and relevance to a wide range of HEP experiments. Here's a brief description of such content:

- *Detector Technologies*: The framework should support various detector technologies, including calorimeters, tracking detectors, particle identification systems, and more, to accommodate different experimental setups.

- *Particle Physics Models*: Integration of comprehensive particle physics models to accurately simulate the behavior of high-energy particles as they interact with matter and produce secondary particles.

- *Geometric Configurations*: The ability to define and customize the geometry of the detector to match the specific experimental setup, including the materials and positioning of detector elements.
- *Data Formats*: Support for common data formats (e.g., ROOT, HDF5) to facilitate data exchange and analysis across different experiments and collaborations.
- *Monte Carlo Techniques*: Implementation of Monte Carlo methods for simulating particle interactions and energy depositions, considering various physics processes and cross-sections.
- *Electronics Simulation*: Accurate modeling of the readout electronics, including pre-amplifiers, amplifiers, digitizers, and trigger systems, to replicate the signal processing chain in detectors.
- *Readout Architecture*: A flexible framework supporting data-driven and triggered systems, including a model library for the main components for both architecture types.

Contributors and areas of competence

- **CERN**: The CERN EP department has launched a strategic R&D programme on technologies for future experiments. In this context, the IC technology work package, WP5, is developing a simulation framework, called PixESL, for the architectural modeling of future particle detectors. In particular, the framework proposed addresses the topic #3 Data readout architecture from B.2.2.
- **IPHC**: The C4Pi group from IPHC laboratory is working on a new generation of CMOS Monolithic active pixel sensors for high-energy physics experiments beyond 2030. The design of these sensors involves precise simulation that encompasses both the physics of particle sensing in silicon and the behaviour of the electronic microcircuits. A complete and detailed simulation chain from the initial interaction of the particle with the silicon to the sensor output data is needed. For this task, C4Pi launched a PhD thesis addressing parts of the topics #1 and #2 in the proposed framework.

User-only contributors

These institutes will get early access to the tools and help the development by providing real use cases and feedback.

- **PSI**: The PSI HEP group aims to exploit this platform in developing a future chip for the CMS inner tracker (PHASE 3). This new chip is designed in a new technology node (28 nm TSMC) to interface with the new generation of detectors based on LGAD sensors.
- **INFN Cagliari:** group aims to model the design developed in the IGNITE collaboration.
- **UK Consortium (University Of Warwick, RAL ASIC Design Group, RAL PPD)**: Virtual Framework User providing evaluation and feedback, with the option of greater participation later. The UK consortium aims to develop a Common interface ASIC for a 'No Backend' approach as in DRD7.5 and hopes to use this framework as a means to develop and decide on the correct architecture for such an ASIC.

Contact persons:

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- Maciej Kachel [maciej.kachel@iphc.cnrs.fr] - IPHC

Available resources, existing funding and frameworks

Table 12 shows the staff and funding currently assured in participating institutes from the relevant funding framework for an initial three-year project duration. The values are given as averaged annual amounts.

Table 12: Available resources and areas of contribution numbered as in Section B.2.2.

Institute	**Framework**	**Areas of Contribution**
CERN	EP R&D	3. and USER
IPHC Strasbourg		1.
Total available per year	**FTE/yr**	**Annual Funding** [EUR]
2024	3.0	0
2025	3.0	0
2026	3.0	0
$\gg$ 2026	3.0	0

Plans for resource requests

Table 13 shows the funding requests to be made by participating institutes from the relevant funding framework. Not all aspirations are available at this time.

Table 13: Planned resource requests. Granted volume not yet available.

Institute	**Framework**	**Request submission year**
CERN	EP R&D	2023
IPHC Strasbourg		2023

B.3 Work Package 7.3: 4D and 5D techniques

B.3.1 Project 7.3a: High performance TDC and ADC blocks at ultra-low power

This project aims to develop ultra-low power high performance TDC and ADC blocks for use in a wide range of future particle physics experiments.

Project Name	High performance TDC and ADC blocks at ultra-low power (WG7.3a)
Project Description	Development of high performance, ultra-low power TDC and ADC blocks. Duration 3 years. A further extension is planned after 3 years.
Innovative/strategic vision	Develop high-performance, ultra-low power TDC and ADC blocks in advanced CMOS technologies, ready to be deployed as key components of SoC readout ASICs for a variety of future particle detectors.
Performance Target	High resolution ($\sim$ 10ps) TDC and medium-high resolution (10-14 bits) fast sampling (>40 MSps) ADC blocks. High performance, especially ultra-low power consumption, should be confirmed with a very good Figure of Merit, compared to the state-of-the-art solutions obtained using the same CMOS technology and characterized by similar parameters
Milestones and Deliverables	**M7.3a.1** (M12) Report on design of ADCs and related blocks **M7.3a.2** (M12) Report on design of TDCs and related blocks **M7.3a.3** (M24) Progress report on development of ADCs and related blocks **M7.3a.4** (M24) Progress report on development of TDCs and related blocks **D7.3a.1** (M36) Delivery of prototype ASICs of ADCs and related blocks **D7.3a.2** (M36) Delivery of prototype ASICs of TDCs and related blocks.
Multi-disciplinary, cross-WG content	TDCs and ADCs are common blocks of readout ASICs for wide range of detector systems.
Contributors	AT: TU Graz ES: ICCUB FR: CEA IRFU, CPPM, IP2I, OMEGA KR: DGIST PL: AGH US: SLAC
Available resources	7.3 FTE/yr 500k/yr
Addt'l resource need	7.3 FTE/yr 280k/yr

Project Description

In newly designed particle physics detection systems, there is a growing demand for detectors with ever-increasing speed, high channel density, and precise measurement of time and signal amplitude in each channel. This can be done only when time or amplitude domain digitization is done at ultra-low power per channel. An ultra-low power, area-efficient, high-speed Analog-to-Digital Converter (ADC) and precise Time-to-Digital Converter (TDC), are two essential components of a high-performance SoC readout ASIC. Many multi-channel readout ASICs in different detectors at LHC and other future experiments require a high-performance medium-high resolution (10-14 bits) ADC with a sampling rate of 40 MSps or higher, and a precise ($\sim$ 10ps) ultra-low power compact TDC. With technology scaling, the TDC quantization resolution is not affected by reduced supply

voltage and can be designed flexibly by tuning the latency of the delay cells, making the TDC an appropriate candidate for low supply applications.

The project will address the development of high-performance TDC and ADC blocks in technologies commonly used by the detector community, such as 130/65/28 nm CMOS, for a variety of detectors in future HEP experiments. Other blocks directly related to ADC/TDC, essential for their high performance (like opamps, serializers) or possibly front-end electronics, will also be part of the project. Since the developed blocks can be used in a high radiation environment with doses reaching many hundreds of Mrad, radiation hardness verified technologies will be used during design and precautions will be taken to improve radiation hardness. Where relevant, the radiation hardness tests will also be performed.

The project will feature various topics to be addressed by different collaborators:

1. ADC design,
2. TDC design,
3. Design of analog blocks essential for ADC or TDC (e.g. opamp),
4. Design of digital blocks essential for ADC or TDC (e.g. DLL, PLL, serializer),
5. Front-end electronics design : full channels with preamps, ADCs and TDCs.

The achieved results will be communicated through reports, conference presentations, scientific articles. Completed ADC and TDC blocks will be documented and documentation will be available to the community. The availability of the developed blocks would require further consideration, both due to licensing or radiation hardness restrictions, as well as intellectual property issues.

The project is originally planned to last 3 years. As the development of high-performance ADC and TDC blocks will continue with architectural and technological improvements, it is planned to extend it after 3 years.

Performance Target

Since different detectors have different requirements for precision in measuring amplitude or time, ADCs/TDCs blocks with different specs are needed. Short-term developments use 130/65 nm CMOS, while smaller feature size processes such as CMOS 28 nm will be used in R&D works for long-term applications. The performance of the ADC/TDC block, mainly speed and power, will strongly depend on the technology used, but one of the main goals for each developed block is ultra-low power, confirmed by a very good Figure of Merit, compared to state-of-the -art developments for a given technology. Some of the development work already started is briefly listed below, along with the main characteristic parameters. Other R&D projects, not yet fully defined, will be launched in the near future.

ADC projects already underway:

- 130/65 nm CMOS. Various fast sampling ($> 40MSps$) and ultra-low power ($FOM < 25fJ/conv. - step$) ADCs are being developed for HL-LHC detector upgrades and other applications. For detectors requiring lower resolution, 10-bit ADCs with expected power consumption of about 0.5-1 mW are designed (AGH). For higher resolution applications such as 5D calorimetry, 12-bit ADCs designs are underway (AGH, CEA IRFU, ICCUB).
- 28 nm CMOS. To achieve better performance (higher sampling rate and lower power) than in 130/65 nm CMOS, R&D work began on high-performance ADCs in CMOS 28 nm. One of development focuses on 100-200 MSps 10-bit ADC with $FOM < 10fJ/conv. - step$ (AGH, SLAC). Other development effort aims to sample waveform much faster, at 16 GS/s, with a small area ($300 \times 200\ \mu m^2$) ADC but at lower resolution of around 7-8 bits (DGIST).

TDC projects already underway:

- 130/65 nm CMOS. Fast sampling (10-40 MSps), high resolution (time bin $\sim$ 20ps), low-power ($< 2\ mW$) TDCs are being developed for future LHC detectors and other fast timing applications (CEA IRFU, ICCUB), mainly for ToA, but also for ToT measurements. The

design of a TDC for monolithic pixel applications has also been started in TPSC0 65nm (IP2I).

- 28 nm CMOS. To achieve better performance at lower power TDC projects in CMOS 28 nm have been initiated. One of the projects aims to develop fast ($40MSps$) TDC with ultra-low power ($\sim 18\ \mu W$@10% occupancy) and 6.25 ps timing resolution, for future 4D trackers and 5D calorimeters (SLAC). In another project, a TDC with lower timing resolution ($< 40\ ps$), low-power ($\sim 5\ \mu W$@0.1% occupancy), and small area ($\sim 200\ \mu m^2$) is designed for pixel detectors in HL-LHC and future linear collider (CPPM). Both projects use rad-hard design techniques to achieve rad-hard TDCs up to 1-2 Grad dose. A TDC radiation hardness studies are also performed (TU Graz).

If not mentioned above, radiation resistance is not precisely defined yet. For applications intended for LHC detectors, doses in the range of several tens to several hundred Mrad are typically expected and targeted (except for innermost detectors). For other applications, expected doses are lower. In parallel to ADC and TDC core blocks other important circuits, necessary for integration into the complete signal processing chain of the front-end electronics, such as differential amplifiers (AGH, OMEGA, SLAC), PLLs and DLLs (AGH, CEA IRFU, CPPM, ICCUB, SLAC), constant fraction discriminators (SLAC) are being developed too. The first joint development of a complete ultra-low power ($\sim 5mW$) front-end channel, including analog front-end electronics with ADC and TDC, for use in future 5D calorimetry has also been initiated (AGH, CEA IRFU, OMEGA).

Milestones and Deliverables

- **M7.3a.1** (M12) Report on the design of prototype ADCs and their related blocks by different groups in different CMOS technologies
- **M7.3a.2** (M12) Report on the design of prototype TDCs and their related blocks by different groups in different CMOS technologies
- **M7.3a.3** (M24) Progress report on the development of prototype ADCs and their related blocks by different groups in different CMOS technologies
- **M7.3a.4** (M24) Progress report on the development of prototype TDCs and their related blocks by different groups in different CMOS technologies
- **D7.3a.1** (M36) Delivery of prototype ASICs of ADCs and their related blocks produced by different groups in different CMOS technologies. Measurement results will be provided along with the prototypes.
- **D7.3a.2** (M36) Delivery of prototype ASICs of TDCs and their related blocks produced by different groups in different CMOS technologies. Measurement results will be provided along with the prototypes.

Multi-disciplinary, transversal content

Time or/and amplitude measurement at ultra-low power is a common concern in high-density high-speed detectors for future HEP experiments. TDC and ADC blocks with different specs, designed in technologies used by detector community, are needed in complex SoC readout ASICs for many detectors. The developed ADC and TDC blocks will find use across the wide range of detector systems being considered by the 2021 ECFA Detector R&D Roadmap.

Contributors and areas of competence

- **AGH**: large track record in mixed-mode front-,end ASICs and in particular in ADC design with leading contributions to LHC and FAIR experiments. Recently: SALT for UT LHCb, contributions to HGCROC for CMS HGCAL and TOFHIR for CMS MTD

- **CEA IRFU**: expertise in low noise and mixed-mode front-end radiation hardened ASIC and in particular TDC, PLL designs with leading contributions to LHC experiments. Recently: contribution to HGCROC for CMS HGCAL
- **CPPM**: the Marseille Particle Physics Center has been involved for several years in the development and construction of the ATLAS detector. The CPPM group is collaborating on the design, testing, and construction of the inner detector. Since 2014, CPPM has been involved in the RD53 readout chip design.
- **DGIST**: expertize in IC design for ultra-high-speed/low-power mixed-signal circuit design with a moderate resolution in advanced CMOS technology. Recent records focus on the ADC designs in CMOS technologies for a wide range of applications from biomedical applications to ultra-high-speed data communication.
- **ICCUB**: long track record in dvelopment og mixed-mode ASICs for particle physics, space missions and medical imaging. Recently: ICECAL for LHCb calorimeter, PACIFIC for the LHCb Scintillating fiber tracker and FastIC/FastRICH for future LHCb upgrades (the 2 latter in collaboration with other groups).
- **IP2I**: expertise in development of TDC and in leading implementation of a full precision timing readout chain in an IN2P3 R&T Master Project (FASTIME) in 130 nm TSMC technology.
- **OMEGA**: large track record in mixed-mode front-end ASICs with leading contributions to LEP and LHC experiments. Recently: HGCROC for CMS HGCAL, ALTIROC for ATLAS HGTD and EICROC for EIC.
- **SLAC**: large track record in mixed-mode front-end ASICs and in particular ADC and TDC design with leading contributions to LHC and photon science experiments. Recently: ALTIROC for ATLAS HGTD
- **TU Graz**: expertize in IC reliability with focus on radiation tolerance, aging, electromagnetic compatibility (onchip and system) and noise effects in IC, studies include robust architectures to mitigate the environmental influence and stress effects.

Project contact person: Marek Idzik, AGH University of Krakow

Available resources, existing funding and frameworks

Table 14 shows the manpower and funding currently assured in participating institutes from the relevant funding framework for an initial three-year project duration. The values are given as averaged annual amounts.

Estimate of to be requested resources

Table 15 shows the manpower and funding foreseen to be requested by participating institutes from the relevant funding framework. Not all aspirations are available at this time.

Table 14: Available resources and areas of contribution numbered as in Section B.3.1.

Institute	**Framework**	**Areas of Contribution**
AGH	PL R&D	**1**,2,**3**,**4**,**5**
CEA IRFU	Institute	1,**2**,**4**
CPPM	IN2P3	**3**,**5**
DGIST	DGIST R&D	**1**,3,**4**
ICCUB	ES R&D	1,**2**,**3**,**4**,**5**
IP2I	IN2P3	**2**,**4**
OMEGA	IN2P3	**3**,**4**,**5**
SLAC	DOE's HEP Detector R&D program, DOE's Accelerate Innovations in Emerging Tech.	**1**,**2**,**3**,**4**,**5**
TU Graz	Institute	2,3,4
	FTE/yr	**Annual Funding** [EUR]
Total available	7.3	500k

Table 15: Resources to be requested. One should consider that requests will be answered in the year following submission.

Institute	**Framework**	**Request submission year**
AGH	PL R&D	2024
CEA IRFU	...	2025
CPPM	IN2P3 R&T	2024
DGIST	Europe/Korean R&D	2024
ICCUB	ES/EU R&D	2025
IP2I	IN2P3 Master project framework	2025
OMEGA	IN2P3 R&T	2024
SLAC	DOE's HEP Detector R&D program	2024
TU Graz	Austrian Science Fund	2024
	FTE/yr	**Annual Funding** [EUR]
Total to be requested	7.3	280k

B.3.2 Project 7.3b1 Strategies for characterizing and calibrating sources impacting time measurements

This project aims to study and propose generic data-driven calibration strategies for the time measurements in detectors requiring high precision timing. These include simulation, impact studies and data-based calibration strategies of phase variations in all or part of the detector timing distribution tree (for example jumps due to resets in the electronics system and or temperature dependent phase drift), as well as the calibration of the front-end TDC timewalk and non-linearities.

Project Name	Strategies for characterizing and calibrating sources impacting time measurements (WG7.3b1)
Project Description	Generic data-driven impact studies and calibration strategies of phase variations for timing detectors. Duration 3 years.
Innovative/strategic vision	First opportunity to have a common strategy between the different experiments for data-driven timing studies.
Performance Target	Design of a protocol of measurement. Development of simulation tools in the different experiments. Definition of common figures of merit. Measurement of the properties in test facilities to compare with the predictions. Design of calibration chain inside the different experiments.
Milestones and Deliverables	**D7.3b1.1** (M12) Delivery of a report summarising common metrics and description of the effects for simulation **M7.3b1.1** (M24) Implementation of measurements on realistic DAQ chain **D7.3b1.2** (M36) Delivery of a report summarising the items (hardware or software) to be improved for the next generation of experiments.
Multi-disciplinary, cross-WG content	Concerns all state-of-the-art timing detectors and therefore requires a unified approach which is proposed by this project. Reciprocal reports with DRD7.3a & 7.3b2
Contributors	CERN: ATLAS HGTD, CMS HGCAL FR: Université Clermont Auvergne. CNRS-IN2P3, LPCA (ATLAS HGTD) US: Boston University (CMS ETL)
Available resources	1.5 FTE/yr (ATLAS & CMS core funds) 0 kEUR[1]
Addt'l resource need	0 FTE 0 kEUR[1]

[1] The teams will have full access to simulation processors, detector simulation data & test-benches

Project Description

In view of the unprecedented High-Luminosity conditions of the LHC, both ATLAS and CMS experiments have planned to upgrade their detectors, adding precise timing information to resolve the bunch crossing structure. This information is particularly essential in the forward region, where the tracking resolution is degrading.

For ATLAS, the High Granularity Timing Detector (HGTD) aims at complementing the new all-silicon Inner Tracker (ITk) of ATLAS, for pseudo rapidity between 2.4 and 4.0. Composed of four layers of Low Gain Avalanche Diodes (LGADs) it can provide an average time resolution per track ranging from 30 ps to 50 ps at the end of the HL-LHC phase. The CMS experiment proposes two new detectors, the High Granularity Calorimeter (HGCAL) and the MIP Timing Layer (MTD), which is composed of the Barrel Timing Layer (BTL) and the Endcap Timing Layer (ETL). The HGCAL sensors provide measurements of both energy and timing, with an expected

resolution of about 30 ps for high energetic electromagnetic and hadronic showers. Similarly to HGTD, the ETL consists of 2 layers of LGAD sensors with an expected resolution ranging from 35 ps to 60 ps at the end of life.

While the sensors are giving an important contribution to the total time resolution (ranging from 25 to 30 ps for a MIP (Minimum Ionizing Particle) detector), external effects, such as the LHC clock distribution and stability have an important impact to the measurement. To reach the precision required by the different experiments to affect the physics, it is thus crucial to understand the source of these biases to act on them. Furthermore, the universal character of these effects and their recent investigations, implies to have a common strategy between the different experiments and could pave the way to the design of future detectors.

In this project, we propose to study generic data-driven calibration strategies for this purpose. This includes:

- Developing a coherent simulation of all the factors impacting the time measurement;
- Constructing a set of figures of merit to asses the calibration;
- Studying the impact of the different factors and their mitigation, including (but not limited to):
  - phase variations in all or part of the detector timing distribution tree, like jumps due to resets in the electronics system and or temperature dependent phase drift;
  - timewalk effect of the TDC and other non-linearities.

Given the habits of the two experiments involved, this work will be conducted as a general forum of exchange of non sensitive information. It will help to foster collaboration at a higher scale, similar to the current High Precision Timing Distribution project, with a slightly different scope.

Performance Target

Several areas of development are identified:

1. Design of a protocol of measurement;
2. Development of simulation tools in the different experiments;
3. Definition of common figures of merit and estimation of their impact on detector's performance;
4. Measurement of the properties in test facilities (unique for each experiment) to compare with the predictions;
5. Design of calibration chain inside the different experiments.

Milestones and Deliverables

It is thought that they could be completed in about three years for existing detectors depending on the feedback from the various participating groups:

- **D7.3b1.1** (M12) Delivery of a report summarising common metrics and description of the effects for simulation.
- **M7.3b1.1** (M24) Implementation of measurements on realistic DAQ chain (unique for each experiment).
- **D7.3b1.2** (M36) Delivery of a report summarising the items (hardware or software) to be improved for the next generation of experiments.

These areas should attract increasing interest inside the community, initially during the transition phase towards commissioning and operation of HL-LHC timing detectors and then with the emergence of future detectors with even more stringent requirements in terms of timing stability and precision.

Multi-disciplinary, transversal content

This question concerns all state-of-the-art timing detectors and therefore requires a unified approach which is proposed by this project. It also requires close interactions between timing simulation physicists and engineering.

Contributors and areas of competence

- **CERN**: Several members of the CERN group are involved in the ATLAS and CMS project, with a specific expertise in ASIC simulation.
  - ATLAS: Simulation of ASIC jitters.
  - CMS: HGCal Simulation of timing effects, calibration.
- **Université Clermont Auvergne. CNRS-IN2P3, LPCA** (called LPCA hereunder): ATLAS HGTD: Long lasting experience with the calibration of the detector (initial internal studies) and the simulation of time shifts and jitters.
- **Boston University**: CMS ETL early studies performed on the simulation of time shifts and jitters, good interest of the team into the calibration.

The project will be co-managed by two chairs, one from ATLAS and one from CMS. For 2024:

- **co-chair**: Louis d'Eramo CERN
- **co-chair**: Giacomo Zecchinelli Boston University

Available resources, existing funding and frameworks

Table 16 shows the person-power and funding currently assured in participating institutes from the relevant funding framework for an initial three-year project duration. The values are given as averaged annual amounts.

Table 16: Available resources and areas of contribution numbered as in Section B.3.2.

Institute	**Framework**	**Areas of Contribution**
CERN	ATLAS & CMS HGCal	1,2,3,4,5
LPCA	ATLAS HGTD	1,2,3,4,5
Boston University	CMS ETL	1,2,3,4,5
	FTE/yr	**Annual Funding** [EUR]
Available 2024	1.5	0 kEUR[1]
Available 2025	1.5	0 kEUR[1]
Available 2026	1.5	0 kEUR[1]
Available >2026	1.5	0 kEUR[1]
Total available (2024-2026)	4.5	0 kEUR[1]

[1] The teams will have full access to simulation processors, detector simulation data & test-benches

Estimate of to be requested resources

Table 17 shows the personpower and funding foreseen to be requested by participating institutes from the relevant funding framework. Not all aspirations are available at this time. As explained in Section B.3.2, this forum only requires human resources, the hardware component being developped by each experiment.

Table 17: Resources to be requested. One should consider that requests will be answered in the year following submission.

Institute	**Framework**	**Request submission year**
LPCA	FR IN2P3 Funding	2024 (tbc)[1]
Boston University	D.O.E. funding	2024 (tbc)[1]

[1] The teams will have full access to simulation processors, detector simulation data & test-benches

B.3.3 Project 7.3b2: Timing Distribution Techniques

This project aims to study and propose strategies to optimize and assess ultimate precision and determinism of timing distribution systems for future detectors. The precision target of upcoming timing detectors is now enforcing new figures of merit to be taken into account in addition to the traditional random jitter, such as clock phase stability and determinism (at picosecond level). Such metrics are systems- and COTS-specific and need to be carefully assessed. In addition, generic solutions shall be provided to mitigate the various kinds of instabilities brought by the selected components. This project will be carried out in tight collaboration with its counterpart project based on simulation (7.3b1): Strategies for characterizing and calibrating sources impacting time measurements.

Project Name	Timing Distribution Techniques (WG7.3b2)
Project Description	Bench-marking of the performance of COTS- or custom-based solutions to assess achievable timing precision and determinism. Investigation of generic solutions to mitigate the observed limitations.
Innovative/strategic vision	Common effort of the community to explore limits of COTS and reach ambitious timing precision not targeted by commercially available solutions
Performance Target	Develop and compare implementations on different COTS and custom platforms. Studies and implementation of FPGA-agnostic or ground-breaking solutions to improve phase stability.
Milestones and Deliverables	**M7.3b2.1** (M12) Specification for a light-weight timing and synchronization protocol also capable of passing fixed latency messages **D7.3b2.2** (M18) Deliver a report comparing the phase determinism of various FPGAs (PolarFire, Agilex, Versal) and potential mitigation mechanisms **D7.3b2.3** (M18) Delivery of first demonstrators of the light-weight protocol, and of a generic deterministic link based on AMD FPGAs and DDMTD + DCPS ASICs from University of Minnesota **M7.3b2.2** (M18) Submission of a unique chip for Phase Monitoring and Phase Shifting (PMPS) **D7.3b2.4** (M24) Delivery of a report on White Rabbit for 4D detectors and for Agilex FPGA **D7.3b2.5** (M36) Delivery of a report summarising a proof of concept demonstration of a FPGA-Agnostic Cascaded Link (FACL) with PMPS ASIC. **M7.3b2.3** (M60) Example of a Milestone if the project continues in Phase II: Implementation of a proof of concept of a FACL with future chips from CERN (SysPIC2 and SysPhDem) as an End-Node.
Multi-disciplinary, cross-WG content	Distribution is critical and universal to all detectors requiring timing. DRD7.3b1 and 7.3b2 will feed each other with simulation and assessed figures
Contributors	CERN: HPTD team ES: CIEMAT, ITAINNOVA, CSIC (IFCA & IMB-CNM) FR: IN2P3 (CPPM, IJCLab) UK: Bristol University NL: Nikhef USA: The University of Minnesota
Available resources	18.7 FTE, 310kEUR over 3 years
Addt'l resource need	10.6 FTE, 485kEUR over 3 years

Project Description

With the increase of luminosity in future colliders, the need of timing detectors with very high resolution is rapidly increasing. This requires the collision clock signal to be distributed with very high precision and stability (o(ps)). However, high determinism of clock and data recovery solutions at picosecond levels is not a high priority of COTS manufacturers. Limits need therefore to be explored for these solutions and implementation must be carefully studied and optimized in order to achieve this challenging goal.

The project will feature various topics to be addressed by different collaborators in order to cover several aspects of this topic. These are:

- Explore limits for these solutions: Develop and compare implementations on different COTS and custom platforms. Assess their ultimate performance.
- Carefully study and optimize implementation: Study and implement solutions to improve phase stability and mitigate non-determinism
- Explore alternative ways of distributing timing.

This project will be handled as a forum where results, plans, ideas and challenges will be openly and regularly shared between the participating teams. It will be chaired on a rotating basis.

Performance Target

Several parallel and complementary studies (Themes) are proposed by the participating institutes:

- *Theme 1*: Precise & deterministic timing distribution study with Microsemi and AMD FPGAs (CIEMAT, Nikhef)
- *Theme 2*: Precise & deterministic timing distribution study with Intel FPGAs (IN2P3 CPPM)
- *Theme 3*: White Rabbit Implementation on Intel based Back-End boards (IN2P3 IJCLab)
- *Theme 4*: White Rabbit Clock distribution system prototype for 4D detectors (ITAINNOVA, IFCA, IMB-CNM)
- *Theme 5*: Generic solutions for precise and deterministic clock distribution with non-deterministic COTS and custom ASICs (CERN, University of Minnesota)
- *Theme 6*: New protocol development for precise & deterministic clock and timestamp distribution for future non LHC experiments (Bristol University)

Milestones and Deliverables

- **M7.3b2.1** (M12) Specification for a light-weight timing and synchronization protocol also capable of passing fixed latency messages, implementable in a wide range of COTS hardware and targeting a small footprint if implemented in an ASIC, and aiming for alignment of clocks at timing endpoints of better than 10ps RMS (report) - Theme 6
- **D7.3b2.2** (M18) Delivery of a report on compared phase determinism of various FPGAs (PolarFire, Agilex, Versal) and potential mitigation mechanisms - Themes 1 and 2.
- **D7.3b2.3** (M18) Delivery of first demonstrator of a generic deterministic link based on AMD FPGAs and DDMTD + DCPS ASICs from University of Minnesota (a paper will be written) - Theme 5.
- **M7.3b2.2** (M18) Submission of a unique chip for Phase Monitoring and Phase Shifting (PMPS) - Theme 5.
- **D7.3b2.4** (M24) Delivery of a report on White Rabbit for 4D detectors and for Agilex FPGA - Themes 3 and 4.

- **D7.3b2.5** (M36) Delivery of a report summarising the proof of concept of a single FPGA-Agnostic Cascaded Link (FACL) with PMPS ASIC (a paper will be written and the firmware and hardware IPs will be made available in Gitlab) - Theme 5.

- M7.3b2.3 (M60) An outlook towards a potential Phase-II of this 7.3b2 project is the implementation of a proof of concept of a FACL or of the light-weight protocol with future devices from DRD7.1 and CERN EP RnD Work Package 6 as End-Node. These components are expected for mid 2028 in the framework of CERN EP RnD work package 6 - Themes 5 and 6.

Multi-disciplinary, transversal content

This activity is universal across HEP for detectors requiring precision timing. DRD7.3b1 and 7.3b2 will feed each other with simulation and assessed figures.

Contributors and areas of competence

The main contributors for this project are:

- **Bristol University**: Long expertise in electronics for detectors, and timing distribution of Dune.

- **CERN**: Activity hosted in the HPTD (High Precision Timing Distribution) team. 20 years of expertise in timing distribution, HPTD Interest Group Coordination

- **CIEMAT**: Activity hosted in a group of 4 people with long term expertise developing, testing and commissioning electronics systems for HEP in the framework of the CMS experiment.

- **IN2P3 (CPPM & IJCLAB)**: Activity hosted in a team of 4.5 FTE which involves 5 IN2P3 labs and CERN teams already including specialists of software, hardware, firmware currently involved in White Rabbit development with research and technology (R&T) project. IJCLab has at its disposal test and qualification setups from the Paris Observatory (SYRTE).

- **ITAINNOVA, CSIC (IFCA & IMB-CNM)**: Activity hosted in a group of 6 people in electronics for particle physics for 25 years (CMS Pixel upgrade, CMS ETL, RD53, ETROC).

- **Nikhef**: Activity hosted in a group of 2 people in the Electronic Technology department, with expertise on timing distribution (FELIX and White Rabbit).

- **University of Minnesota** Long expertise in detector design and construction. Expertise in custom electronics for detectors, precision clock distribution using COTS and in ASIC design.

The project will be managed on a rotational basis, with one year's deputy project manager becoming the project manager the following year. For 2024:

- **Project Leader**: Sophie Baron (CERN)

- **Deputy**: Javier Galindo (Itainnova)

Available resources, existing funding and frameworks

Table 18 shows the manpower and funding currently assured in participating institutes from the relevant funding framework for an initial three-year project duration. The values are given as averaged annual amounts.

Estimate of to be requested resources

Table 19 shows the manpower and funding foreseen to be requested by participating institutes from the relevant funding framework. Not all aspirations are available at this time.

Table 18: Available resources and areas of contribution numbered as in Section B.3.3.

Institute	**Framework**	**Areas of Contribution**
CPPM CNRS/IN2P3	FR IN2P3 Funding	Theme 2
Bristol University	UK R&D	Theme 6
CERN	CERN EP R&D	Theme 5
CIEMAT	Spanish R&D funding	Theme 1
CSIC (IFCA/IMB-CNM)	Spanish R&D funding	Theme 4
IJCLab CNRS/IN2P3	FR IN2P3 Funding	Theme 3
ITAINNOVA	Spanish R&D funding	Theme 4
Nikhef	NL R&D funding	Theme 1
University of Minnesota	DOE Instrumentation R&D	Theme 5
	FTE/yr	**Annual Funding** [EUR]
Available 2024	7.2	162.5k
Available 2025	6.8	117.5k
Available 2026	4.7	30k
Available >2026	3.6	10k
Total available (2024-2026)	18.7	310k

Table 19: Resources to be requested. One should consider that requests will be answered in the year following submission.

Institute	**Framework**	**Request submission year**
CPPM CNRS/IN2P3	FR IN2P3 Funding	2024
CERN	CERN EP R&D	2026
CIEMAT	Spanish R&D funding	2024
CSIC (IFCA/IMB-CNM)	Spanish R&D funding	2024
IJCLab CNRS/IN2P3	FR IN2P3 Funding	2023/2024
ITAINNOVA	Spanish R&D funding	2024
Nikhef	NL R&D funding	2024
University of Minnesota	DOE Instrumentation R&D	2023
	FTE/yr	**Annual Funding** [EUR]
To be requested 2024	2	50k
To be requested 2025	3	170k
To be requested 2026	5.6	265k
To be requested >2026	7.1	265k
Total To be requested (2024-2026)	10.6	485k

B.4 Work Package 7.4: Extreme environments

B.4.1 Project 7.4a: modelling and Development of Cryogenic CMOS PDKs and IP

The project will focus on cryogenic device modelling from selected CMOS technology nodes, the development of "cold" Process Design Kits (PDKs) and mixed-signal CMOS IP blocks and mixed-signal demonstrator chips for cryogenic operation.

Project Name	Device modelling and Development of Cryogenic CMOS PDKs and IP (WG7.4a)
Project Description	Device modelling from selected CMOS technology nodes, development of "cold" Process Design Kits (PDKs), design and characterisation of mixed-signal CMOS IP blocks and demonstrator chips for photon detection in (LAr, LXe) noble liquid experiments, quantum computing interface and sensing.
Innovative/strategic vision	The aggregation of the international research teams will create the critical mass needed for the construction of infrastructures and tools, needed for device characterisation and modelling , towards the development of Cold PDKs and cold-IP blocks. These will be made available to a wider community working towards the construction of frontier particle and photon cryogenic detectors.
Performance Target	Cold PDK for a deep sub-micron CMOS technology, with temperature corners at 165-87-77-4K, Cold IP blocks demonstrated on board of a multi-channel mixed-mode demonstrator chip.
Milestones and Deliverables	**D7.4a.1** (M9) Deliever a specification and requirements document for a full-chip demonstrator. **M7.4a.2** (M18) Cold-PDK for TSMC28nm complete **M7.4a.3** (M26) Tapeout of full-demonstrator chip **D7.4a.4** (M38) Deliver a report of full-demonstrator silicon chip characterisation.
Multi-disciplinary, cross-WG content	The availability of reliable device models and PDKs for advanced CMOS technology nodes, qualified for operation at cryogenic temperatures, will pave the way for the development of cryo-qualified CMOS IP blocks suitable for integration on complex mixed-signal ASICs for DRD2 and DRD5.
Contributors	Graz University of Technology (Austria) University of Sherbrooke (Canada) Forschungszentrum Jülich (Germany) INFN (Italy) KEK (Japan) ICCUB, University of Barcelona (Spain) EPFL (Switzerland) RHUL (UK) University of Oxford (UK) Fermilab (US)
Available resources	5.4 FTE/yr 46k/yr
Addt'l resource need	6.3 FTE/yr 184k/yr

Project Description

Modern CMOS technologies are qualified down to -40C and, although the extrapolation of the device models down to 77K was verified with VDSM bulk CMOS and FDSOI technology nodes,

cold PDKs are fundamental for the development of complex mixed-signal ASICs implementing innovative detector architecture and concepts, data transfer, readout and control. Future Noble Liquid detectors for dark matter searches, neutrino physics, quantum computing interface electronics and quantum sensing will require integrated electronics operating down to the 87K and 4K/100mK temperature ranges, respectively. Some foundries are already working on the development of cryo-capable nodes (e.g. GF 22nm FD-SOI or SkyWater, which offers a 90nm node with cryo-models at 45K-77K-120K-150K) and it is reasonable to assume that the growing interest on the use of CMOS for Quantum Computing and Quantum Sensing could open new opportunities for collaborative efforts with selected silicon foundries on the optimisation of solid-state sensors and CMOS processes for operation at cryogenic temperatures.

The aggregation of the international research team participating to the project will create the critical mass and infrastructures' network needed to work on device characterisation, development of reliable models and PDK deployment on advanced CMOS for cryogenic temperatures. The project will select the TSMC 28nm as baseline technology node, while for the TSMC 65nm 87K corners will be made available by Fermilab. While the project aims to have the initial involvement of an industrial partner for the cold-PDK design, the availability of new funding and resources will allow to create infrastructures, tools and competences for in-house cold-PDK development. The potential applications of these IP blocks and design framework include photon detection in Liquid Argon and Liquid Xenon experiments for astroparticle physics, and CMOS interface circuitry for quantum computing and sensing. Consequently, the project will explore temperature corners spanning from 165K-87K down to 4K.

The design teams will, in parallel, develop core mixed-signal IPs optimised for low-temperature operation, such as ADCs, TDCs, DACs, LVDS transceivers, SPI, bandgaps and power management circuits. The project will also support the characterisation, documentation and git repository of such Cold-IP Library. The design groups will work on the development of a small-scale (MPW) cold demonstrator single-photon detector chip for fast timing applications implementing a low-power and scalable architecture. The use of a digital-on-top integration flow on such a multi-channel mixed-signal IC will allow for the demonstration of the cold-PDK capabilities for the implementation of system-ready complex designs.

Performance Target

The overall goal of this project is to develop tools and infrastructures for device parameter extraction and modelling of selected CMOS technology nodes at cryogenic temperatures, and the development of cryo-qualified CMOS IP blocks and integration flows for the design of complex multi-channel ASICs for photon and particle detection implementing innovative and scalable architectures. The characterisation of test structures and parameter extraction will make use of the facilities already installed at Fermilab, EPFL and FZJ. These groups will then join the IC design and characterisation team, which also include ICCUB, TU Graz, KEK, U. Sherbrooke, INFN and RHUL/Oxford. The project will develop innovative IP blocks and a full-scale photon sensor demonstrator chip for operation at temperatures down to 4K.

Milestones and Deliverables

- **D7.4a.1** (M9) Deliever a specification and requirements document for a full-chip demonstrator.
- **M7.4a.2** (M18) Cold-PDK for TSMS28nm complete.
- **M7.4a.3** (M26) Tapeout of full-demonstrator chip.
- **D7.4a.4** (M38) Deliver a report of full-demonstrator silicon chip characterisation.

The specification and requirements document for a full-chip demonstrator will be delivered after a wide discussion with the community working on the research towards innovative noble-liquid detectors for astroparticle physics, as well as the groups developing sensing and interface electronics for quantum computing. The development of the cold-PDK, which includes the fabrication of test structures, characterisation and modelling, will start with the kick-off of the project and does not

gate the IP design activities. General purpose IPs will be adapted from WG7.3.1 and the design of custom cold IP blocks, as well as the chip integration and verification flows, will start using the foundry's standard CMOS PDK. The availability of the cold-PDK with a float time of 8 months in respect to the full-chip tapeout should allow for a thorough verification task before the chip fabrication.

Multi-disciplinary, transversal content

The availability of reliable device models and PDKs for advanced CMOS technology nodes, qualified for the design of mixed-signal circuits and full-chip integration and sign-off of complex ASICs targeting operation at cryogenic temperatures, will pave the way for the development of core IPs and chips for other DRDs: e.g. DRD2 (Liquid Detectors) and DRD5 (Quantum and Emerging Technologies). A substantial amount of the modelling activity would apply just as well to radiation models, thereby a consistent synergy with Project 7.4b "Radiation resistance of advanced CMOS nodes" is foreseen. Moreover, the development of innovative cold IP blocks will benefit from a strong synergy with Project 7.3a: "High performance TDC and ADC blocks at ultra-low power".

Since the modelling, PDK and IP core qualification tasks will extend to temperature range below 4K, the results of this research project could find application in the field of quantum computing and generate potential for technology transfer towards industrial applications.

Contributors and areas of competence

- WP1: CMOS Cold Process Design Kit development and parameter extraction
  - FZJ: characterisation circuits and participation in cryo-measurements. FZJ is currently characterising a 22nm FD-SOI technology for a cryo-PDK.
  - Fermilab/EPFL: development of cryo-PDK (BSIM-IMG) for 22nm FDSOI well under way in collaboration with Synopsys, cryogenic models and libraries for extended lifetime developed for 65nm, 4K and 55K dry closed loop cryostat, development of simplified EKV models for analog design (with EPFL). Also currently working on AI/ML deep-learning modelling for extreme environments (including cryo operation). Collaboration with GF for upcoming cryoPDK for their 28nm HV process.
  - INFN: PAC200 Cryoprobe for 8-inch wafer measurements at 77K currently operating at INFN-LNGS, needed for wafer-level characterisation, mismatch and yield measurements; Smaller setups and dry cryostats for LN characterisation.
  - RHUL/Oxford: operations down to ULT (in the London Low Temperature Laboratory has cryostats reaching 100 microKelvin, first ASIC operations at 1K expected soon). Currently using available setups for ASIC measurement at 4K.
- WP2: CMOS IP development, mixed-signal ASIC demonstrator design and characterisation
  - U. Sherbrooke: Small SPAD array with readout chain including TDC.
  - FZJ: Design of bandgap, voltage regulators and power management, flexible/scalable ADC, DACs, PLLs; extensive RT and cryo verification capabilities available.
  - ICCUB: Readout ASICs for SiPMs in RICH and PID detectors focused to "mild" cryogenic operation (required due to sensor radiation damage).
  - TU Graz: Focus on 28nm variability and aging at cryo-temperatures. Characterisation of IPs currently in design (28nm: LDO, TDC,) with respect to longevity (accelerated stress). Improved developments for these IPs and further IP blocks.
  - Fermilab: currently focusing on 22nm FDSOI: large portfolio of chips and circuit blocks for 4K operation (PLL, VCO, ADC, SRAM, NN for anomaly detection, low power DACs, 5ps resolution TDC, etc.). For 65nm: circuit blocks (LVDS Rx and Tx, POR, Bandgap, etc) plus custom 90nm standard cell digital library for longevity (230 cells, including STA libraries). Collaboration with GF for development of cryo SPADs (LAr, LN2).

- KEK: Readout ASICs for liquid-Ar detectors, custom IPs (ADC/DAC) for quantum computing and test facilities for 4K operation.
- INFN: Circuits and architectures for time-based readout systems, TDCs and SiPM readout front-ends, SPI, LVDS transceivers and chip integration.
- RHUL/Oxford: ASIC characterisation of single-photon and timing response.

- Project 7.4a contact person: Manuel Rolo.

Available resources, existing funding and frameworks

The FZJ has an active R&D using a 22nm FDSOI technology and with participation of industrial partners. In addition, the group developed in the past optimised signal-processing circuits for operation at cryogenic temperatures. The FZJ infrastructure is ready for measurements down to 6 Kelvin, while a cryostat to measure at mK temperatures is currently in preparation. Currently, the core group that is working on cryogenic activities comprises 6 senior scientists and 5 doctoral researchers. A realistically minimum contribution to this research task would require funding for two doctoral researchers, however larger teams can be assembled depending on agreements within the working group.

The INFN and RHUL/Oxford groups collaborate on the development and production of CMOS ASICs for SiPM readout on dark matter cryogenic detectors, with a large team of scientists and engineers currently working on the construction of cryogenic photon sensors and integrated CMOS readout (designed at INFN) for the instrumentation of 6 m^2 of detector operating at LAr temperature. The INFN and RHUL/Oxford groups will provide access to infrastructures for tests at 77K and 1K/100mK, respectively. At INFN the involvement of several microelectronics experts and PhD students is foreseen, while the contribution of UK groups would involve both senior scientists and a solid group of PhD and post-doctoral researchers.

At KEK, other than expert ASIC designers, physicists and technical staff, the team expects to engage long-term budget assigned to this activity. Design experience on cryogenic chip design is also present at KEK, with the group having developed ASICs for dual-phase liquid-Ar TPCs with 180 nm CMOS. A new test setup for cryogenic electronics is in preparation.

Fermilab is leading several activities for the cryogenic characterisation of 22FDX transistors. In a collaboration with Synopsys and UTA, the laboratory is working on PDK-compatible BSIM-IMG for 4K and on measurement and modelling of high voltage devices at 4K.

EPFL, in collaboration with Fermilab, is conducting measurements of transistors at 4K and is developing simplified EKV models for analog design and low noise test structure measurements. These models will refer to a number of technologies, in primis, 22FDX.

In addition, Fermilab developed cryogenic CMOS models (84K), vendor based on test structures and data collected by FNAL, SMU and BNL groups. The list of IPs available include LVDS Tx and Rx, POR, Bandgap, level shifters, IO circuitry, which were integrated on system-ready chips (COLDATA, COLDADC) in collaboration with LBNL, BNL and SMU.

The groups from University of Sherbrooke, TU Graz and ICCUB will contribute to the design of SPAD arrays and to the design and characterisation of core IP blocks and demonstrator chips.

Table 20 shows the manpower and funding currently assured in participating institutes from the relevant funding framework for an initial three-year project duration. The values are given as averaged annual amounts.

Estimate of to be requested resources

Table 21 shows the manpower and funding foreseen to be requested by participating institutes from the relevant funding framework.

Table 20: Available resources and areas of contribution numbered as in Section B.4.1.

Institute	**Framework**	**Areas of Contribution**
TU Graz	tbd	WP2
U. Sherbrooke	tbd	WP2
FZJ	FZJ	WP1, WP2
INFN	Darkside-20K, DUNE	WP1, WP2
KEK	KEK-ITDC	WP2
ICCUB	LHCb, CTA	WP2
EPFL	DUNE	WP1
RHUL	Darkside-20K	WP1, WP2
U. Oxford	Darkside-20K	WP1, WP2
Fermilab	tbd	WP1, WP2
	FTE/yr	**Annual Funding** [EUR]
Total available	6.6/5.1/4.6/3.0	48k/50k/40k/20k

Table 21: Resources to be requested. One should consider that requests will be answered in the year following submission.

Institute	**Framework**	**Request submission year**
TU Graz	tbd	2024
U. Sherbrooke	tbd	tbd
FZJ	DFG	2024
INFN	INFN-CSN5, DUNE	2024
KEK	KEK-ITDC	2024
ICCUB	MCIN, EC	2024
EPFL	DUNE	2024
RHUL	Darkside-20K	2024
U. Oxford	Darkside-20K	2024
Fermilab	tbd	2024
	FTE/yr	**Annual Funding** [EUR]
Total to be requested	4.0/7.5/7.5/7.5	110k/191k/251k/140k

B.4.2 Project 7.4b: Radiation Resistance of Advanced CMOS Nodes

This project investigates the radiation response of CMOS technologies from the 28nm node onward for use in the next generations of ASICs for particle detectors.

Project Name	Radiation Resistance of Advanced CMOS Nodes (WG7.4b)
Project Description	This project aims to evaluate the radiation response (total ionizing dose TID, single event effects SEE, and displacement damage DD) of commercial CMOS technologies more advanced than the 65nm node for use in the next generations of ASICs for particle detectors. Duration 4-5 years.
Innovative/strategic vision	Understanding the effects of radiation on CMOS technologies is essential for the design of ASICs used in particle detectors. This project represents a first and crucial step in evaluating the performance of advanced CMOS nodes for the unique environment of particle detectors.
Performance Target	Deepen the knowledge of the radiation response of 40nm and 28nm technologies and begin to study finFETs technologies.
Milestones and Deliverables	Month 12: D7.4b.1 28nm CMOS front-end (FE) circuits for pixel sensors prototype; TID test of IP-blocks in 28nm node. **D7.4b.1** (M12) Deliver a 28nm CMOS front-end (FE) circuits for pixel sensors prototype; TID test of IP-blocks in 28nm node **D7.4b.2** (M18) Deliver a chip in 28nm CMOS including matrices of FE channels for readout of pixel sensors **M7.4b.3** (M24) Radiation test of FE structures; Design and testing of rad-hard memory elements in 28nm node **D7.4b.4** (M36) Deliver a prototype in FinFET technology including IP blocks for pixel readout circuits **D7.4b.5** (M42) Deliver a chip in FinFET technology including matrices of FE channels for readout of pixel sensors **M7.4b.6** (M48) Radiation qualification (report) of the FinFET readout channels.
Multi-disciplinary, cross-WG content	In order to ensure the success of projects involving ASIC design for particle detectors, it is imperative to consider the radiation resistance of the technologies used. On the other hand, the definition of radiation qualification would greatly benefit from the input of the designer. For example, ASICs developed in WP7.3a must be radiation tolerant and could also serve as valuable test vehicles to evaluate radiation effects.
Contributors	CERN AT: TU Graz IT: INFN Pavia, Uni. Bergamo, Uni. Padova, Uni. Pavia FR: CPPM
Available resources	3.2 FTE/yr 104k/yr
Addt'l resource need	2.4 FTE/yr 105k/yr

Project Description

CMOS technology has long served as the foundation for electronic devices used in both commercial and scientific applications. The performance of MOS transistors generally improves as feature size is reduced, leading to continuous efforts to miniaturize the technology and devices. The benefits of scaling have led CERN to move from the 250nm technology node used for the Application Specific Integrated Circuits (ASICs) installed in the particle detectors of the LHC, to the 130nm and 65nm

CMOS technologies used for the HL-LHC, and more recently to the 28nm technology for post-LS4 projects. Although scaling brings performance benefits, the sensitivity of CMOS technology to radiation effects does not necessarily improve with advanced nodes. As ASICs for future detector will continue to be based on CMOS technology, it is imperative to assess the radiation hardness of advanced nodes. The evaluation of the radiation sensitivity of a technology node may require multiple years and it is a multi-perspective process that benefits from a collaborative effort across several institutes.

1. prototyping test chips in 28nm CMOS technology,
2. radiation tests in 28nm CMOS technology,
3. prototyping test chips in FinFET technology,
4. radiation tests in FinFET technology,

Performance Target

The goal of the project is to evaluate the radiation response of advanced CMOS technologies, providing designers with the necessary information to be able to develop radiation-resistant ASICs. Thus, on the one hand the project is exploratory in nature, seeking to study each technology accessed, and on the other hand it has the practical purpose of providing information to designers regarding the technology already used. The project deliverables will therefore include the design of both simple and complex test chips to comprehensively evaluate the physical mechanisms that drive a given technology node's response to ionizing and non-ionizing cumulative effects (TID and DD), as well as sensitivity to SEE. The results of these tests will be shared with the community through detailed reports and journal articles.

Milestones and Deliverables

- **D7.4b.1** (M12) Deliver a prototype chip in 28nm CMOS including analog building blocks for the design of front-end circuits for pixel sensors.
- M7.4b.1 - (M12) Report on random telegraph noise density and TID evolution in 40nm bulk CMOS small devices will be prepared. (Although 40nm technology may not be the main focus of future studies, the methodology developed to measure and evaluate RTND on irradiated 40nm-node-device will serve as a model for chips and tests on more advanced technologies.)
- M7.4b.2 - (M12) Radiation tolerance qualification study of the IP-blocks in 28nm technology will be undertaken.
- **D7.4b.2** (M18) Deliver a small-area chip in 28nm CMOS including matrices of front-end channels for the readout of pixel sensors.
- D7.4b.3 - (M24) The design and test of radiation-hard memory elements in 28nm technology.
- **M7.4b.3** (M24) Radiation tolerance qualification of the submitted front-end structures.
- M7.4b.4 (M24) Report on a study of random telegraph noise density and TID evolution in the 28nm bulk CMOS small devices will be prepared.
- **D7.4b.4** (M36) Deliver a prototype chip in a FinFET technology including IP blocks for the design of pixel readout circuits.
- D7.4b.5 (M42) Delivery of a second small-area chip in a FinFET technology including matrices of front-end channels for the readout of pixel sensors.
- M7.4b.6 (M48) Radiation tolerance qualification (report) of the FinFET readout channels.

Multi-disciplinary, transversal content

An extensive examination of the radiation response of CMOS technologies demands a diverse range of skills, spanning designing of test chips, PCBs, and test systems. Other essential skills include formulation of qualification processes, as well as knowledge of particular measurement techniques, like noise measurements. The outcome of this research will be valuable for all detector systems being considered by the 2021 ECFA Detector R&D Roadmap. By its nature, WP7.4b is intertwined with several other WPs. For example, the ASICs developed in WP7.3a need to be radiation tolerant, but could also serve as valuable test vehicles to evaluate radiation effects. Another example is the radiation tolerant RISC-V processor and SoC platform targeted in WP7.2b, which could benefit from a comprehensive evaluation of the radiation response of advanced CMOS nodes.

Contributors and areas of competence

- **University of Bergamo / INFN Pavia / University Pavia**: The research group has a wide experience in the design of readout electronics for semiconductor detectors. The research interests are focused on low-noise, rad-hard analog front-ends as well as on mixed-signal multichannel readout systems. The research activities are also focused on the study of noise and radiation effects in electronic devices. Radiation hardness studies have been pursued in different nanoscale CMOS technologies.

- **University of Padova**: The Department of Information Engineering at the University of Padova has developed a significant expertise in the field of radiation effects on electronic components in the last twenty years. The RREACT (Reliability and Radiation Effects on Advanced Components and Technologies) group has been strongly involved in the characterization of the effects of the space, terrestrial and high-energy physics environments in electronic components. The devices studied in the framework of several Italian and European projects in collaboration with industrial and academic partners range from FinFETs and small circuits to full-size commercial non-volatile memories and complex microprocessors and FPGAs.

- **CERN EP-ESE-ME section**: has designed several test-chips for radiation effects and possesses a unique knowledge and expertise on TID, ultra-high-TID, and Single-Event effects in modern CMOS technologies (e.g., 250nm, 130nm, 65nm, 40nm 28nm, 22FDSOI). Access to two X-ray machines is also available.

- **CPPM, the Marseille Particle Physics Center** has been involved for several years in the development and construction of the ATLAS detector, a general-purpose particle physics experiment installed at the LHC. The CPPM ATLAS group is collaborating on the design, testing, and construction of the inner detector, the closest detector to the collision point. Since 2014, CPPM has been involved in the RD53 front-end chip design. In the framework of this collaboration, our group has been one of the main contributors to the testing and analysis of TID and SEE effects on the readout chip. The group has thus been able to consolidate its expertise in the effects of radiation on complex electronic devices and circuits.

- **Graz University of Technology**: The Institute of Electronics at TU Graz conducts research on robust ICs and systems, with focus on radiation tolerance, electromagnetic compatibility, aging and combined effects, where TID studies became a topic of research since 2015. Since then group has been involved in characterization of integrated devices and circuits under TID stress for medical, space and high energy physics applications, gaining know-how in dose rate calibration and experiment design.

- **Project 7.4b contact person:** Giulio Borghello.

Available resources, existing funding and frameworks

- The groups at University of Bergamo and Padova are involved in a 2-year project, started in October 2023 and funded by the Italian Ministry of University and Research for ∼190 kEuro,

focused on the design and radiation hardness qualification of analog front-end channels for pixel sensors in a 28 nm CMOS technology. Working stations with CAD tools for design and verification are available for the group, together with instrumentation for noise and static characterisation of devices.

- The "Technology survey and evaluation" work package of the CERN EP-ESE-ME section will span from 2024 to 2028, providing a total of 120 kCHF and 1.5 FTE/year. The ME section has also access to two x-ray machines and a probe-station setup suitable for long-term high-temperature annealing.Around 1.3 FTE/year are available for this activity.

- The group at TU Graz is leading a 4-years' research programme with funding covering 2 FTE granted by the Austrian Science Fund (FWF), of which 1 FTE, available until February 2025 is focusing on the activities dedicated to this project (DRD7.4b). Next to instruments for device and IC characterization, the Institute of Electronics has an X-ray irradiator for TID stress of ICs and workstations with CAD tools enabling in-house IC design and verification.

- As part of our institute's national scientific and technical outlook, CPPM is leading an R&T (Research and Technology) project focusing on the development of prototype circuits using the highly advanced technological processes required for the design of future generations of pixel-readout integrated circuits. This project is interested in the development of prototype detectors based on small hybrid pixels as well as monolithic DepMAPS sensors aimed primarily at very high hit rates and very high radiation levels. The project started in 2023 and is also interested in the tests and characterization aspect of advanced technologies with respect to radiation effects. As part of the overall R&T project, around 0.3 FTE/year is available, and a budget of 20 k€/year has been allocated to carry out this radiation work.

Table 22: Available resources and areas of contribution numbered as in Section B.4.2.

Institute	**Framework**	**Areas of Contribution**
Bergamo University / INFN Pavia / Pavia University	–	2, 3, 4, 5
Padova University	–	2, 3, 4, 5
CERN	EP R&D	2, 3, (4, 5)?
Aix Marseille Univ, CNRS/IN2P3, CPPM	–	2, 3
Graz University of Technology	–	1, 2, 3

Total available per year	**FTE/yr**	**Annual Funding** [EUR]
2024	4.1	124k
2025	3.4	169k
2026	2.0	20k
$\gg$ 2026	1.5	50k
Total available 2024-26	9.5	313k

Estimate of to be requested resources

- The groups at University of Bergamo, Pavia, and Padova plan to extend the study, to be carried out on the 28 nm technology, to more advanced CMOS nodes in the near future (from ∼M25 of the DRD7 project). In particular, they plan to investigate the design of front-end readout circuits based on FinFET technologies, exploiting the 16 nm (or beyond) process currently available through Europractice. Around 1 FTE/year is requested for this activity, together with a contribution close to 100 kEuro/year.

- The Institute of Electronics at TU Graz plans to extend the ongoing studies to further fundamental investigations of TID stress on advanced CMOS nodes, with the focus on TID

dose rate and temperature dependence. The resources requested for DRD7.4b will amount 200kEUR, covering 1 FTE as well as material budget of 15kEUR/year. Envisaged time frame: 4 years (DRD project M12 to M56).

- CPPM: This kind of radiation test requires a huge amount of preparation in terms of the test set-up, as well as financial resources for missions and access to certain facilities. On the basis of our ambitious project which should lead to the development of a high-radiation hard pixel readout chip prototype, it would be advisable to operate with 1 FTE/year and a budget of 50 k€/year.

Table 23: Resources to be requested. One should consider that requests will be answered in the year following submission.

Institute	**Framework**	**Request submission year**
Bergamo University / INFN Pavia / Pavia University	–	2023
Padova University	–	2023
CERN	EP R&D	2023
Aix Marseille Univ, CNRS/IN2P3, CPPM	–	2023
Graz University of Technology	–	2023
	FTE/yr	**Annual Funding** [EUR]
2024	2.0	45k
2025	2.0	65k
2026	3.3	205k
$\gg$ 2026	3.3	205k
Total to be requested 2024-26	7.3	315k

B.4.3 Project 7.4c: Cooling and cooling plates

This project focuses on the development of the next generation of cooling plates for front-end electronics and sensors based on different materials/techniques. The main goal is to explore manufacturing techniques while improving electronics integration with a cost-effective solution. This project groups different topics covered by different collaborations which will be presented in the coming sections.

Note that depending on the evolution of the forming DRD8 Collaboration, some cooling-related projects may be best integrated in DRD8. This will be fine tuned in due-time to best match the needs of the projects.

Project Name	Cooling and cooling plates (WG7.4c)
Project Description	Development of the general purpose next generation of microchannels cooling structures to deliver excellent cooling performance, minimal material budget, and better electronics integration. Duration about 2+ years.
Innovative/strategic vision	Better integration of electronics features to the cooling plates especially in dense electronics applications. Better scalability considering alternative manufacturing techniques (more cost-effective). Thermal performance numerical simulation tools for new applications.
Performance Target	Different topics will explore different combinations of the following parameters: power dissipation (up to 2W/cm^2), material budget ($\leq 0.5\%X_0$), integration and/or cost. Different experiments will be able to profit from the portfolio created and optimize those solutions for their final application. The progress will be tracked via public reports in the form of presentations, public notes and/or papers.
Milestones and Deliverables	**D7.4c.3** (M15) Deliver a feasibility public note or paper (topic 3) **M7.4c.6** (M24) 3D printing public note or paper (topic 4) **D7.4c.5** (M27) Deliver a report summarising fluidic and thermal tests of demonstrators public note or pape5 (topic 1) **M7.4c.7** (M36) Bi-phase CO2 Thermo-fluidic models developed for microchannel, nuclear and annular flows, and thermal heat exchanger characterization and interconnection (topic 2).
Multi-disciplinary, cross-WG content	Communication with DRD8 (Mechanics) and DRD3 (Semiconductor detectors) via liaisons and workshops (e. g.: Forum on tracking mechanics) and 7.6b project (common access 3D and advanced integration) within the DRD7.
Contributors	CA: Sherbrooke CERN DE: DESY ES: IMB-CNM, IFIC-Valencia UK: Manchester FR: CPPM, LAPP, LEGI, LPNHE, LPSC
Available resources	7.7 FTE/yr (First year), 102k/yr (First year)
Addt'l resource need	7.0/yr (Largest, on 2026), 275k/yr (Largest, on 2026)

Project Description

Micro-channel cooling plates are extremely efficient in removing the heat from the front-end electronics and/or sensors since the coolant is very close to the heat source. This project aims to improve its integration and cost, and also explore alternative base materials while minimizing its material budget, increasing its ability to dissipate more power and integrating more electronics fea-

tures. The optimization of those aspects is extremely application-dependent. The topics covered by different collaborations are presented below:

- *Silicon microchannels via buried channels (T1)* → this topic has two work lines: On one hand, the development of "active interposers" which hold the mechanical support and the embedded micro-channels to provide the local, high-efficient cooling, together with a re-distribution metal layer (RDL) that can provide the interconnection of the assembly of detector plus front-end electronics with the back-end electronics and the rest of the system. On the other hand, the work to obtain a microchannel technology fully compatible with the (CMOS) sensors in the same substrate.

- *Silicon microchannels via thermo-compression (T2)* this topic covers several developments carried by a collaboration of French laboratories: 1) the setting up of a dedicated cooling test bench; 2) the fabrication of cooling plates with micro-channels of various geometrical and surface form factors; 3) the development of numerical 3D models - based on dedicated measurements - and their implementation in numerical simulation tools to optimize the micro-channel heat exchanger design; 4) the development a low-cost silicon cooling-plates fabrication process, mainly based on an innovative bonding technique: "the hyperbaric bonding", which uses thin layer of gold - similarly to the thermo-compression - and is performed at room temperature inside an hyperbaric chamber; 5) the developments of cooling-plates interconnects to allow the fabrication of heat exchangers covering large areas.

- *Ceramics substrate (T3)* → This topic covers the investigation of ceramics cooling plates with embedded microchannels and additional electronic features. Low-temperature cofiring ceramic (LTCC) and high-temperature cofiring ceramic (HTCC) combine different ceramic layers to enclose the channels and it offers the possibility to integrate high conductivity materials in between those layers as well. Lines inside the cooling plate can be accessed via vias. The benchmark model for the characterization of those structures will be the LHCb VELO Upgrade 2 which has very challenging requirements (high power density, high pressure, and in vacuum operation).

- *3D printing (T4)* → The ability to print cooling/mechanical structures brings a higher level of design flexibility, fast turn-around processing time, and cost-effectiveness, especially in electronics-dense areas with limited space. In this scenario, titanium 3D printing via selective laser sintering will be explored in this topic. The surface finishing and potential of the material budget will be improved by exploring in addition post-processing techniques. This topic will also follow the requirements for the LHCb VELO Upgrade 2 (CO_2) as a benchmark but a similar approach can also be used for different applications.

During the DRD7 implementation, only projects involving microchannels-based designs have been proposed by different research groups. Therefore, different topics covering this strategy were collected in this single project. New ideas will continue to be welcome and either incorporated into this project or a new one depending on its technology. New calls for ideas will be made in the DRD7 workshops.

Performance Target

The overall goal of this project is to design, manufacture, and validate the next generation of microchannels cooling plates based on different materials (Si, ceramics or metal). For the ceramics approach, the main deliverable is the feasibility study of this technique. On the other hand, for the other topics, the main target is a demonstrator by the end of the project followed by a report (public note or paper). The different techniques will be optimized with different combinations of targets based on the power dissipation (up to 2W/cm^2, LHCb VELO Upgrade 2 as a benchmark), material budget ($\lesssim 0.5\%X_0$), better electronics integration and/or cost. The balance of those parameters is extremely dependent on the application. In this sense, some applications are foreseen to have more demanding requirements in the material budget (down to $\lesssim$0.2 $\%X_0$), together with less demanding requirements in power dissipation ($\sim$10-100 mW/cm^2). Therefore, this general R&D proposal will create a portfolio of potential solutions that can be optimized to the final specific application requirements.

Milestones and Deliverables

Topic		Month	Description
T1	D7.4c.1	6	Demonstrate the 3D integration of cooling interposers with RDL
T4	D7.4c.2	9	3D printing prototypes with post-processing manufacturing
T3	M7.4c.1	10	Ceramics validation (Leak tightness, High pressure and flow tests)
T2	M7.4c.2	12	Bi-phase CO2 Thermo-fluidic models development for microchannels/ Slug flow with heat mass transfer
T3	M7.4c.3	12	Ceramics cooling tests (Demonstrator)
T1	D7.4c.4	15	Demonstrate the integration of microchannels in a CMOS process
T3	**D7.4c.3**	15	Ceramics feasibility tests public note or paper
T2	M7.4c.4	18	Prototypes bonded with thermo-compression or hyperbaric process characterization
T4	M7.4c.5	18	3D printing prototypes testing and validation (high pressure, flow, cooling, x-ray tomography)
T4	**M7.4c.6**	24	3D printing public note or paper
T1	**D7.4c.5**	27	Fluidic and thermal tests of demonstrators public note or paper
T2	**M7.4c.7**	36	Bi-phase CO_2 Thermo-fluidic models development for microchannels/ nuclear and annular flows. Heat exchangers characterization and interconnections

Note: Deliverables and milestones shown in the summary tables are listed in **bold**

Multi-disciplinary, transversal content

Designing, manufacturing, and validating the next generation of cooling plates are critical to dense front-ends, at the interface between electronics, sensors, mechanics, and integration. There is a clear overlap with DRD8 and DRD3 which will be covered by communications via the respective *liasons* and workshops (e.g.: Forum on tracking mechanics). The synergy with the 7.6b project (common access 3D and advanced integration) will be done within the DRD7.

Contributors and areas of competence

- **University of Manchester**: Experience in the assembly, testing, and quality control of silicon detectors in general and micro-channel cooling plates with CO_2 evaporative cooling. Recently, played a major role in the LHCb VELO Upgrade 1 module assembly.
- **IMB-CNM**: Technology development, 3D integration, electronic testing.
- **IFIC**: Full system integration, cooling interconnection, mechanics, services.
- **DESY**: Fluidic and thermal tests, system development.
- **CPPM**: Experience in the assembly, testing, and validation of silicon detectors in general (ATLAS) and in the development of micro-channel cooling plates (NA62 GigaTracKer). Recently, the development of bonding processes at room temperature in collaboration with the micro-fabrication CNRS laboratory FEMTO-ST.

- **LAPP**: Experience in CO2 microchannels heat exchanger studies, thermal and mechanical simulations, characterization and measurement on bi-phase CO2 cooling test bench.
- **LEGI**: Experience in numerical modeling to simulate the flow of bi-phase coolant inside micro-channels. Microchannel heat exchanger production (etching, anodic silicon/Pyrex bonding and connectors brazing)
- **LPNHE**: Experience in assembly, construction and characterization of silicon pixel modules, design of micro-channel cooling plates and interconnections.
- **LPSC**: Experience in CO2 microchannels heat exchanger studies, thermal and mechanical simulations, characterization and measurement on bi-phase CO2 cooling test bench.
- **Project 7.4c contact person:** Oscar Augusto De Aguiar Francisco.

Available resources, existing funding and frameworks

Table 24 shows the manpower and funding currently assured in participating institutes from the relevant funding framework for an initial three-year project duration. The values are given as averaged annual amounts.

Table 24: Available resources and areas of contribution numbered as in Section B.4.3.

Institute	**Framework**	**Areas of Contribution**
University of Manchester	LHCb VELO Upgrade 2 (UK-STFC)	Microchannel cooling plates and Silicon detectors
IMB-CNM	AIDAInnova EU National Funding	Technology development, 3D integration, electronic testing
IFIC	AIDAInnova EU National Funding	Full system integration, cooling interconnection, mechanics, services
DESY	National Funding	Fluidic and thermal tests, system development
CPPM, LAPP, LEGI, LPNHE, LPSC	In2p3 R&T "Micro-canaux"	Microchannel cooling plates low cost fabrication process, thermo-fluidic simulation tools, optimisation of microchannel designs, 3D printing ceramic and low temperature (down to -45°C) characterisation.
	FTE/yr	**Annual Funding** [EUR]
Total available	7.7 (2024)	102k (Maximum in 2024)

Estimate of to be requested resources

Table 25 shows the manpower and funding foreseen to be requested by participating institutes. The table indicates the current framework (project name/funding agency) which provides (the current) partial funds to cover the topics. To be able to achieve the milestones/deliverables more funds will be required. Hence, the endorsement from the DRD7 will help to enable those initiatives in the medium/long-term.

Table 25: Resources to be requested. One should consider that requests will be answered in the year following submission.

Institute	**Framework**	**Request submission year**
The University of Manchester	TBC	2024
IMB-CNM	TBC	2024
IFIC	TBC	2024
DESY	TBC	TBC
CPPM, LAPP, LEGI, LPNHE, LPSC	TBC	TBC
	FTE/yr	**Annual Funding** [kEUR]
To be requested	7.0 (Maximum, in 2026)	275.0 + TBC (Maximum, in 2026)

B.5 Work Package 7.5: Backend systems and commercial-off-the-shelf components

B.5.1 Project 7.5a: DAQOverflow

The DAQOverflow project aims to provide a benchmark of heterogeneous COTS architectures alongside a open-access, repository-hosted infrastructure and set of commonly used tools and algorithms that will keep pace with evolving COTS technologies (GPU, CPU and FPGA coprocessor farms) for the purpose of cost- and performance considered near-detector, near-real-time backend processing for HEP experiments.

Project Name	DAQOverflow (WG7.5a)
Project Description	Benchmarking of heterogeneous COTS architectures and development of TDAQ tools and algorithms distributed via a common repository that are up-to-date with evolving COTS technologies for cost- and performance-considered near-detector/real-time backend processing.
Innovative/strategic vision	Identify experiment-agnostic common TDAQ activities, define generic benchmarks to allow easy comparison of cost/energy efficiency for various compute architectures for the purposes of backend/trigger processing. Make generic algorithms / tools available for various architectures as a repository of 'best practice'.
Performance Target	Cost- and performance-evaluated figures of merit (cost/energy per unit of work), mutil-disciplinary deliverables (kept up-to-date for newer generations of hardware) and distributed reference implementations and examples through a documented common repository of firmware and software. The target after three years is a community-driven, growing project of development with appropriate funding mechanism from the work package and interested users to re-benchmark for new hardwares/technologies when needed.
Milestones and Deliverables	**D7.5a.1** (M9) Delivery of first reference implementations of workflows on simpler platforms **D7.5a.2** (M12) Delivery of a repository and documentation with format agreed upon, reference implementations hosted **D7.5a.3** (M24) Delivery of reference implementations of workflows for a full suite of ASIC/CPU/GPU delivered **D7.5a.4** (M30) Delivery of the benchmarking for full suite, documented and published **D7.5a.5** (M33) Delivery of any followup benchmarks using improved algorithms on existing hardware and first benchmarks on next-gen hardware **D7.5a.6** (M36) Delivery of any comparative performance studies between previous and current generation hardware published.
Multi-disciplinary, cross-WG content	Commodity TDAQ hardware is cross-experiment in nature. The outcomes will be transverse to much of the DRD program for specific DAQ considerations.
Contributors	Instituto de Física Corpuscular (IFIC) Valencia, University College London, University of Birmingham, University of Bristol, Rutherford Appleton Laboratory, University of Geneva, Universidad de Oviedo, University of Manchester
Available resources	$\sim$ 6.5 FTE/yr, $\sim$ 30kEUR/yr
Addt'l resource need	$\sim$ 2.5 FTE/yr, $\sim$ 125kEUR/yr

Project Description

Backend processing for HEP experiments has traditionally been the realm of limited localised workflows on FPGAs or dedicated ASICs. In recent years the power and complexity of ASIC devices has increased substantially, and at the same time typically offline workloads have moved closer to the detector using online, near-real-time COTS compute resources (GPU, CPU and FPGA coprocessor farms). The DAQOverflow project aims to keep pace with these COTS technologies as they evolve by benchmarking common TDAQ workflows on a variety of architectures, providing a resource which allows future experiments to pick and choose based on cost- and performance considerations using reference implementations of these workflows.

Performance Target

The project aims to determine a open-access, repository-hosted infrastructure and set of commonly used and generally applicable TDAQ workflows for near-detector, near-real-time backend processing for HEP experiments. It will provide reference implementations for these on a variety of existing architectures (GPU, CPU and FPGA coprocessor farms) that are evaluated for both cost and performance , and will benchmark these using defined metrics. The deliverables will be architecture optimised, benchmark implementations that will continue to grow over time. The targeted outcomes should be multi-disciplinary in their inception and realisation, with dedicated and committed resources across the WG keeping the deliverables updated in the repository as newer generations of hardware become available. The resulting products will be freely available to the wider community through a webpage, and can be updated by submitting new implementations subject to project-internal review. The goal after three years is to have transitioned into the developed infrastructure being widely shared via the common repository and therefore largely community-driven. An appropriate funding mechanism from the work package and interested users will need to be established to re-benchmark with new hardwares and technologies when needed.

Milestones and Deliverables

Separated into years:

Deliverable*	Target Date	Description
M7.5a.1	(M3)	Determine a set of specific workflows to test
M7.5a.2	(M3)	Agree on initial hardware platforms and arrange access
M7.5a.3	(M6)	Benchmark criteria, figures of merit agreed on a per-architecture basis
D7.5a.1	(M9)	Delivery of first reference implementations of workflows on simpler platforms (CPU/HLS)
D7.5a.2	(M12)	Delivery of a repository and documentation format agreed upon, reference implementations hosted
D7.5a.3	(M24)	Delivery of reference implementations of workflows for a full suite of ASIC/CPU/GPU delivered
D7.5a.4	(M30)	Delivery of the benchmarking for a full suite documented and published
D7.5a.5	(M33)	Delivery of and followup benchmarks using improved algorithms on existing hardware and first benchmarks on next-gen hardware
D7.5a.6	(M36)	Delivery of any comparative performance studies between previous and current generation hardware published

*Note: Deliverables or milestones shown in the summary tables are listed in **bold**

Multi-disciplinary, transversal content

The purpose of DAQOverflow is to benchmark common TDAQ workflows on COTS hardware. As commodity hardware is cross-experiment in nature, there is a natural transversal component to the work: Initial workflows will be determined based on what tasks common to existing projects, and with a view towards what tasks may be commonplace in future TDAQ environments. Close coupling with R&D activities in the other DRD themes is natural since testbed / beamline activities will need TDAQ infrastructure. Off-the-shelf software and firmware options benchmarked by cost/performance will be beneficial for these themes as it will reduce development time on 'infrastructure' in favor of their specific goals. In general, the other DRD themes will have direct access to the common repository code which they can use to inform the DAQ software relevant to their project, and that they can contribute back to with specific implementations customised to their use cases. A DRD7.5a point-of-contact or contributor would be able to recommend the fastest and most optimum solution in the repository for them to access and begin a new implementation that could be developed on e.g. a new branch of the repository and potentially merged if fully developed and of more general HEP use. In this way, the project is intended to become somewhat self-perpetuating, with users contributing directly to the managed project during, and beyond the initial three year period. This is particularly important as future generations of COTS architectures become available. The repository will maintain a history of the performance and design evolution of common DAQ workflows over future generations of hardware.

Contributors and areas of competence

- **IFIC Valencia:** Real time GPU tracking algorithms for LHCb. Fast NN implementation on GPUs. Real time signal reconstruction in DSPs and FPGAs. ML algorithms for peak detection and energy reconstruction on FPGAs for ATLAS.
- **University of Oviedo:** Real time tracking algorithms for muon reconstruction for the CMS software (HLT) and hardware (L1) trigger on FPGAs.
- **CIEMAT:** Muon Trigger at CMS (BMTL1), real time algorithms on FPGAs and Data acquisition in CMS.
- **Rutherford Appleton Laboratory:** ATLAS L1 Trigger (eFex & Global). Xilinx + GPU development, benchmarking and tools.
- **University of Manchester:** Real-time trigger leadership (LHCb), Muon g-2, Mu2e and MuEDM, FPGA development for O(ns) real-time processing, ATLAS, DUNE, event filtering & tracking. Benchmarking of clustering on FPGA, CPU + GPU.
- **University of Bristol:** CMS L1 trigger development, DUNE DAQ, Trigger algorithm development (Firmware, Software + GPU). Low latency Machine Learning in firmware.
- **University of Geneva:** Real-time hadronic jet finding (also using ML) for ATLAS (HL-LHC) triggers on heterogeneous (FPGA coprocessor) event filter farms and low-latency algorithms for ATLAS and FASER
- **University of Birmingham:** Atlas L1 trigger (eFex and Global). DUNE DAQ CCM group.
- **University College London:** Data Acquisition in ATLAS (SCT, ITk & global), g-2, mu2/3e, PUEO and DUNE experiments. Tracking, Trigger and Machine Learning algorithms using GPU, FPGA.
- **Queen Mary University of London:** ATLAS, DUNE, Belle II, generic Detector Development, Online software (control, databases, monitoring, hardware testing, GUIs), trigger simulation, trigger performance, Raspberry Pi-based systems, GPU, machine learning on FPGA.

Project Contact: Alex Keshavarzi (alexander.keshavarzi@manchester.ac.uk), University of Manchester.

Table 26: Available resources.

Institute	**Framework**	
Instituto de Física Corpuscular (IFIC) Valencia	COMCHA	
Universidad de Oviedo	COMCHA	
CIEMAT	COMCHA	
Rutherford Appleton Laboratory	UK R&D	
University of Manchester	UK R&D / Royal Society	
University of Bristol	UK R&D	
University of Birmingham	UK R&D	
University College London	UK R&D	
Queen Mary University of London	UK R&D	
University of Geneva	SNF	
	FTE/yr	**Annual Funding** [EUR]
Total available	6.5	33k

Estimate of to be requested resources

Table 27 shows the person-power and funding foreseen to be requested by participating institutes from the relevant funding framework. Not all aspirations are available at this time.

Table 27: Resources to be requested. One should consider that requests will be answered in the year following submission.

Institute	**Framework**	**Request submission year**
Instituto de Física Corpuscular (IFIC) Valencia	COMCHA	2024
Universidad de Oviedo	COMCHA	2024
Rutherford Appleton Laboratory	UK R&D	2024
University of Manchester	UK R&D	2024
University of Bristol	UK R&D	2024
University of Birmingham	UK R&D	2024
University College London	UK R&D	2024
Queen Mary University of London	UK R&D	2024
University of Geneva	SNF	2024
	FTE/yr	**Annual Funding** [EUR]
Total to be requested	2.5	123k

B.5.2 Project 7.5b: From Front-End to Back-End with 100GbE

The perspective of future HEP experiments with lower radiation levels than typically seen at LHC opens the door to increasing the complexity of Front-End electronics, implementing for example RISC-V based processors and SoC in the Front-End. In this context, high throughput 100GbE-based data readout link can reasonably be envisaged. This is a new paradigm which will be investigated in this DRD7.5 Project. It will be tightly linked to other Working Groups like DRD7.2/RISC-V or DRD7.1/links activities.

Project Name	From Front-End to Back-End with 100GbE (WG7.5b)
Project Description	Develop full 100Gb Ethernet-based solutions for Data Readout links from Front-End to DAQ.
Innovative/strategic vision	Lower radiation levels and higher data throughput in future detectors open the door to envisage and investigate 100GbE-based data readout links.
Performance Target	Design and performance comparison between network demonstrators of 100GbE networks based on specific protocol designs, configurations of COTS and potentially customized switches.
Milestones and Deliverables	**M7.5b.1** (M12) Delivery of a report on generic implementation of standard 100GbE on current custom Back-End boards **D7.5b.1** (M12) Delivery of a demonstrator of a FEC-based asymmetric 100GbE link with lpGBT **M7.5b.2** (M18) Specifications for a Macrocell for potential future 100GbEFront-End ASICs **D7.5b.2** (M18) Delivery of smart switch specifications (document) and prototype, including a paper submission and a gitlab repository - Theme 2 **D7.5b.3** (M24) Delivery of demonstrators of a full 100GbE system **D7.5b.4** (M24) Delivery of first prototype test ASIC including protocol IPs and test report. **M7.5b.3** (M36) Full report with conclusion on feasibility of 100GbE-based readout links for Front-End of future detectors **D7.5b.5** (M36) Second prototype test ASIC including Protocol IPs and test report - Theme 4 **M7.5b.6** (M60) If relevant: demonstrator of a 100GbE network combining existing and future Front-End ASICs.
Multi-disciplinary, cross-WG content	Universal across HEP for detectors requiring high/concentrated data readout bandwidth. Tightly linked to other WG like DRD7.2/RISC-V or DRD7.1/links activities
Contributors	CERN FR: CPPM CNRS/IN2P3 NL: Nikhef UK: Bristol University,[1] Imperial College, Rutherford Lab US: Brookhaven National Lab[1]
Available resources	9.7 FTE over 3 years 70k over 3 years
Addt'l resource need	14 FTE over 3 years 185k over 3 years

[1] The participation of this institute in the project depends on the success of the request for funds made at the end of 2023.

Project Description

Streaming data directly from HEP detector Front-End to the DAQ processing farm over Ethernet is very attractive for readout systems of future detectors. Several approaches could be envisaged to reach such a goal: using COTS switches to handle data-streams from the Front-End to Network Interface Cards (NICs) or even DAQ processors (the "No backend" approach), or to design a COTS-based high-density switch bridging the detector environment to the COTS/DAQ world (the "Smart Switch" approach). These approaches are complemented with Back-End board adaptation to explore DAQ topologies with 100GbE (based on the PCIe400 & FELIX for DAQ, concentration and processing) and with the study and design of the building blocks IPs necessary for 100Gb Ethernet cores implementation in future FE ASICs.

These various topics are to be addressed by different collaborators according to their respective expertise.

To address this objective, two main (and complementary) approaches will be investigated in parallel:

- **the "No backend" approach - *Theme 1***: using 100GbE COTS switches to handle data-streams from the Front-End to Network Interface Cards (NICs) or even DAQ processors (CERN LBC and ESE groups).
- **the "Smart Switch" approach - *Theme 2***: design of a COTS-based high-density switch bridging the detector environment to the COTS/DAQ world (Imperial College).

Their Back-End and Front-End counterparts will be organised as follows:

- **Back-End boards adaptation - *Theme 3***: to explore DAQ topologies (based on custom boards for DAQ, concentration and processing) (CPPM CNRS/IN2P3, Nikhef, Brookhaven National Lab (if resource requests are granted in 2024)).
- **Front-End ASICs - *Theme 4***: study and design of the building blocks IPs necessary for 100Gb Ethernet cores implementation in future FE ASICs. (Rutherford Lab (if resource requests are granted in 2024)).

Performance Target

The objective of this project is to study the feasibility and to build network demonstrators of a 100GbE readout network mostly based on COTs (at least for the off-detector part) but tailored to fit the expected needs of future experiments. This system shall therefore combine the best of both worlds. In the one hand, it must allow:

- asymmetric bandwidth,
- potentially machine-synchronous line rate (to be clarified over phase I of the project)
- no or reduced auto-negotiation protocol
- strong or custom Forward Error Correction schemes to target a link error rate below 10^{-12}

In the other hand it should provide:

- large data throughput,
- commercial components for the switches and the Network Interface Cards (NICs)
- full reconfigurability and scalability

Each of the points listed above is a challenge in itself and must be studied and tackled. Some trade-offs may be proposed (like custom backend boards or smart switches for example) to overcome difficulties. Several proofs of concept shall be built (one targeting the "No Backend" approach and another one based on the "Smart Switch" approach) and compared to demonstrate the feasibility of 100GbE for frontend, and to highlight the main strengths and weaknesses of each architecture

choice.
At the end of the first phase of the project, the comparison will have been made and feasibility established. If feasibility is proven, the protocol will have been defined and the first IPs drawn up for a future ASIC capable of formatting data according to this protocol.
Phase II of the project, if validated, will focus on prototyping ASICs, consolidating the Data Acquisition (DAQ) part of the network, and establishing the demonstrator of a complete network also incorporating the protocol ASIC, coupled with the transceiver proposed by Working Group DRD7.1.

Milestones and Deliverables

- **M7.5b.1** (M12) Report on generic implementation of standard 100GbE on current custom Back-End boards - Theme 3
- **D7.5b.1** (M12) Delivery of emonstrator of a FEC-based asymmetric 100GbE link with lpGBT as Front-End End-nodes and 4x10Gbps to 1x100GbE protocol conversion, available for experimentation in the CERN ESE timing lab (including a paper submission and a gitlab repository - Theme 1.
- **M7.5b.2** (M18) Specifications for a Macrocell for potential future 100GbEFront-End ASICs (Technical document) - Themes 1 and 4
- **D7.5b.2** (M18) Delivery of smart switch specifications (document) and prototype, including a paper submission and a gitlab repository - Theme 2
- **D7.5b.3** (M24) Delivery of demonstrators of a full 100GbE system with current and emulated Front-End ASICs, COTS and smart switches, commercial NICs and custom Back-End boards, and custom Software (including a paper submission and a gitlab repository) - Themes 1, 2, 3
- **D7.5b.4** (M24) First prototype test ASIC including protocol IPs and test report - Theme 4
- **D7.5b.5** (M36) Delivery of second prototype test ASIC including Protocol IPs and test report - Theme 4
- **M7.5b.3** (M36) Full report with conclusion on feasibility of 100GbE-based readout links for Front-End of future detectors (PhD Thesis Report) - Themes 1, 2, 3, 4
- D7.5b.6 (M60) If relevant and on the second stage of the project >2026: demonstrator of a 100GbE network combining existing and future Front-End ASICs - Themes 1, 2, 3, 4

Multi-disciplinary, transversal content

This project is universal across HEP for detectors requiring high/concentrated data readout bandwidth. It will be tightly linked to other DRD7 Working Groups like DRD7.2/RISC-V or DRD7.1/links activities

Contributors and areas of competence

- **Bristol University**[1]: has worked on the DUNE readout using 100GbE and COTS NICs.
- **Brookhaven National Lab**[1]: has designed the FELIX Back-End board used by ATLAS, sPHENIX and ProtoDUNE-I. Is currently designing the upgraded version of FELIX based on Versal Prime FPGA and Versal Premium FPGA. Expert in PCB design.
- **CERN-ESE**: has designed several backend boards for ATLAS (CTP, LTI, MuCTPI), CMS (FC7) as well as generic Back-End boards (GLIB). Is currently investigating and implementing a first proof of concept of a 100GbE-based data readout link using open source COTS switches and FPGA evaluation kits.

[1]The participation of this institute in the project depends on the success of the request for funds made at the end of 2023.

- **CERN-LBC**: has designed LHCb's DAQ network. Expert in networks in general.
- **CPPM CNRS/IN2P3**: has designed the PCIe40 Backend board used by LHCb and ALICE. Is currently designing the PCIe400 prototype. Expert in PCB and firmware design.
- **Imperial College**: has designed MicroTCA cards, such as the MP7 and FC7, the latter in conjunction with CERN. Contributed to the Serenity ATCA board for CMS. Expert in PCB and Firmware design.
- **Nikhef**: has designed the firmware of the FELIX board. Expert in firmware development.
- **Rutherford Laboratory (Technology)**: The ASIC design group has designed several ASICs for experiments at CERN and has recently developed IP for high-data-rate applications. The group has developed serialiser IP based on the Aurora 64/66 bit protocol with speeds up to 14Gbps NRZ and 28Gbps PAM4 using the 65nm TSMC process. The group plans to study and design the building blocks necessary for implementing Ethernet up to 100Gb on front end ASICs.

The project will be managed on a rotational basis, with one year's deputy project manager becoming the project manager the following year. For 2024:

- **Project Leader**: Sophie Baron
- **Deputy**: Antonio Pellegrino (Nikhef)

Available resources, existing funding and frameworks

Table 28 shows the manpower and funding currently assured in participating institutes from the relevant funding framework for an initial three-year project duration. The values are given as averaged annual amounts.

Table 28: Available resources and areas of contribution numbered as in Section B.5.2.

Institute	**Framework**	**Areas of Contribution**
CPPM CNRS/IN2P3	FR IN2P3 Funding	Theme 3
Bristol University	UK R&D[1]	Theme 1
Brookhaven National Lab[1]	US DOE	Theme 3
CERN	CERN EP R&D	Theme 1
Imperial College	UK R&D	Theme 2
Nikhef	NL R&D	Theme 3
Rutherford Laboratory[2]	UK R&D	Theme 4
	FTE/yr	**Annual Funding** [EUR]
Available 2024	3.9	37.5k
Available 2025	3.4	32.5k
Available 2026	2.4	0k
Available >2026	1	0k
Total available (2024-2026)	9.7	70k

[1] The participation of this institute in the Themes indicated depends on the success of the request for funds made at the end of 2023.

[2] Theme 4 is the responsibility of Rutherford Laboratory alone. In the event that the request for funds made by this institute is not fully granted, theme 4 will be maintained but at a slower pace.

Estimate of to be requested resources

Table 29 shows the manpower and funding foreseen to be requested by participating institutes from the relevant funding framework. Not all aspirations are available at this time.

Table 29: Resources to be requested. One should consider that requests will be answered in the year following submission.

Institute	**Framework**	**Request submission year**
CPPM CNRS/IN2P3	FR IN2P3 Funding	2024
Bristol University	UK R&D	2023
Brookhaven National Lab	US DOE	2023
CERN	CERN EP R&D	2026[3]
Imperial College	UK R&D	2023
Nikhef	NL R&D	2024
Rutherford Laboratory	UK R&D	2023
	FTE/yr	**Annual Funding** [EUR]
To be requested 2024	3.5	10k
To be requested 2025	5	95k
To be requested 2026	5.5	80k
To be requested >2026	7.5	80k
Total To be requested (2024-2026)	14	185k

[3] Such a resource request will be issued only if the feasibility of 100GbE for Front End readout links is proven by the phase I of the project.

B.6 Work Package 7.6: Complex imaging ASICs and technologies

B.6.1 Project 7.6a: Common Access to Selected Imaging Technologies

This project aims to provide common access to advanced imaging technologies through the organization of common fabrication runs. These are initially envisaged for the TowerJazz 180 nm, TPSCo 65 nm ISC, and the LFoundry 110 nm CMOS imaging technologies. These will be accessible for different clients in the community, among which the other DRDs like DRD3, experiments and projects in HEP. Assembly of the reticle for the different runs is foreseen, as well as design support for the PDK, development of special design rules, TCAD support for sensor optimization and interfacing to the foundry. IP development is also foreseen to accelerate and streamline the design effort. Continuation of this common access beyond the initial three years is expected. Synergy with the 7.6b 3D development will be explored possibly with already existing chips or chiplets. Full 3D-stacked runs, offered in all three technologies, may possibly be pursued later.

Table 30: Summary of project 7.6a.

Project Name	Common Access to Selected Imaging Technologies (WG7.6a)
Project Description	Provide common access and centralized support for selected CMOS imaging technologies, including specific IP development to accelerate the design effort. Duration 3 years, expected to be extended.
Innovative/strategic vision	Potential of monolithic technologies, confirmed by successful ALICE ITS2 tracker and the widespread community interest. Efficient and affordable technology access requires concentration of the resources in the community.
Performance Target	Organize common runs and efficient and cost-effective access to selected technologies.
Milestones and Deliverables	***TPSCo 65 nm ISC:*** **M7.6a.1a** (M12) Completion of IP specifications **M7.6a.2a** (M18) First version of IP complete **D7.6a.1a** (M24) Delivery of a report summarising foundry submission Q4 2025 **M7.6a.3a** (M36) Documentation of IP for common use ***TJ 180 nm (submissions subject to demand):*** **M7.6a.1b** (M12) Completion of IP specifications **M7.6a.2b** (M18) First version of IP complete **D7.6a.1b** (M24) Delivery of a report summarising foundry submission Q4 2025 **M7.6a.3b** (M36) Documentation of IP for common use ***LF110 nm:*** **D7.6a.1c** (M24) Delivery of a report summarising foundry submission Q4 2025 **D7.6a.2c** (M36) Delivery of a report summarising foundry submission Q2 2026
Multi-disciplinary, cross-WG content	Concerns several detectors types, calorimeters, tracking, etc. Serves other DRDs like DRD3 and DRD6, experiments and projects in HEP. Strong connection with 7.6b (e.g. 3D integration of chiplets). Requires expertise in analog and digital IC design, device design and technology, and significant testing effort.
Contributors	CH: CERN FR: IN2P3: CPPM, IPHC, IP2I + others IT: INFN(TO, TIFPA, MI, BO, PD, PV, PG, PI) NL: NIKHEF NO: UiB, UiO and USN UK: STFC US: TBC, SLAC already doing effort
Available resources	TPSCo 65nm 12 FTE/yr 290k/yr TJ 180 nm 1.5 FTE/yr 20k/yr LF 110 nm is 8 FTE/yr 100 k/yr
Addt'l resource need	6.5 FTE/yr 410k/yr (TBC)

Project Description

Common access through the organization of common runs is initially envisaged for the TowerJazz 180 nm, TPSCo 65 nm ISC, and LFoundry 110 nm CMOS imaging technologies, all allowing 1-D and 2-D stitching. These common runs, shared among the clients (for example, other DRDs like DRD3, experiments and projects in HEP) will contain small test chips (chiplets), reticle scale devices and stitched prototypes. A successful run requires assembly of the different prototypes into the reticle, design support (PDK, special design rules, etc.), technology support including TCAD to support sensor optimization, and interfacing to the foundry. Some reruns at much lower cost and effort, with only few mask changes, may be envisaged for sensor optimization. IP development for general use is also foreseen, to accelerate and streamline the design effort. The project comprises several activities:

1. Silicon TPSCo 65 nm ISC Design support of common runs
2. Silicon TPSCo 65 nm ISC Logistics
3. Silicon TPSCo 65 nm ISC TCAD and Technology Support
4. Silicon TPSCo 65 nm ISC Interface to the foundry
5. Silicon TPSCo 65 nm ISC IP Development
6. Silicon TJ 180 nm Design support of common runs
7. Silicon TJ 180 nm IS Logistics
8. Silicon TJ 180 nm IS TCAD and Technology Support
9. Silicon TJ 180 nm IS Interface to the foundry
10. Silicon TJ 180 nm IS IP Development
11. Silicon LF 110 nm is Design support of common runs
12. Silicon LF 110 nm is Logistics
13. Silicon LF 110 nm is TCAD and Technology Support
14. Silicon LF 110 nm is Interface to the foundry
15. Silicon LF 110 nm is IP Development

Table 30 indicates the required and available manpower and resources. With the exception of TCAD, support for 65nm and 180nm designs has so far been provided by designers and physicists in addition to their normal workload. To ensure succesful provision of shared runs in the future, FTEs dedicated to this activity will have to be planned and financed. IP development effort needs to be worked out further, but will be at least 10 FTE in design and test for 65 nm. Significant IP development in 180 nm has already happened, but without preparation and documentation for shared use, and is not expected to be at the same level as the 65nm. If still significant development and activity is to be foreseen for the 180 nm this may amount to an additional 4-5 FTE to be requested, especially if new process modifications are envisaged. INFN has ensured manpower for support and IP development for the 110 nm technology through the ARCADIA project.

Submission costs are to be confirmed after tendering is complete. The extension of the CERN EP R&D program has been approved, but some funding adjustments can still be expected. CERN is tentatively planning to cover half of the cost of the shared engineering runs for 65 nm from its EP R&D WP1.2 program. Synergy will be explored with chips or chiplets, possibly already existing, for the 3D development in 7.6b. No budget is initially foreseen for full 3D-stacked runs, offered in all three technologies, but they may be pursued at a later stage. Thinning and dicing, and fabrication and distribution of one generation of a standardized test setup is presently budgeted at 200 kCHF. In the beginning, existing systems will continue to be distributed to new groups starting the activity. Some measurement equipment for instance for high precision timing, requires

significant investment, not counted here. INFN has secured funding for the first two runs for the LFoundry 110 nm technology. It is assumed that the rest of the submission and other material costs and also the FTEs for support will be carried by the DRDs and experiments taking part in the common runs.

Performance Target

The overall goal of this project is to provide efficient and cost-effective common access to selected CMOS imaging technologies through common runs, provide design support through a common design environment including selected IP, and provide TCAD support for special developments.

Milestones and Deliverables

First milestones and deliverables are indicated in table 30. The main deliverables are the submissions. It is the intention to continue this common access beyond the initial 3 years and therefore tentative submission dates extend beyond this: for 65 nm common submissions are foreseen Q4 2025, Q2 2027 and Q4 2028. For 180 nm common submissions could be foreseen in 2025, 2027 and 2028, if demand is sufficient. For 110 nm, runs are foreseen in 2025, 2026 and 2028.

Multi-disciplinary, transversal content

The project is transversal and multi-disciplinary: monolithic CMOS sensors concern several detector types, calorimeters, tracking, etc, and require specific expertise in analog and digital IC design, device design and technology, and significant testing effort.

Contributors and areas of competence

- **CERN**: has an approved EP R&D program, extended throughout 2028. The detailed budget is still being finalized. CERN intends to finance half of the 65 nm common runs through WP1.2, and a fraction of the additional cost for thinning and dicing and test setups through WP1.2 and WP1.4. A budget is not yet foreseen for stacked runs. At present CERN coordinates and participates in the 65 nm development through its EP R&D and its participation in the ALICE experiment. It has coordinated and participated in several developments of monolithic and hybrid sensors in the past.

- **INFN**: The INFN groups involved on ongoing and future activities employing the LF11is FDMAPS technology are: Torino, Trento (TIFPA), Padova, Milano, Bologna, Perugia, Pavia and Pisa. The ARCADIA budget of $\approx$ 1.4 MCHF covered so far the cost of 3 full-maskset engineering runs (ER) and hardware for DAQ systems. At the time of the writing of this note, the budget for 2 full-maskset ERs during 2024-2026 has been secured by INFN. Also INFN has significant experience in the development of monolithic and hybrid pixel sensors.

- **IN2P3**: has a strong historical involvement in the development of complex imaging sensors through two laboratories: CPPM and IPHC. Large contributions to sensors in the Tower 180 nm and TPSCo 65 nm have been and continue to be carried out for various experimental programs (including ATLAS and ALICE). The work involves design of pixel front-ends, matrix read-out, DACs and specific circuits for radiation hardness assessment. New laboratories – APC, IP2I and LPNHE – are joining the national effort following the ECFA roadmap, with a strong emphasis on the TPSCo 65 nm. In addition IPHC, through its C4Pi facility devoted to MAPS development, also supported by Strasbourg University, could offer support to the community for the organisation of submissions in the Tower 180 nm process. This program is supported by two IN2P3 projects named GRAM and DEPHY, with a planned budget for 3 to 4 years, updated each year. The requests are currently being submitted to IN2P3 and cover a budget for DRD3 and DRD7 CMOS sensors activities. They include two contributions of the order of 120 kEUR for two submissions and additional 30 kEUR/year for common test systems relevant for WG 7.6. The person power involved in DRD 7 activities from these programs is currently estimated to reach 5 FTE/year.

- **NIKHEF**: has been very active in the 180 and 65 nm technology developments within the ALICE collaboration, and has already designed several IP blocks in both technologies, including bandgaps, temperature sensors, PLL, linear regulators. It is interested in providing these blocks as IP in this framework. For the 65 nm it intends to continue the development of a 10 Gb/s transmitter. Together with its 6 University partners it is preparing an application for a large roadmap grant to finance its future R&D, focused on LHC experiments, also with specific interest in high granularity pixel detectors in timing applications. It considers IP development strategic in this framework. It is also interested to later work on future technology nodes.

- **STFC RAL**: has been active in monolithic sensor development for many years. It has recently been involved in 65 nm work together with the ITS3 Upgrade project and the EP R&D Programme. Work so far has been on high speed transmitters, high yield logic gates and power regulation architectures. Work is funded by the UK Infrastructure fund for the Electron Ion Collider, and this would make a contribution to the 65nm FTEs and costs.

- **Norway groups**: The Universities of Bergen (UiB), of Oslo (UiO) and of Southeast Norway (USN) participate in the ALICE ITS2 project since 2016, and in ALICE FoCal and the proton CT project, also using the ALPIDE sensor. Accumulating design experience of ASICs and test platforms, they were involved in testing and qualification of the MIMOSA sensor, of the RD53 chip and its verification, and several irradiation campaigns not only on ALPIDE but also on the SAMPA chip used in the ALICE TPC. They now contribute to ITS3 with verification, testing and qualification, and with studies thinning and bending ALPIDEs at the NorFab facility at USN, which also has some 3D integration experience. UiO coordinated the 3D-MUSE European project on CMOS 3D sequential integration technology also applicable to image sensors, and its Nanoelectronics group has long standing experience with event-based image sensors akin to the read-out concepts of the ALPIDE sensor system.

- **US DOE**: TBC. SLAC is already participating to the 65 nm development with a submission of pixel sensor prototype in the ER1 run and contributing effort to the ALICE ITS3 measurement team. It has extensive general expertise in the design of pixel readout, but also in TDCs and regulators, which it would like to make available as IP in this framework. SLAC is supported by the HEP Detector R&D program directly from DOE OHEP. These funds are meant to support generic R&D. SLAC would like to contribute to the DRD7.6 efforts which synergistically advance research interests in US and at CERN.

- **Participants in common runs**: The experiments, other DRDs, and other teams participating in common runs, the 'clients', are expected to contribute to the expenditure and human resources required for the submissions. In addition to the design activity, a very significant effort in test is expected as well.

- **Contact persons**: M. Barbero, M. Rolo, I. Sedgwick, W. Snoeys.

Available resources, existing funding and frameworks

Table 31 shows the manpower and funding currently assured in participating institutes from the relevant funding framework for an initial three-year project duration. The values are given as averaged annual amounts.

Estimate of to be requested resources

Table 32 shows the manpower and funding foreseen to be requested by participating institutes. In addition to institutes specifically contributing to the organization of common runs and support, the 'clients' participating to the common runs are expected to contribute to the cost of the submissions and of the personnel required to support it. A very significant effort in test is expected as well.

Table 31: Available resources and areas of contribution numbered as in Section B.6.1.

Institute	**Framework**	**Areas of Contribution**
CERN	EP R&D	1-10
INFN	ARCADIA	11-15
IN2P3	C4Pi, GRAM and DEPHY	1,5,6,7,9,10
NIKHEF	Roadmap grant TBC	5,10
NORWAY		5
STFC RAL	UK Infrastructure for EIC	1,5
US DOE	TBC	TBC
	FTE/yr	**Annual Funding** [EUR]
Total available	21.5	410k

Table 32: Resources to be requested. One should consider that requests will be answered in the year following submission.

Institute	**Framework**	**Request submission year**
CERN	–	–
INFN	See text	2023
IN2P3	See text	2023
NIKHEF	Roadmap grant	2024
NORWAY		2024
STFC RAL	–	–
US DOE	–	–
Participants in common runs	TBC	TBC
	FTE/yr	**Annual Funding** [EUR]
Total to be requested	6-12 + TBC depending on demand	430k (TBC)

B.6.2 Project 7.6b: Shared access to 3D integration

This project aims to develop essential technologies for both 2.5D and 3D integration that can be quickly transposed to wafer-to-wafer 3D integration for a wide range of future particle physics applications, ranging from low-temperature neutrino detectors to high-radiation environment HL-HLC pixel detectors. Synergy with the 7.6a will be explored by employing either already existing chips or dedicated test structures. Furthermore, 3D-integration technologies are evolving quickly in industry. Therefore, exploring concrete connections with industrial partners is a key mission of the project.

Table 33: Summary of project 7.6b.

Project Name	Shared Access to 3D Integration (WG7.6b)
Project Description	Develop advanced chiplet and 3D integration technologies, including the integration of SiPh chips on detector, by in-house infrastructures and third-party vendors. Initial duration of 3 years with potential for further prolongation beyond.
Innovative/strategic vision	Potential of silicon interposer and chiplet technologies. In-house infrastructure for quick production of prototypes/demonstrators and test vehicles, by employing bump-bonding and detector packaging technologies already available. To establish a concrete connection with the industrial partners.
Performance Target	Shared competences/experiences and infrastructures/processes. Build up and maintain the capability for a quickly transposed to 3D integration. Keeping a cost-effective access to selected technologies.
Milestones and Deliverables	**M7.6b.1** (M18) Establish TSVs process on Si interposer and dummy wafers **M7.6b.2** (M24) Establish RDL process on Si dummy structures **D7.6b.1** (M30) Delivery of report summarasing the integration of SiPh on detector by 2.5D interposer/chiplet technologies **D7.6b.2** (M30) Delivery of a report on W2W bonding by industrial partners **D7.6b.3** (M36) Deliver documentation of the process for the common use.
Multi-disciplinary, cross-WG content	Strong connection with 7.1 for the integration of SiPh chip and optical fiber on detector module. Strong connection with 7.6a (e.g. 3D integration/chiplets).
Contributors	CA: Sherbrooke DE: MPG-HLL, FH Dortm. KIT NO: Norwegian Institutes (Uni. of Bergen (UiB), Uni. of Oslo (UiO), and Uni. of Southeast Norway (USN)) US: Fermilab (TBC)
Available resources	5.5 FTE/yr 390k/yr
Addt'l resource need	3 FTE/yr 68 k/yr

Project Description

The main mission of the project is to provide access to critical integration technologies for the R&D of future detector prototypes. Access to 2.5D and 3D technologies is initially planned through collaborating institutes by both in-house technologies and industrial partners. The critical technologies to be developed and qualified include the formation of through silicon vias (TSV) for inter-chip connections and redistribution layers (RDL) and back-side metallization on dummy wafers, real CMOS sensors and custom-designed silicon interposer layers. The combination of these two

technologies, along with already existing in-house packaging technologies, will allow for a rapid transition towards the implementation of 3D-ASIC integration at the level of a single assembly (e.g. Multi-Project Wafer). Above that, after the initial three-year project, these technologies will also facilitate a quick transposition to wafer-to-wafer (W2W) direct bonding technologies on 8-inch wafers at the Max Planck Institute.

In addition to in-house activities, exploring and establishing a concrete connection with industrial partners represents a key mission of the project. Sherbrooke University, Fermilab and the University of Oslo (UiO), will collaborate with industrial partners. In particular, Sherbrooke collaborates with Teledyne DALSA for the development and qualification of W2W bonding technology and IZM for detector packaging. Fermilab launched the Chicago 3D Chips Codesign Community to foster the type of ecosystem necessary to push developments in this area and UiO will address the 3D-sequential integration technology under development by CEA-LETI and STMicroelectronics.

The project objective includes also the employment of TSV, RDL and interposer technologies for the direct integration of photonic chips on detector modules. In collaboration with 7.1, the ultimate goal is to establish the necessary process steps to ensure the long-term availability of the integration of silicon photonics (SiPh) chips and optical fibers on already available sensors or test structures manufactured in the technologies offered by 7.6a.

The project will feature various topics to be addressed by different collaborators in order to build a complete picture of the full potential offered by the 2.5D and chiplet technologies. These are:

1. Provide access to TSV technology
2. Provide access to RDL technology
3. Provide access to 2D-bonding process
4. Provide access to chiplet/2.5D integration
5. Provide access to W2W, C2W by industrial partners
6. Integration of monolithic/hybrid PIC on the detector

Performance Target

The overall goal of the project is to provide cost-effective access to critical integration technologies for fast prototyping of future detectors through in-house infrastructure. It will also provide a concrete connection with 3D-integration technologies that evolve quickly in industry.

Milestones and Deliverables

The main milestones consist of the development and qualification of TSV and RDL processes. Both processes are foreseen to be developed at KIT and MPG-HLL in Q2 2025, while the mechanical and thermal qualifications will be executed by Fachhochschule Dortmund. The project aims to consolidate the W2W bonding process through collaboration with industrial partners. The report is foreseen in Q2 2026. The key deliverable is the development of prototypes (test vehicles) of detector modules using 2.5D interposer and chiplet technologies, scheduled for completion in Q2 2026. The development of both technologies will take place using different approaches. MPG-HLL and KIT will employ in-house machinery, whereas Sherbrooke will rely on an industrial partner (IZM-Germany). The main focus of the deliverable is the seamless integration of optical packaging with CMOS sensors (e.g., 7.6a) and SiPM detectors for neutrino experiments (e.g., Sherbrooke). The integration of radhard RISC-V processor and/or bare eFPGA/FPGA with state-of-the-art monolithic/hybrid sensors (e.g., 7.6a) by employing of the aforementioned technologies, will be explored. The prototypes will be carried out by KIT, MPG-HLL and Dortmund within or beyond the initial three years, depending on the availability of the components.

Multi-disciplinary, transversal content

The project has a wide range of applications, such as CMOS sensors (7.6a), calorimeters (DRD6), cryo-detectors (DRD5), and more. Collaborators are skilled in ASIC design, semiconductor sensor fabrication, PCB design, FPGA design, radiation effects, cryogenics and detector integration technologies.

Contributors and areas of competence

- **Semiconductor Laboratory of the Max Planck Society**: fabrication of test devices, development of wafer processing for hybrid bonding (Cu, PECVD oxide), C2C, C2W and W2W bonding processes, AC and DC coupled bonding, low-temperature plasma-activated direct Si-Si bonding and hybrid bonding (Cu-Cu pads embedded in SiO2).

- **Karlsruhe Institute of Technology**: development of 2.5D and chiplet integration technologies based on active/passive interposer layer. Several in-house bumping technologies. Direct integration of optical fibers with SiPh chips by either grating or edge couplers on the detector. Development and production of cryogenic detectors (MMC) and the TSV-last process.

- **Fachhochschule Dortmund**: expertise in analog, digital and mixed-signal CMOS circuit design, chip and module testing. A thermostream climate device for fast temperature ramping from -70° to 225°is available to test mechanical stability and validate chips and modules with respect to PVT.

- **US DOE:** : Fermilab has recognized the significance of 3D integrated circuits to high energy physics for more than a decade and has taken every opportunity possible to involve itself in advanced packaging developments. Most recently, Fermilab along with the University of Chicago has launched the Chicago 3D Chips Codesign Community to foster the type of ecosystem necessary to push developments in this area. The next activity of the community is to partner with IMEC and NHanced Semiconductors to provide a 3D integration on Multi-Project Wafer run to begin in 2024. This is a simple two-layer face-to-face bonding structure with DBI tier-to-tier interconnect, backside TSVs and backside metallization. The wafers themselves will use the TSMC 65nm process. Subscription to the run as well as its final schedule will depend on funding. The most ambitious goal Fermilab has in this area is the creation of an advanced packaging facility that would permit regular MPW runs for the community as well as the ability to develop techniques and standards best-suited to the scientific community as well as the small-volume industrial community. The contribution of the US-DOE team is under discussion due to uncertainty regarding DOE funding.

- **Université de Sherbrooke**: radiation instrumentation for nearly 4 decades, including digital single-photon detectors (photon-to-digital converters –PDC or Digital SiPM), time to-digital converters (TDC), embedded signal processing, and real-time on-detector edge computing for high data rate instruments. Will provide access to Teledyne DALSA foundry for the 3D integration of multiple-tier wafer stacking.

- **Contact persons**: M. Caselle, L. Andricek, S. Charlebois.

Available resources, existing funding and frameworks

Table 34 shows the manpower and funding currently assured in participating institutes from the relevant funding framework for an initial three-year project duration. The values are given as averaged annual amounts.

Estimate of to be requested resources

Most of the funding is secured up to 2027 with the existing projects. German funds BMBF (Si-D consortium) is not confirmed.

Table 34: Available resources and areas of contribution numbered as in Section B.6.2.

Institute	**Framework**	**Areas of Contribution**
FH Dortmund	BMBF (05H21PRCA9, 05H21PRRD1)	4
MPG-HLL	Institute	1,2,3,4
KIT	Helmholtz	1,2,3,4,6
Norway		3,4,5
Fermilab		5
Sherbrooke	CRSNG	4,5,6
	FTE/yr	**Annual Funding** [EUR]
Total available	5.5	390 k

Table 35: Resources to be requested

Institute	**Framework**	**Request submission year**
KIT	BMBF (Si-D consortium)	2023
MPG-HLL	BMBF (Si-D consortium)	2023
Norway		2023
	FTE/yr	**Annual Funding** [EUR]
Total to be requested	3	68 k

B.7 Working Group 7.7: Tools and Technologies

In response to the DRD7 projects detailed above and those related to electronics in other DRDs, and in order to manage ASIC-related design risks in our distributed community, the Steering Committee invites Conveners of WG7.7 to create and steer a task force that will propose an implementation solution for a hub-based structure for ASICs developments.

B.7.1 A Hub-based structure

A few central ASIC development centres defined as 'Hubs' will be established with CERN as the lead focus. On behalf of the DRD7 Collaboration, these Hub centres will be available to support best practice design of a selection of large and complex DRD sponsored ASIC projects within their region.

The overall goal of this Hub-based structure is to:

- Establish and maintain access, for the community at large, to state-of-the art microelectronics technologies and EDA software tools through regional collaboration and coordination
- Ensure a professional approach to prototyping and production fabrication cycles by delivering best practice in design, verification and foundry submission,
- Facilitate collaborative work across distributed design teams establishing the necessary infrastructure for IP block sharing, and
- Follow rigorous project review and submission processes to manage risks and control changes in projects

The Hub institutes will collaborate with their wider region's design groups to deliver a wide programme of sophisticated, complex or large size DRD-sponsored ASICs. They will contribute by ensuring thorough planning, review and design validation in all design fabrication cycles. Then, working with CERN and other Hubs, they will plan and coordinate foundry access for these projects over their lifetime.

In addition, the Hub institutes will collectively:

- Provide access to necessary technical support for projects to ensure rigorous completion of all design validation and foundry design rules checks. Maintain signoff checklists, foundry submission check lists and 'lessons learned' logs to support each other and build best practice
- Coordinate fabrication manufacturing runs and IP library access in partnership with supported foundries, CERN ASIC support and Foundry Services and Europractice
- Maintain a master list of all current projects to enhance global overview and forecast foundry access, and
- Provide advice in ensuring that projects are correctly resourced for the anticipated goals

Locally, in their region, Hub institutes will also:

- Lead the preparation and management of IP sharing agreements that meet the needs of their region
- Ensure that the strict end-use rules, export controls and taxation issues in each region are recognised, understood and met by their community, and
- Engage with their local funding agencies to ensure that support and submission management costs are planned for and included in projects.

The overall objective of the above is to support the wider community so that everyone can continue to contribute and innovate new electronic systems in the knowledge that with their Hub partner they will be able to implement successful ASIC production solutions for their experiments, when needed by the experimental programme. The best way to achieve this objective at project-level is to include from the beginning a Hub institute in all the most complex and risky DRD-sponsored ASIC projects.

B.7.2 Hub roles and requirements

Hub centres will be expected to be equipped and have all the resources and skills necessary to develop and submit full-scale ASICs to supported foundry(ies), making best use of state-of-the-art practices and tools. In addition, they must demonstrate their ability to support a reasonable number of community projects in their region. Practically, Hubs are expected to be large established institutions or national laboratories. Hubs might adopt an infrastructure setup resembling the CERN ASIC support and Foundry service model. This would involve personnel working on design projects and providing support services as necessary.

As members of the DRD7 collaboration, Hubs will participate in Working Group WG7.7 (tools and technologies). They will collectively maintain their expertise through appropriate training, collaboration with industry and engagement in ASIC design projects. They will, wherever necessary, develop "common design platforms" incorporating design kits, IP libraries and design flows and provide long-term maintenance, technical support and training. Funding of Hub support will be achieved directly via centralised national channels, or indirectly via the projects requesting support.

The list of Hub institutes will be agreed and reviewed periodically by the DRD7 collaboration.

In their preparation for complex projects, the community will be invited to discuss and agree the level of Hub involvement required with their regional Hub centre. This could range from active design and/or verification work to just engagement with design reviews.

The DRDC may, based on expert reviews, recommend that a Hub institute is added to the list of project participants, in case it judges that the design is too challenging for the project team as is.

CERN, as lead focus, will coordinate the overall structure and undertake central roles including:

- Negotiating legal and commercial aspects for accessing new technologies on behalf of the community
- Maintaining a list of Institutes eligible to collaborate on NDA protected technologies
- Providing technical support and training to Hub Institutes
- Working with Hub institutes to develop "common design platforms" and to facilitate maintenance, technical support, training and collaboration, and
- Assisting in supporting the wider community when circumstances prevent a regional Hub from doing so

B.7.3 Timeline

The timeline for the taskforce to propose an implementation solution to the Hub-based model sketched above is 12 months. The proposal will identify the hub institutes and their interactions, the supported technologies and target projects, and will propose a roadmap for presenting, discussing and rolling out the new structure for the DRD community.