ISBN: 978-3-95450-231-8 ISSN: 2673-5490 doi: 10.18429/JACoW-IPAC2023-THPA023

DATA ACQUISITION AND SUPERVISION SYSTEMS FOR THE HL-LHC QUENCH PROTECTION SYSTEM – PART I THE HARDWARE*

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Abstract

The protection of the superconducting circuits of the High Luminosity Upgrade of the LHC project (HL-LHC) will be ensured by a new generation of quench detection systems and various quench protection systems for the superconducting circuits and magnets. The HL-LHC quench detection systems serve as well as high-performance data acquisition systems, that also provide essential input for the automatic analysis of events such as a superconducting magnet quench. The supervision of the quench protection systems required the development of data acquisition and monitoring systems adapted to the specific characteristics of this equipment. Of particular importance are the protection device supervision units (PDSU), which are monitoring and interlocking the quench heater circuits and the Coupling Loss Induced Quench (CLIQ) systems. All data acquisition and monitoring systems use Ethernet-based communication with precise timing instead of a classic serial field-bus solution. This approach ensures the required data transfer rates and time synchronisation. The contribution will discuss the specific functional requirements, the status of development and the results of extensive system validation testing. It will also report on the system integration and the preparation for the first deployment in the upcoming IT-String project.

INTRODUCTION

The High Luminosity Upgrade of the LHC project (HL-LHC) introduces major changes to the layout of the interaction points of IR1 and IR5. In order to enhance the luminosity of the ATLAS and CMS experiments, these regions are going to receive an upgraded chain of superconducting magnets, crab cavities and new collimation systems to name a few [1]. Requirements for the new inner-triplet superconducting magnets called for serious technological advances in the domain of magnet design, and in particular, the required larger apertures and peak fields impose the use of Nb_3Sn superconductors. The inner-triplet magnet chain consist of multiple magnets operating in a nested circuits configuration, with varied nominal currents, hence its powering schemes are non trivial. Moreover, the inner-triplets and their protection infrastructure introduce a new beam failure mode, which gives only a few LHC turns for detection and beam extraction [2, 3].

The new generation of quench protection systems (QPS) is going to satisfy tight requirements for protection of these superconducting circuits and magnets. The Universal Quench Detection System (UQDS) [4] enables very accurate magnet instrumentation and high configurability. Hence, the entire quench detection can be based on a common hardware configured to satisfy given protection requirements. The Protection Devices Supervision Unit (PDSU) enables to interlock the Coupling Loss Induced Quench (CLIQ) systems and the quench heater discharge power supplies. This system is capable of detecting a spurious trigger of the aforementioned protection devices in time providing sufficient margin to extract the beam from the machine before its trajectory is substantially affected and becoming dangerous to the accelerator infrastructure.

The quench protection system serves as well as data acquisition equipment with a primary objective to enable accurate instrumentation of the entire protection infrastructure. The complexity of the inner-triplet installation calls for high definition data for three reasons. Firstly, the commissioning phase of the entire infrastructure will be demanding, and in particular because many components are used for the first time in such a scale. Moreover, the IT-String project [5], whose main objective is to build a test installation representing an exact copy of the inner-triplet chain of the insertion region right of point 5, will enable to gather an important operational experience that is expected to ease the commissioning process of the HL-LHC machine. Secondly, the safe and reliable operation will require a complete insight into protection events and methods to assess the state of health of the superconducting circuits and their protection. Lastly, automated analyses can significantly facilitate the operation as well as enable accurate preventive maintenance. High quality data is a key factor to fully utilize it, and the HL-LHC QPS will have potential to pave the way towards it.

SYSTEM ARCHITECTURE

The architecture of the data acquisition and supervision systems is common for UQDS and PDSU. It relies on the fact that the data taking process is deeply embedded in their system design. As a result, they enable to access high resolution instrumentation required by their core protection functions. Furthermore, the system design reassures that these processes are independent. Native high sampling frequency rates and data resolution drove the development of a scalable and high throughput communication system to interface with the QPS supervisory control and data acquisition (SCADA) stack. Completed test campaigns in the framework of Nb_3Sn magnet development [6, 7] were the primary driving factor for requirements for the data acquisition system. Nevertheless, aspects related to the system deployment,

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ISBN: 978-3-95450-231-8 ISSN: 2673-5490 doi: 10.18429/JACoW-IPAC2023-THPA023

maintenance and flexibility played a non negligible role in the definition of the complete set of requirements. The most prominent are the following:

- The system shall provide 10 Mbps data throughput to enable acquisition of QPS data at a rate up to 10 kHz.
- The system shall synchronize to the accelerator timing on the level of sub-μs in order to enable accurate analysis of powering events involving multiple systems.
- The infrastructure shall enable scalability of its size and data rates, and coexistence of networking standards (i.e. 100Base-TX, 1000Base-T and 10Base-T1L/S).
- The communication stack shall enable real time transactions with a small footprint.
- Ionizing radiation tolerance is not required as HL-LHC equipment will be located in shielded caverns.

Network

The Ethernet-enabled data acquisition system – EDAQ, implements a private network for QPS devices. Central points are the Ethernet switch (Juniper QFX5110-48S) and the front-end computer (FEC, Industrial PC, Siemens 2U IPC647E). The switch realizes a star based network with 100Base-TX towards the devices and 1000Base-T to the FEC. The FEC bridges the general machine timing of CERN into the EDAQ network, implements an EDAQ server and runs the SCADA software. Furthermore, it acts as a gateway between CERN's technical network and the EDAQ network and provides relevant interfaces. The communication between the server and QPS devices employs an EDAQ protocol, which uses the UDP protocol for transport. The main reasons for the UDP protocol are interoperability, real-time behavior, limited buffering capability of hardware nodes and a small footprint. The IEEE 1588 Precision Time Protocol (PTP) enables synchronization of hardware nodes to the general machine timing through a dedicated service running on the FEC. The general overview of the network is presented in Fig. 1, while exact details on the networking stack and implementation are presented in another contribution to this conference [8].

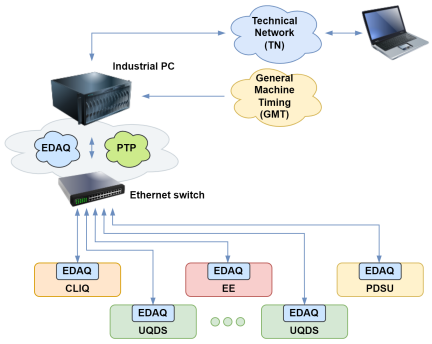

Figure 1: Layout of the EDAQ network.

Hardware

The EDAQ enabled hardware employs a modular design methodology and shares common functional blocks across the systems. This greatly simplified the development process for data acquisition controllers for UQDS, PDSU, CLIQ and Energy Extraction (EE) systems, requiring only a minimal number of iterations. In terms of the integration of the EDAQ controllers into UQDS and PDSU systems two architectures exist. The UQDS platform has its own data processing subsystem based on Microchip's IGLOO2 FPGA. The SPI communication interface exposes the memory that has the configuration and data acquisition regions. The EDAQ controller is a standalone Eurocard form factor (220x100 mm) hardware unit (see Fig. 2), which implements an SPI master interface and a set of unidirectional lines to synchronize data taking and event time stamping processes towards the UQDS FPGA. The circuitry marked in a red rectangle in Fig. 2 constitutes the core part of the system. At its heart is the Cortex-M4F Microchip's SAME54 MCU equipped with a 10/100 Mbps Ethernet MAC with hardware support for PTP and a time stamping unit (TSU). Available RAM memory, an advanced direct memory access (DMA) controller, a powerful event system, and the maximal operating frequency are key features for high-performance data acquisition applications. The MCU is complemented by an Ethernet PHY (Microchip's KSZ8081) and a temperature compensated crystal oscillator (Connor Winfield's T602-040.0M) to ensure good short-term frequency stability.

In contrast to the UQDS platform, the PDSU architecture requires a much higher scale of integration. Hence, instrumentation cards are equipped with up to four analog to digital converters to enable multichannel instrumentation and the system controller card form factor was significantly reduced to 220x100 mm Eurocard. The system controller uses the same FPGA subsystem as UQDS, thus the firmware development methodology and IP blocks are shared. Moreover, the system controller embeds the EDAQ controller block with the same interfaces and technical choices as for the stand alone card. As a result, development of data taking and synchronization processes is streamlined for both platforms and firmware blocks are reused in a great extent.

Firmware

The firmware development methodology for the EDAQ controller leverages from a common hardware approach and a modular architecture of the firmware. The architecture is optimized for the latency and therefore the development strategy is to run the bare-metal firmware. The overview of the hardware architecture and communication interfaces between modules are presented in Fig. 2. The functional modules encapsulate the operational data structures and expose only relevant interfaces in order to reinforce isolation and portability. The hardware drivers, the Ethernet stack, EDAQ communication, EDAQ synchronization constitute common modules and they are reused in all developments. The drivers and the Ethernet stack are Microchip's libraries supplied with the MCU and the firmware uses them with minor modifications. The EDAQ communication module connects to the Ethernet stack and implements the EDAQ protocol, data buffers and the user application interfaces. The

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EDAQ synchronization module enables PTP communication, which is used to evaluate timing error between the node and the master clock. Moreover, the module implements a servo-controller for the local time, and interfaces to synchronize events and provide time-stamping. The application-specific module (i.e. QPS agent) comprises of control state machines performing operational data and post mortem data acquisition, and hardware control through the command processor. The agent module interfaces to the EDAQ modules and the system control module, which performs inter-system communication over SPI. In addition, it controls auxiliary circuitry and application specific hardware.

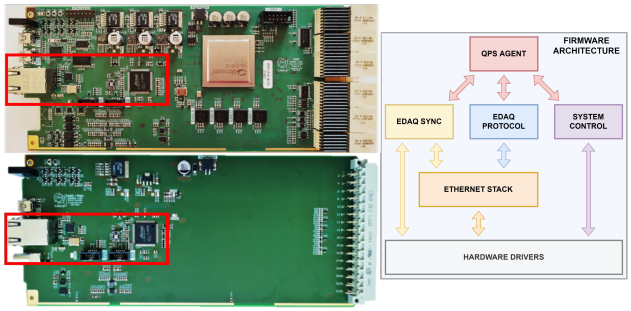

Figure 2: Overview of the EDAQ hardware (left): PDSU system controller (top) and UQDS communication (bottom) cards, and the EDAQ firmware architecture (right).

INTEGRATION AND PERFORMANCE

The integration work of the EDAQ controllers and all required protection systems is in progress. Notably, hardware modules are available and functional. Available firmware implements core features and system specific modules, which enable data acquisition and system control. An important stage of the integration process is the assessment of key performance metrics. The most prominent are the available bandwidth, the sampling frequency, the stability and the accuracy of the system clock. The integration process is the most advanced in the context of UQDS. Furthermore, this system has the most demanding bandwidth requirements, hence it provides a solid framework to evaluate the entire performance. The measured bandwidth of the EDAQ controller running the firmware with core features and an arbitrary data generator is approximately 22 Mbps. The result is satisfactory, and thus the firmware did not receive further optimization towards a higher bandwidth. The data acquisition rate in UQDS system reaches up to 10 kHz with a set of 16, 32-bit integer values. The resulting total bandwidth of the EDAQ controller is 5.5 Mbps and the bottleneck is the slave controller of the internal SPI bus, which is going to receive optimizations towards higher throughput. As a result, the acquisition of larger data sets will be possible. The time synchronization received particular attention and multiple test scenarios enabled a thorough assessment. The measurement conditions used to characterize the performance of the local clock were varied over multiple tests campaigns. However, a common requirement was to use a set of devices

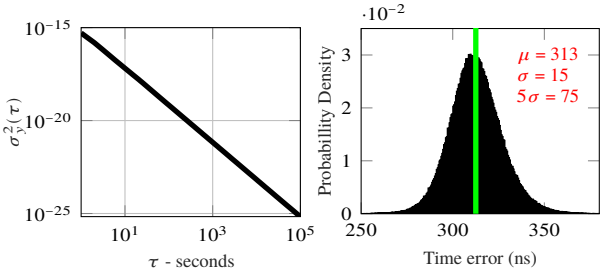

Figure 3: Allan variance (left) and absolute time error (right) of the system clock acquired over 187 h.

connected to the network with the data acquisition processes active. Furthermore, the measurement duration was at least 24 hours and the performance of active systems was monitored. The objective for these measurements was to quantify the clock stability of the EDAQ controller with respect to the accelerator timing. Both clock sources generated a pulse per second (PPS) signals and the accelerator timing system was the reference. This measurement configuration allowed to obtain the frequency stability quantified using Allan variance and the maximum time interval error of the local clock of the EDAQ controller. Both results are presented in Fig. 3. The Allan variance metrics achieved over 187 hours shows a good short term stability of the system that is determined by the crystal oscillator and the clocking circuitry. The mid and long term clock stability reveals performance of the time error measurement and servo-controller modules. The slope and the linear shape of the curve suggests that the configuration is properly tuned, only white noise is present in the system and the oscillator drift is entirely compensated by the servo-controller. The absolute error metrics shows the maximal difference observed between the local clock and the reference clock. The mean value of the error was approximately 300 ns and it was consistent over multiple measurements and among the population of 18 cards. The main contributor to this error is likely due to the asymmetry of transmission and reception paths of the system. The five sigma deviation of nearly 80 ns confirms the overall high stability of the clocking system.

CONCLUSION

The development of the data acquisition and supervision systems for the HL-LHC quench protection system is advanced and they gradually reach readiness for their operational deployment. The developed hardware and firmware enable to cover a broad area of applications and the system can be used as well for other quench protection systems for the HL-LHC installation. The proposed framework enables to share core modules between applications. This approach reinforces stability of the solution and saves the necessary time for testing. The integration of UQDS and PDSU devices reached the phase that allowed confirming the key system requirements. Further works are oriented on implementing all features required for the operation and deploying a full scale installation to gain the operational experience.

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