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SPECIFICATIONS FOR THE INTERFACES OF THE EMAS COMPUTER AND ITS RESIDENT MONITOR

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C O N T E N T S

PART 1

EMAS INTERACTIONS WITH DTS AND PS COMPUTER COMPLEX

1. THE SYNCHRONIZATION OF EMAS

Any exchange of information between the EMAS computer and the rest of the system is embedded in fixed sequences of time intervals (100 msec) synchronized to the PS cycle. The synchronization works as follows (see Fig. 1: Synchronization of EMAS): Starting with M_1 the synchronizer produces after each multiple of 30 M pulses the signal INTR2 which indicates the start of a DTS cycle and enters the computer as INTR2 via the DTS-PDP interface. The synchronizer also resets and starts the DTS. In addition to INTR2 it produces the signal INTR1 if $M = M_1$ to indicate the start of a new PS cycle. The signal gets to the computer as INTR1. The last multiple of 30 M pulses, $M(n \times 30) + 1$, is estimated by the synchronizer. The time between this pulse and the restart of the PS cycle is $\geq$ 100 msec. The delays between the occurrence of INTR1, INTR2 and RESTART DTS are foreseen for saving of interrupted computer programs and preparation of DTS-PDP-11 interactions.

2. THE LINK BETWEEN DTS AND EMAS COMPUTER

The interface DTS-PDP allows, after being enabled by the computer, direct memory access (DMA) in both directions as well as program controlled (PC) transfer from PDP to DTS. The proper sequence of operation is governed by five different interrupt facilities.

The sequence is shown in Fig. 2 (Time scale for data transfer) which gives, for DTS-PDP interactions, a more detailed picture than Fig. 2 in Ref. 1.

The purpose of INTR1 and 2 is described above in Section 1. The minimum time between INTR2 and the first NPR (non-processor request) is 38 μsec. Due to the fact that the timing of EMAS is synchronized to the

PS cycle and not to the computer, the computer must be ready for DMA when the non-processor request occurs. In the DMA transfer towards the computer the DTS addresses, after encoding, are directly used as memory addresses. By comparing them with a prestored DTS address (so-called last address) the end of the transfer is recognized and INTR3 sent to the computer.

Communication between DTS and PDP is finished if for the actual cycle no transfer from PDP to DTS was foreseen. This will be indicated by loading a certain bit in the control status register (CSR) of the interface during the preceding DTS cycle.

In the other case the DTS central unit with its control-signals enters the interface and INTR5 is sent to the computer to start the transfer PDP → DTS. Independent of the transfer mode (DMA or PC) the computer provides data in two-word blocks, the first word being the DTS address, the second word being the appropriate value. In the interface these two words are paralleled and transmitted to the DTS. In the case of program controlled transfer only the word count register (WCR) in the interface is preloaded with the 2's-complement of the number of transfers.

An overflow of WCR after stepwise increment during the transfer indicates its end and provokes INTR3. In DMA transfer a memory address register (MAR) is preloaded with the starting address for the memory block to be read. After the transfer PDP-DTS the computer starts a DTS data diagnostic program. Afterwards communication tasks between the EMAS computer and PS central computer become possible.

In the link system DTS-PDP four different types of malfunction are reported to the computer by INTR4 and setting of certain error bits in the CSR.

Type ∅: Transfer DTS → PDP is not finished within ΔT_0 = 5 msec (hang-up in DTS).

Type 1: The computer does not deliver a couple of words to the interface within ΔT_1 = 28 µsec (hang-up in the computer) during PC transfer.

Type 2: Successive DTS advance signals (AD) do not arrive within ΔT_2 = = 40 µsec (hang-up in DTS) during transfer PDP → DTS.

Type 3: The response-time from slave (PDP memory) to actions of the master (interface) takes more than 5 µsec (hang-up in PDP, e.g. malfunction of unibus or memory).

It is guaranteed that, when a malfunction in one of the two subsystems (DTS or PDP) occurs, the other one continues working.

To avoid interference of unfinished DMA transfers of burst type with the starting DTS scan, foreign DMA transfer is inhibited for the time the DTS transfer takes place. Interrupted transfers have to be repeated.

3. BASIC FUNCTION OF THE LINK BETWEEN EMAS AND THE PS COMPUTER COMPLEX

The link between EMAS and the CONTROL centre is shown in Fig. 3: Link between EMAS and PS computer complex (see also Refs. 2, 3).

Any transfer will start by interrupts to or from the Message Switching Computer (MSC) via the interfaces DR11-C-I, II and their interrupt modules (IM) and distributors (ID). Incoming interrupts will be handled on level BR 4 with a maximum of two interrupt vectors. By action on the CSR in the appropriate DR11-C (for EMAS DR11-C-I) enabling and disabling of the LINK must be guaranteed.

The EMAS, loading the registers WCR and MAR in DR11-B-I, enables a DMA transfer MSC → EMAS of the protocol (header) of the message.

After interpretation of this protocol and further "interrupt" communication between EMAS and MSC, the registers WCR and MAR in DR11-B-I are loaded for a second time to enable the message transfer between EMAS and the PS computer.

PART 2

SPECIFICATIONS FOR A MONITOR TO BE USED IN THE EMAS-PDP-11/45 COMPUTER

1. INTRODUCTION

Unlike other manufacturers DEC does not offer operating systems for small core computers without disc. The disc-based operating systems DOS and RSX-11D occupying 10 to 40 k words of memory only pay for large computer configurations. The EMAS computer is an example for a small on-line real-time processor, where some rudimentary multiprogramming has to be organized. Besides ejection hardware control, a few other tasks like I/O device control, simple background tasks or dynamic loading of programs have to be performed. Hence a moderate operating system (monitor) is required specifically adopted to the EMAS needs.

2. PURPOSE

As a slave of the DTS the EMAS computer has to perform cyclically a defined sequence of real-time tasks (Ref. 1). The strict and immediate servicing of the DTS data transfer and data processing demands will be guaranteed by high priority hardware interrupts described in Part 1 of this note. These main tasks will be executed within a minor fraction of the total DTS cycle-time of 100 msec. The rest of the cycle-time will be devoted to less important tasks, including the input and output control of the Decwriter LA30, of the fast paper tape reader and punch and of the link with the central PS computer(s). In addition it is foreseen to run simple background programs like hardware performance statistics, MD aid programs, etc. The dynamical loading and deleting of such tasks must be feasible during DTS run-time without interruption of the standard DTS real-time programs.

A fixed sequence of hardware control programs could be treated without a special operating system. It is mainly due to the mentioned lower priority tasks that the need for a monitor arises.

The required monitor must provide the basic features of task manipulation: task installation, task activation and deactivation according to

priority, task deletion, and the scheduling of requests for I/O service or other services like de- and encoding. The main software for the hardware control is integrated into the monitor in the form of interrupt service modules. These programs and the other parts of the monitor have to be protected against faulty interferences with the different user programs. This can be achieved by a monitor which includes the memory management facilities (KT11-C) and the different processor working modes of the EMAS PDP 11/45.

3. THE STRUCTURE OF THE MONITOR

The monitor consists of an arrangement of carefully interfaced modules.

a) The basic monitor module

It handles all the fundamental tasks such as dead-start, task switching, queueing and channelling of requests for different monitor services and control of the memory management unit.

b) The interrupt service modules

The most important interrupt service routines concern the DTS interface interrupts INTR1,2,3,4,5 (see Part I), which start or stop the data transfer to and from the DTS. The requests for the DTS-interrupts will arrive at highest priority level (BR7). They can even interrupt the basic monitor program. A running DTS interrupt service routine can only be interrupted by a consequent DTS interrupt. All other interrupt requests arrive at lower priority levels and can be locked out when the basic monitor module runs. The following interrupt service routines have to be written:

I/O - Decwriter (2 modules)
Input - HSR (High-speed reader)
Output - HSP (High-speed punch)
Input - PS-Link (2 modules)
Output - PS-Link (2 modules)
(KW11-P Clock-service)

The I/O routines are handling mainly the character transfer. For interpretation and generation of messages special routines have to be written (see below).

c) Trap handling modules

A minimum number of trap handling routines are necessary to guarantee a safe and continuous long term operation. The following modules are required:

Power fail and restart routine

Memory management trap handler for recovery from attempts to access forbidden memory areas

Recovery routine for stack limit violations.

d) Communication routines

Modules have to be provided for the communication between system or user programs on one hand, and the different I/O devices (including the PS computer link) on the other hand. They decode or encode the messages received or to be transferred and initiate the required actions.

e) Other service modules

In the EMAS computer certain services are frequently needed by the system or the user programs. Decoding and encoding operations like

"BCD" ASCII to Binary conversion
Binary to ASCII - Octal conversion
Binary to ASCII - Decimal conversion

should be implemented as monitor service modules. Also general error routines (software errors, time-out errors, hardware error) belong to this category.

4. MEMORY PROTECTION

A high overall reliability is one of the most important aims in the EMAS control. The ejection hardware surveillance and maintenance software has to be absolutely protected from unintentional or erroneous interferences with peripheric user programs. Together with the appropriate software the KT11-C memory management within the PDP-11/45 is a facility which can supply such a protection to a high degree. Very effective protection can be achieved by using the three processor modes (Kernel, Supervisor and User mode) in connection with the KT11-C unit. The three processor modes can be allocated to completely separated memory areas (Kernel, Supervisor and User space). Interactions between different spaces are controlled by the monitor.

The monitor with all its service routines will reside in Kernel space. All low priority tasks will run in User mode. The DTS data processing program may be placed into the Supervisor space. Only programs running in Kernel (that means, the monitor) will have direct access to the low core interrupt and trap vector area and to the upper 4k I/O page, including the KT11-C segmentation registers and the processor status word. User space programs will not be able to communicate with Kernel program space except by interrupt or trap sequences. Through appropriate mapping certain areas with commonly used tables can be made accessible for several programs running in different processor modes. Since certain instructions like HALT and SPL ("Set Processor Priority") are forbidden in User space the computer cannot be stopped or locked out by a user program.

The additional separation of memory into instruction and data space offered by the KT11-C facility seems to be less advantageous, since it complicates the software considerably compared with the moderate gain in protection reliability which it brings about for such a small core machine like the EMAS computer. Furthermore the KT11-C control need not be dynamical, e.g. the PAR- and PDR-registers can keep constant values during operation.

5. EXISTING MONITORS

Two monitors for PDP 11/20 machines were written, one by P.A. Jeavons and another one by S. Lauper in the DD-Omega-SFM Group. Another monitor was written by B. Carpenter for the PS-PDP 11/10 message switching control computer. Neither of these small operating systems meets all the specifications outlined above for the EMAS PDP 11/45 though their basic ideas of task-switching and request queueing can be accepted. The precedence of DTS interrupts over all other running software can be implemented in either of these monitors. However inclusion of the features of memory protection and dynamic user task installation practically require a complete rewriting of the basic monitor modules and modifications in the service modules which are taken over from one of the existing monitors. To any of the mentioned monitors a large number of specific EMAS service modules would have to be added.

FINAL REMARKS

The second part of this note pointed out the essential reasons for having a small operating system in the EMAS computer to efficiently and reliably perform its tasks. It can be clearly stated that the existing monitors, even with minor modifications, will not meet the requirements for the EMAS computer. Writing a new monitor as specified above will certainly pay also for the other real-time processors to be installed in future around the PS. The development of a suitable monitor was promised by MPS-CO in the initial stage of the PS computerization project (Refs. 4, 5).

The final version of the new monitor must run in January of next year. Design, development and testing of the monitor will take at least 6 months, hence writing of the monitor has to be started immediately.

REFERENCES

1) D. Bloess, H. Kugler, P. Pearce and H. Riege, The ejection computer system, MPS/SR Note 73-2

2) B. Carpenter, Preliminary specifications for the communications monitor and message switcher software in the PS multi-computer system, MPS/CO-Note 73-9.

3) J.H.B. Madsen, Minutes of meeting No. 13 of the CC, 2nd May 1973.

4) J.H.B. Madsen and H. v.d. Beeken, Memorandum, 1.12.1972.

5) J.H.B. Madsen, Status report on the controls engineering work in the PS, 17.1.1973.

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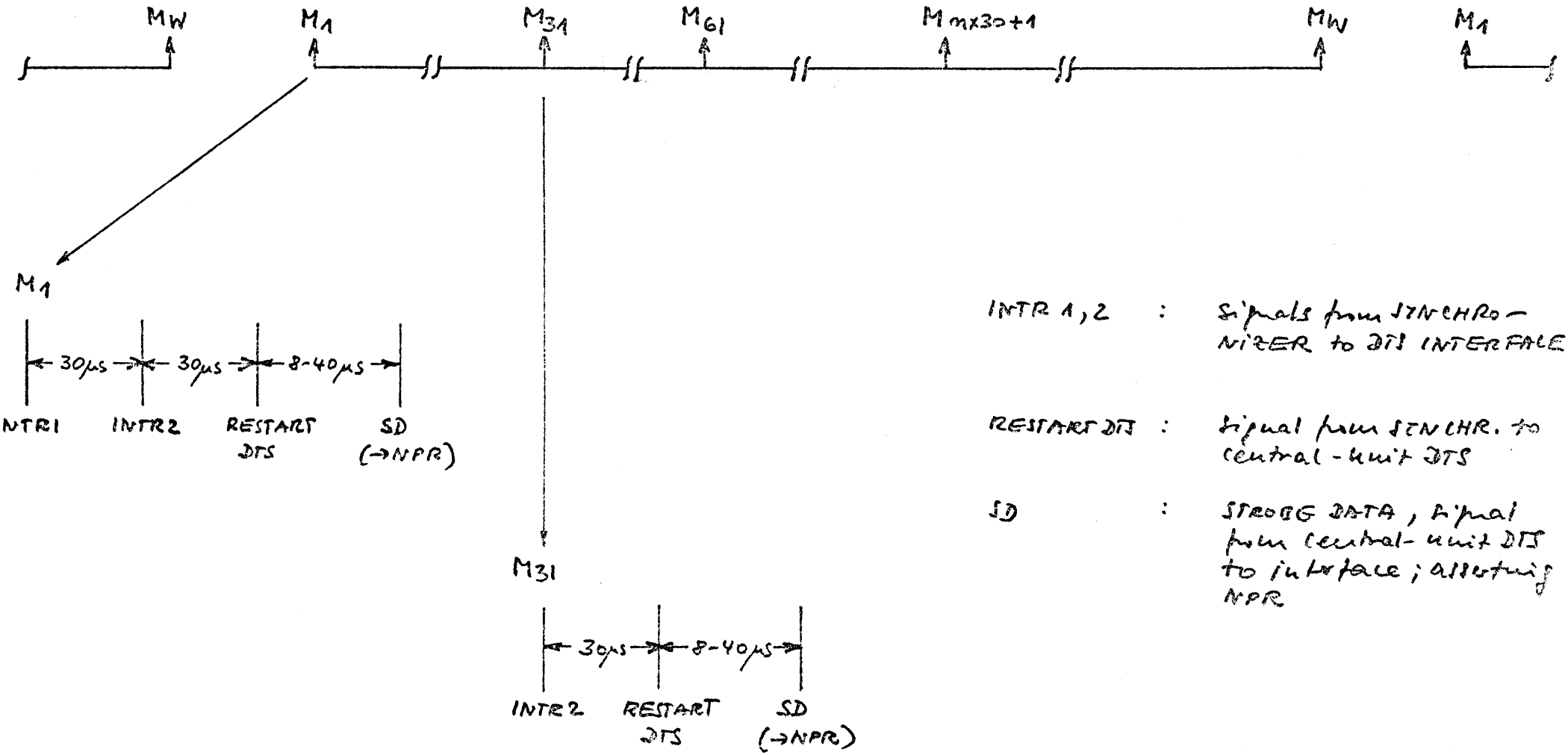
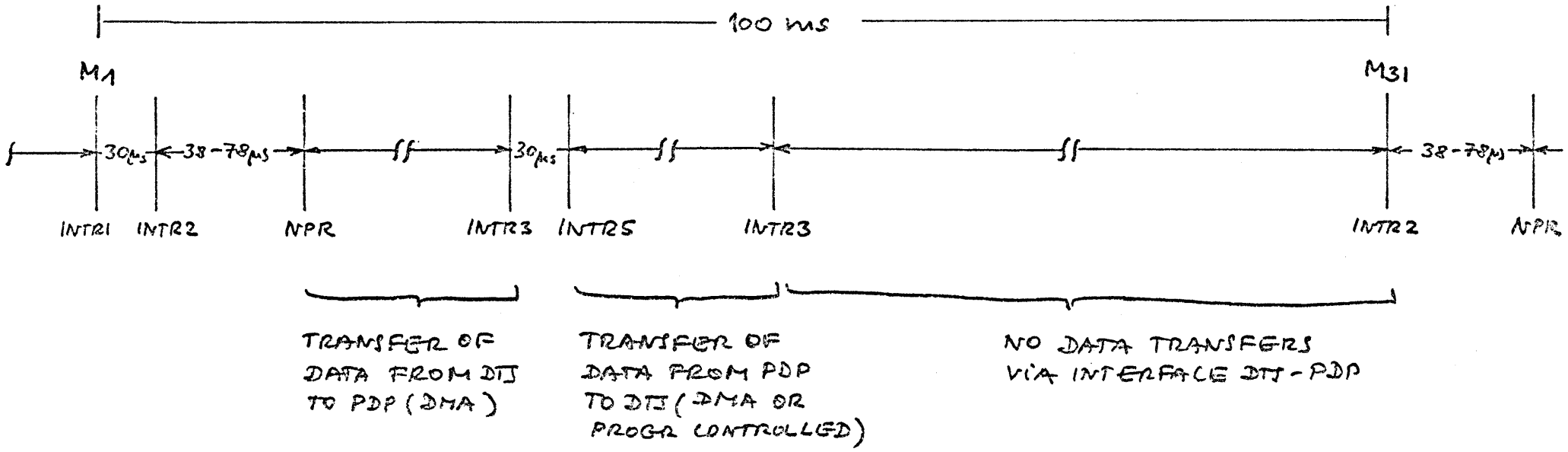


INTR 1,2 : Signals from SYNCHRONIZER to DTS INTERFACE

RESTART DTS : Signal from SYNCHR. to central-unit DTS

SD : STROBE DATA, Signal from central-unit DTS to interface; allowing NPR

FIG1 : SYNCHRONIZATION OF EMAS



INTR1 : indicates start of PS-cycle

INTR2 : indicates start of DTJ-cycle

INTR3 : indicates end of DATA-transfer

INTR5 : indicates that the DTJ treats the interface as measuring-unit and wants data

FIG 2 : TIME SCALE FOR DATA TRANSFERS BETWEEN DTJ AND PDP11

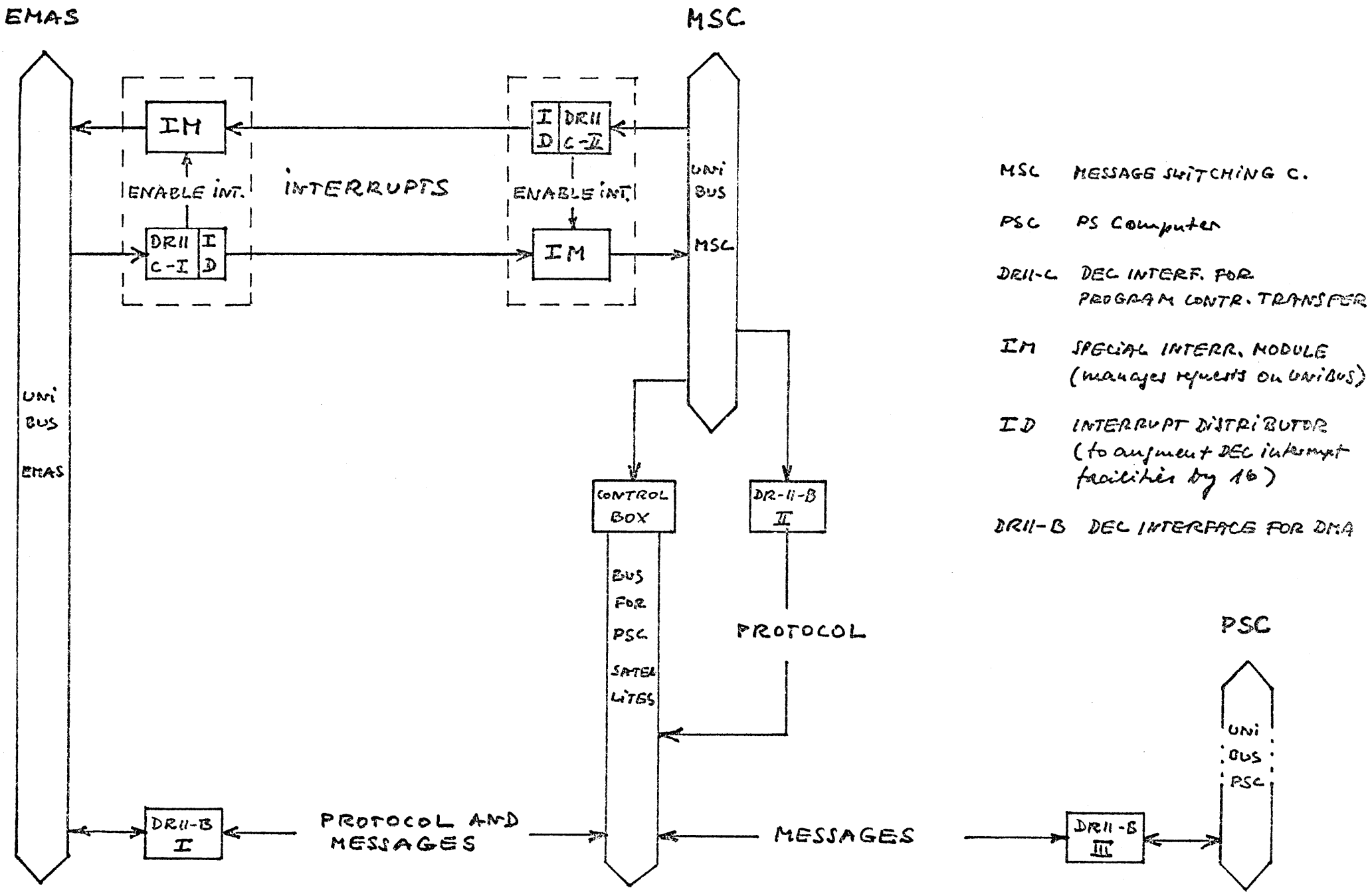


FIG. 3: Link between EMAS and PS-Computer Complex