CHOICE OF A MINI-COMPUTER FOR

AN EJECTION MAINTENANCE ASSISTANT SYSTEM (E.M.A.S.)

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1. General Remarks

In May the use of a small computer for an Ejection Maintenance Assistant System (E.M.A.S.) was proposed (MPS/SR/Note 71-8). This proposal included a rough preselection of small computers. In the

meanwhile 8 of 9 manufacturers were contacted directly; they sent information material as well as price lists. Most informations concerning Modular One were gathered from contacts entertained by CTL and DD-Division, CERN.

2. Some Reasons for the Exclusion of: Mitra 15, Modular One, SPC 16, H 316, SYN 909 and SEL 72.

2.1 Mitra 15:

Mitra 15 is the recent development of CII, it has modular structure with multipurpose registers, it is very fast (0.8μs cycle-time) with flexible I/O facilities (minibus). This machine, however, will not be on the market before September 71 and cannot be delivered before Spring 72. In June a manual was not yet available. Till now, software is tested on machines simulating this new computer only (e.g. CII 10070, IRIS 50, IBM 360). The price for our configuration will be > 97 k Frs.

The lack of experiences on this brand new machine and its price prevent its choice.

2.2 Modular One:

This machine is unique in its multiprocessor structure, it is very fast (0.75μs cycle-time), it is ideal for multi-user systems. This, however, involves a complex and ambitious software; people at Rutherford Laboratory who bought one of the first machines (2 years ago) are waiting until now for sufficient software. Maintenance could not be done but from Paris or Hertfordshire. The price of our configuration would be 180 k Frs.

2.3 SPC 16:

SPC 16 is a very powerful machine (80 instructions) with general purpose registers, it is fast (0.96μs cycle-time) and in fact the fastest machine (of our collection) in interrupt servicing. The main reasons for its exclusion are the far away maintenance

places (Aachen), another that there is no machine at CERN or convenient near to CERN to gain and exchange informations and experiences on its operation and programming and that its price for our small configuration exceeds 90 k Frs. already.

2.4 H 316:

H 316 is a proven machine, it is on the market since $2\frac{1}{2}$ years. It has well established software. However, it is relatively slow (1.6μs cycle-time), it has no general purpose registers (it has one index registor only), it has poor addressing modes and a slow DMA data transfer rate of $3 \cdot 10^5$ W/sec. Multiplication by software takes more than 258 μs

2.5 SEL 72:

This computer is already a medium size computer, it is very fast (0.8μs cycle-time) with a powerful soft- and hardware combination. It is, however, not fully applicable but with the use of a disk. This makes the machine rather expensive for our low level data processing. The price for a configuration fitting our tasks will be more than 130 k Frs.

2.6 SYN 909:

SYN 909 is the European version of GRI 909 (GRI Computer Corporation, Mass., USA). It has general purpose registers and is fully modular. However, it is the slowest machine of our collection (1.7μs cycle-time), to use it optimally for programming and operation, two expensive front-panels are needed; the nearest place from where maintenance could be done is not yet known (Paris, Strassbourg?). Only 10 machines are on the French market. The price for our small configuration exceeds 90 k Frs. already.

2.7 TABLE I

GENERAL INFORMATIONS AND COMPUTER CONFIGURATIONS

Model	MITRA 15/20	MODULAR	SUPERNOVA	PDP 11/20
On the market since:	not yet	1968	1970	MARCH 70
Machines now on the market	NO	80 [7]	EU : 10	EU :~ 100 USA :~ 900
Configurations	Proc. UC Mem. 2x4 K 1 DMA Multiply/Divide gen. I/O Interface interrupt unit real-time-clock PFS [1]	Proc. 1.11 Controller 1.220 2 interfaces 1.22 2x4 K Memory 1.21 Peripheral I/O-Multiplexer 1.051 Keyboard Console 1.311 ASR 33 I/O-Interface [3]	Central Proc. 8001 PFS 8006 Multiply/Divide 8007 High speed data channel 8009 I/O-Controller 8022 Expans.Channel 8024 2x4 K mem 8003 real-time-clock 4088 I/O-Subassembly 4007 TTY/O 4010A Gen. Purp. I/O 4040	PDP 11/20-CB MM 11-Fx4 mem Arithmetic hw KE 11-A real-time-clock KW 11-P Gen.Purp.Interface DR 11-A
Prices k Frs.	97 [2]	186	88	75
Nearest Maintenance	LYON	PARIS or HERTFORDSHIRE	GENEVA	GENEVA or CERN
Machines at CERN [4]	NO	NO	NO	3 [5]
Other machines of this company at CERN [4]	1 CII 10070	NO	NO	20 (PDP 8/9/10/15)

[1] : PFS = Power Fail Safe
[2] : verbal information 97 k Frs. without real-time-clock
[3] : numbers are taken from manufacturer's catalogues or price-lists
[4] : list of CERN's small computers (DD-Division, 11th June 1971)
[5] : two other machines come to CERN in the next months
[6] : partly verbal price without real-time-clock
[7] : information from CERN-Small-Computer-File (DD-Division)

In general, delivery time is 3 to 4 months

Mitra 15 cannot be delivered before spring 1972

SPC 16	H 316	SNY 909	SEL 72	620/F
MAY 70	APRIL 69	1969	SEP. 68	MAY 71
EU : ~25	EU + USA: ~2000	EU + USA:200 FRANCE :~20	EU + USA: 150 [7]	
Proc. + 8 K Mem 1 4-0250 Multiply/Divide 1604-0004 TTY ASR 33 1362-8006 DATA ADAPTER 1665-1000 DATA-Multiplexer 1658-1000 DC (Direct Memory Access) 1659-1000	Proc. + 8 K Mem. ASR 33 DMA Multiply/Divide Interfacing	Proc. 40001 Mem. 4 K 40003 Panel Prog. 40006 PFS 40024 Arithmetic 40102 6 Gen. purpose registers 40122 DATA I/O TTY 42001/2 ASR 33 42003 I/O 47005 47015 real-time-dock 40007	Proc. + 4 K Mem. + 32 K DISK ASR 33 7200 DA-channel 7240 DA-interface 7245 Priority Interrupt 7251 Multiply/Divide 7220 PFS 7241 I/O-Multiplexer Real-time-clock 7211	620/F-002 Multiply/Divide 620/F-10 PMA 620/F-12 PFS 620/F-14 BIC 620/F-20 TTY + Controller 620/F-06 PIM 620/F-16 Buffer I/O Control. 620/F-80 real-time-clock 620/F-13
93	84 [6]	90	132	91.3
AACHEN	BULL	? (Strassbourg)	RUEIL-MALMAISON	PARIS (BASEL)
NO	NO	NO	NO	1
NO	1 (DDP 516)	NO	NO	3 (620/I)

3. Final Selection (please refer to Tables I and II)

3.1 Hardware Performances

3.1.1 Memory

All machines are sufficiently fast (cycle-time<1µs). SUPERNOVA offers a time overlap of fetch and execution phase. This technique is however limited to read-only-memory. PDP 11/20 uses an interleave technique by assigning successive locations to alternating 4 K blocks of core memory. This reduces memory cycle-time for most operations by nearly 50 %.

3.1.2 CPU

Supernova and PDP 11 are multi-accumulator machines. This feature reduces the use of memory-cycles and facilitates programming. PDP 11 (8 general purpose registers) offers the higher flexibility. Varian 620/F has two accumulators (one of which can be used for indexing) and one index register only. PDP 11 has a read-pause-write cycle available which offers the possibility of high speed operations of special purpose hardware.

Comparing addressing modes and instruction set, PDP 11 is the most flexible and powerful machine.

3.1.3 I/O structure

Supernova as well as Varian 620/F offer three different I/O facilities involving an extensive interfacing. The unibus structure of PDP 11 is easily accessible. An interface on the level of interrupt controlled I/O can be extended to handle high speed direct memory access.

The unibus is fully asynchronous which eliminates time losses due to synchronisation processes.

3.2 Software

To judge software quality objectively demands programming and running of each machine for a sufficiently long time. Besides the

fact that we must come to a decision within a foreseeable space of time [ref. MPS/SR/Note 71-8] these studies easily double the real price for the machine and make any choice uneconomical, so some other aspects like exchange of informations and machine simulation must be considered.

The possibility to profit from experiences and to exchange information with other people using the same machine is given for VARIAN 620/F as well as for PDP 11/20. A possibility to test and check programs on a simulated machine - which frees the own machine for other tasks in the meanwhile - exists for PDP 11 on PDP 10. Programs can be assembled on other CERN machines e.g. CDC 6600 (A. Jeavons, DD-Division, report in preparation). Further it exists already a PDP 11-User-Group at CERN to deal with software.

3.3 Maintenance

The maintenance for VARIAN 620/F comes from Basel. People working on this machine mention however, that in general the service in Paris must be consulted. The maintenance for SUPERNOVA will be done by SEN (Geneva). Until now, nobody at SEN has any experiences with this machine. (SEN saled 1 Nova and about 4 Novas 1200 in Switzerland).

The maintenance of PDP 11/20 can be done by somebody who stays at CERN.

Taking into account all informations and machine performances results in the choice of PDP 11/20 to solve our maintenance problems.

SUPERNOVA and VARIAN 620/F have (for our application) serious drawbacks and should only be considered if there exist strong reasons.

H. Kugler

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3.4 TABLE II

DETAILED PERFORMANCES OF SUPERNOVA, PDP 11/20 AND 620/F

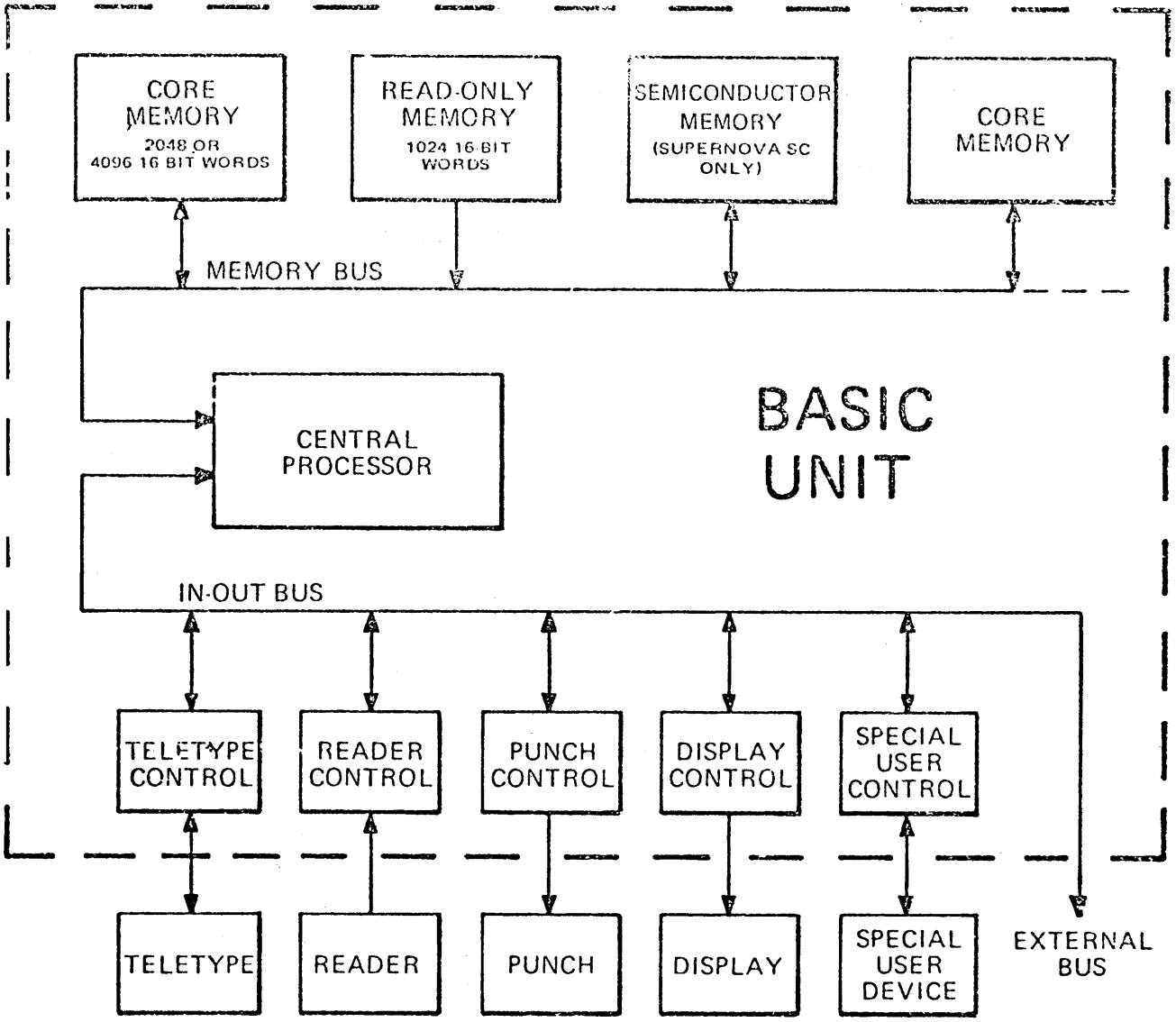
MODEL	SUPERNOVA	PDP 11/20	VARIAN 620/F
MEM word length [bits]	16, (8)	16,8	16
core cycle-time [ns]	800	950 (490 interl)	750
mini word size [K]	4	4	4
increment size [K]	4	1,2,4	4,8
rom cycle-time [ns]	300	350	300
word size (s) [K]	1,2,4	1	2,4
parity check	NO	*	NO
Me allocation protect	OPTION	OPTION	OPTION
other mem. features	rom {fetch + exec.phase overlap	core {interleave (4+4) 8 K necess.	---
CPU: max no.of reg.usable as accumulators	4	8	2
as index registers	2	8	2
as general purpose-registers	2	8	-
addressing modes	absolute (0-256) indexed relative indirect auto-increment auto-decrement	register register deferred auto-increment auto-increm. deferred auto-decrement auto-decrem. deferred indexed indexed deferred immediate absolute relative relative deferred	direct relative pre-indexing post-indexing indirect indir.-indexed immediate extended
words direct. addressable	1K	32K	2K
instruction set (standard) (MUL, DIV. not included)	185 instructions combined of: mem. ref. instr. arithm. + logical functions I/O-instructions special instruct. (e.g. interrupt serv.)	>400 [8] combined of 63 instruct. move, binary + unary arithmetics, shifts, logical operations, branch + subroutine calling, proc. state modifications and addressing modes no I/O instructions necessary	141 combined of load-store, arithm., logical, control, shift, change, jump, execute, extended, double-word adressing, I/O instruct.
Arithmetic op. capability			
add-time for a full word [ns]	800	< 2000	1500
multiply t.p. } OP [µs]	(3.8), 5.4 max.	4.3	3.1-7 max.
divide t.p. }	6.9	4.8	7.0
I/O structure	1) program controlled 2) data channel ST 3) high speed chann. OP	unibus structure fully asynchronous	1) party-line 2) DMA-channel ST 3) high-speed-channel PMA, OP

high speed data transf. [MHz]	1.2	1.11 (with interleave mem.: 2.04 IN, 1.25 OUT)	1.33
response time on request [µs]	4.5	3.5	4.9
max. data transf. under interrupt control	0.434 MHz		0.275 MHz
response time [ns]	5(with M/D:9)	7.2	
priority interrupt levels	1 party line	4	64 OP
max. no. of external interr	62	unlimited (32 K)	64 OP
Power fail safe (PFS)	OP restarts programme at location 0	STANDARD	OPTION
Basic software package usable in our configuration	standard assembler relocat. assemb.(4 K) relocat. loader editor, debugger 2 basics, math.-rout. floating point interpreter, diagnostics macro-assembler	standard assemb.(4,8K) absolute loader editor on-line debugger IOX-executive floating point and math. packages (relocat. assembler)	assembler subroutine libr AID II MAINTAIN

[8] : estimated by DEC

* originally not foreseen in PDP 11/20
mem. with 18 bits already available : MM 11-FPX

SUPERNOVA



TYPICAL NOVA SYSTEM CONFIGURATION

supplies all timing information needed for the execution of that function. A device control unit usually requires timing circuits for its own internal operations, but no timing functions need be performed by the circuits that connect to the bus – all such timing is supplied by the processor in the signals sent over the bus control lines. Moreover the control lines are set up so that a given device need connect only to those that correspond to the functions the device requires.

Within the basic enclosure the bus is simply printed connections from one subassembly slot to another. If the bus must run out of the basic enclosure, the external bus is in the form of a cable composed of fifty twisted pairs in a single black covering. External bus wires must be terminated at the far end to match the characteristic impedance of the cable; this allows the transmission of high speed digital pulses without reflections or ringing. The cable has very low interpair crosstalk and high surge impedance so individual twisted pairs do not require separate shields. With this system a number of bus drivers can be connected to a single data line, and data may be transmitted and received directly with ICs at distances up to 50 feet (including internal wiring) with good noise margins and low signal delays.

A2

PDP11

machine state flow: F fetch
SO source
D destination
E execute
SE service

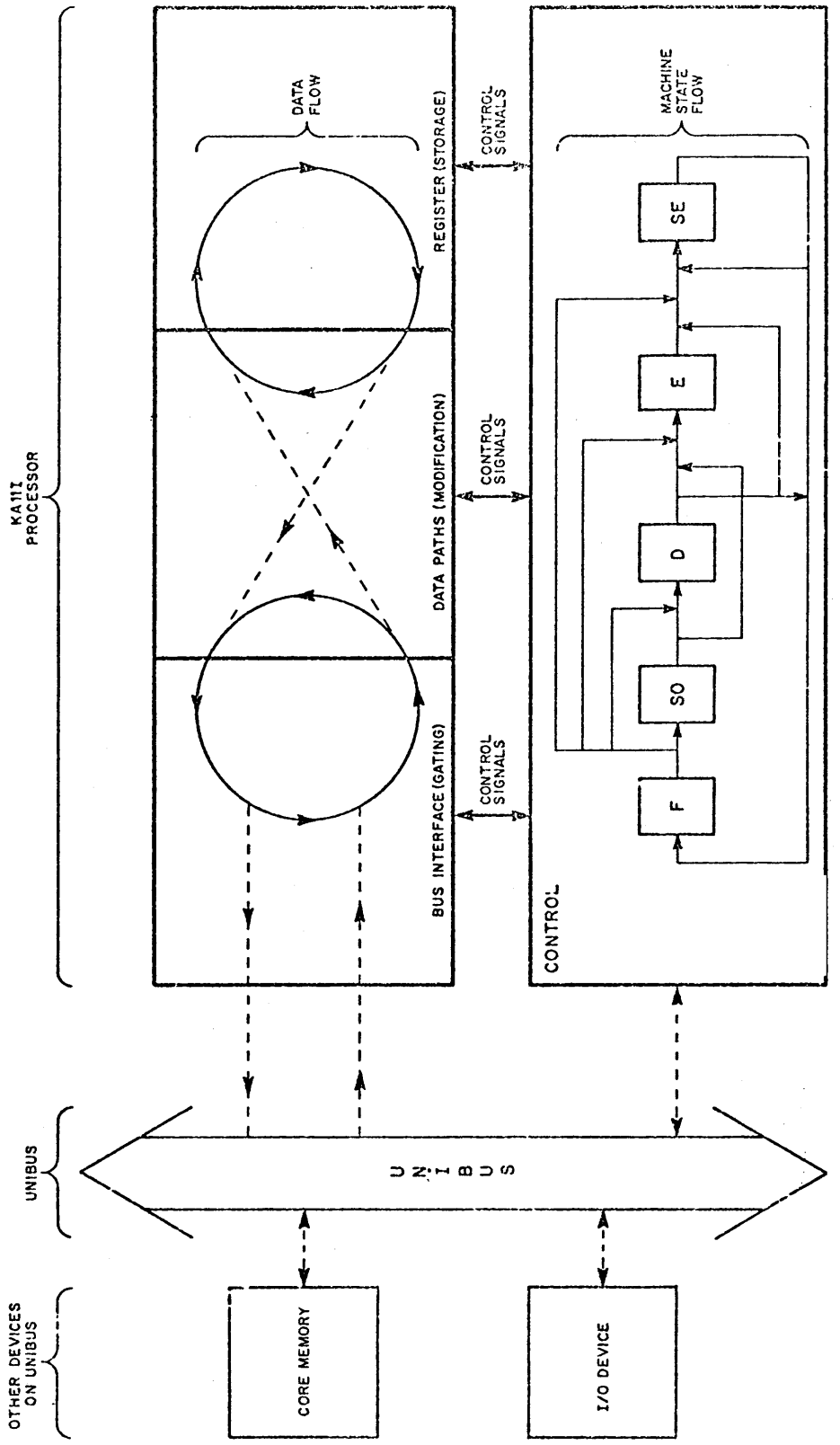


Figure 1-1 KA11 Simplified Block Diagram

VARIAN 620/F

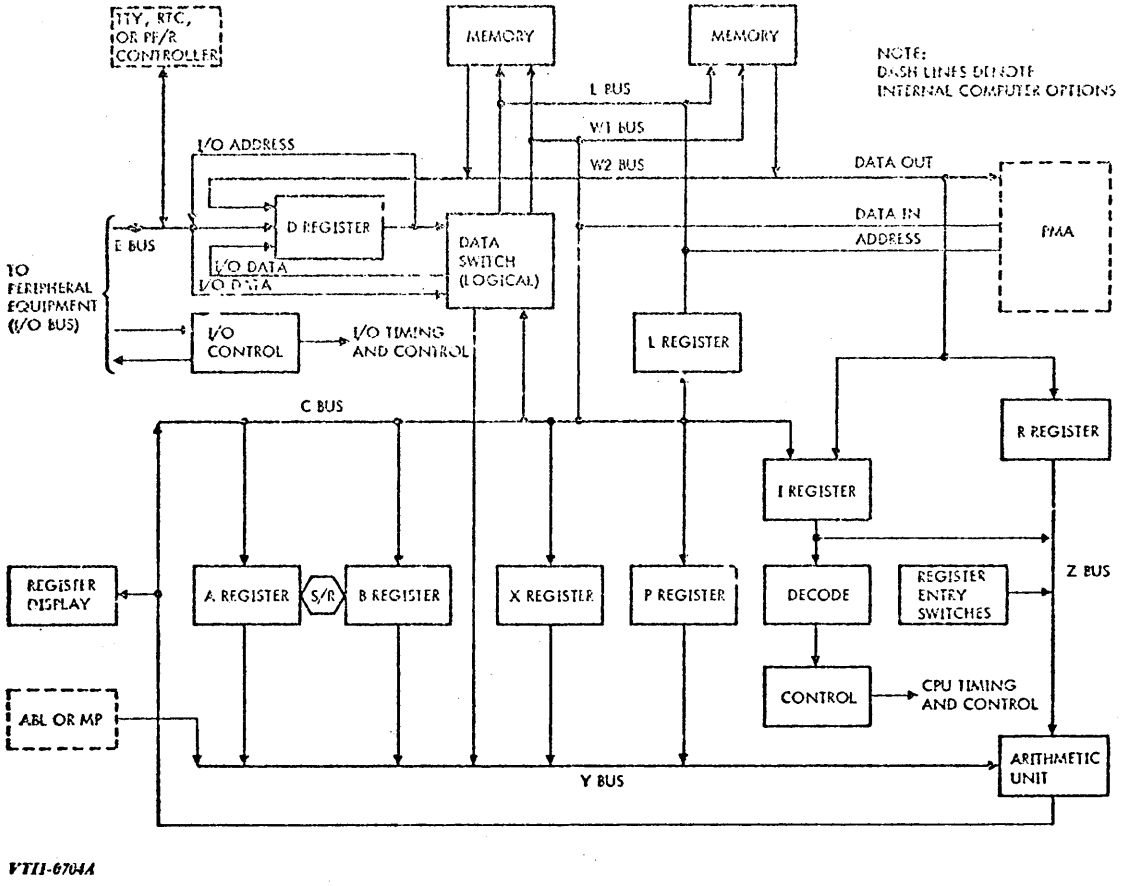


Figure I-1. Computer Functional Organization

(S/R) shift / rotate

A, B accumulators (B also for indexing)

X index reg

P program counter

I instruction reg.

L mem. addr. reg.

R arithm buffer reg.

D I/O reg.

PMA priority mem. acc.

MP memory protect

ABL automatic bootstrap loader