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An ultra-low power 10-bit, 50 MSps SAR ADC for multi-channel readout ASICs

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Abstract: The design and measurement results of a fast, ultra-low power, small area 10-bit SAR ADC, developed for multi-channel readout systems, in particular for applications in particle physics experiments, are discussed. A prototype ASIC was designed and fabricated in 130 nm CMOS technology and a wide spectrum of static (INL < 0.4 LSB, DNL < 0.3 LSB) and dynamic (ENOB = 9.45) measurements was performed to study and quantify the performance of ADC. The ADC converts analogue signals with a sampling frequency up to 55 MHz and power consumption below 1 mW. The ADC works asynchronously, so no external clock is required. The ADC Figure of Merit (FOM) at 50 MHz sampling frequency is 24 fJ/*conv.-step*, and is the lowest among the State of the Art designs with similar technology and specifications.

Keywords: Analogue electronic circuits; Digital electronic circuits; Front-end electronics for detector readout; VLSI circuits

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1 Introduction

With new challenges for higher spatial and time resolution in particle physics experiments [1, 2] the demand for high-granularity and high-channel density detector systems is continuously increasing. This directly translates into the requirements for readout electronics, especially in terms of high-speed and ultra-low power multichannel front-end Application-Specific Integrated Circuits (ASICs). While signal processing in the ASIC may be performed either in the analogue or digital domain, it is much more efficient when digitised samples are already available in a front-end ASIC and Digital Signal Processing (DSP) can be applied directly. Although the integration of a fast Analog-to-Digital Converter (ADC) in each readout channel is natural and results in a simple and elegant architecture, it had been a bottleneck in past readout systems due to excessive power consumption [3]. The availability of deep-submicron CMOS technologies and the rapid advances in ultra-low power ADC architectures made it possible to overcome these limitations. In particular, the Successive Approximation Register (SAR) ADCs are among the fastest growing due to their simplicity, low component count, and low power consumption [4, 5].

Today, it is feasible to design a multichannel front-end ASIC comprising fast, medium, or high resolution, and a small area ADC per channel, where the ADC power consumption is only a small fraction of the total power consumption of the chip. An example of such development is a 32-channel SAMPA readout ASIC, designed for detector upgrade in the ALICE experiment at CERN [6, 7],

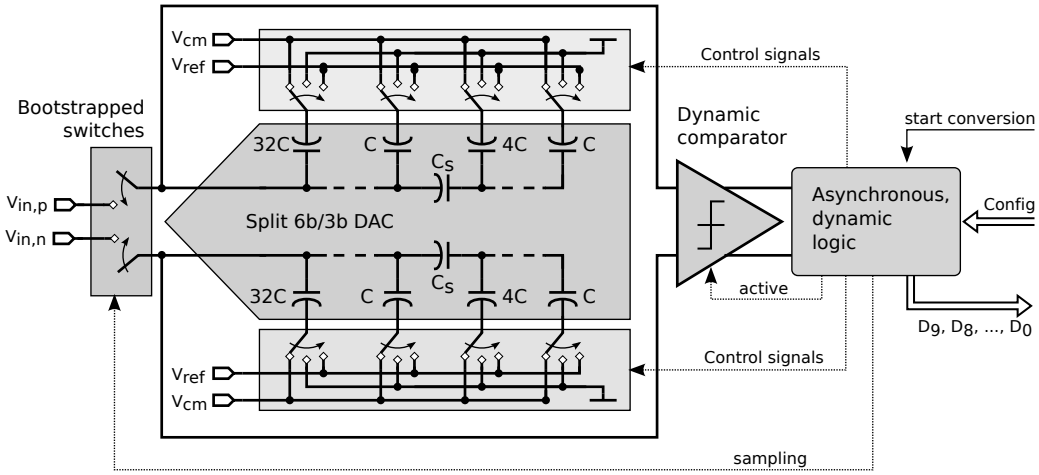

Figure 1. Block diagram of 10-bit SAR ADC.

which contains 10-bit SAR ADC in each channel sampling at 10 MHz. For applications in future particle physics detectors one of typical requirements regarding speed is a sampling frequency of at least 40 MHz, which corresponds to the beam crossing frequency in the world's largest accelerator, the Large Hadron Collider (LHC) at CERN [8]. Recently, the first 128-channel front-end ASIC containing a 6-bit ADC in each channel sampling at 40 MHz, has been developed for the readout of the Upstream Tracker subdetector of the LHCb experiment at CERN [9]. For various detector systems, e.g., calorimetry, a much higher amplitude resolution of 10 or even more bits is required.

The goal of this work was to develop an ultra-low power (< 1 mW/channel), small-pitch (and area) general purpose 10-bit ADC with a maximum sampling frequency beyond 40 MHz. As mentioned above, such an ADC is suitable for multi-channel readout ASICs in particle physics detectors, particularly in LHC experiments. For the considered applications, radiation hardness is often one of the important issues. Radiation studies fall outside the scope of this paper; however, the 130 nm CMOS process used in this work has been shown to be radiation-hard [10]. The article consists of two main sections, the first of which describes the ADC design, and the second presents the measurements made on the ADC prototype. They are followed by the comparison to the State of the Art and conclusions.

2 ADC design

The requirement of very low power consumption of the designed ADC naturally led to the choice of the SAR architecture with a capacitive Digital-to-Analog Converter (DAC), as shown in the block diagram in figure 1. To achieve additional power savings, all its blocks are designed to dissipate power only during conversion, completely eliminating static power. The ADC is fully differential and consists of a pair of input sampling circuits, a pair of DACs, a comparator, and a SAR control logic, similarly to the previous design [11], done in another 130 nm CMOS process. The actual implementation is a new design driven by the best compromise between ultra-low power consumption, the highest effective resolution, and maximum speed at the same time. The design was optimised for 10-bit resolution, but an option was added to reduce the resolution in one-bit

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steps down to 5 bits. This was done to extend the functionality and see how lower resolution could be traded for higher speed and lower power consumption.

2.1 Analogue ADC part

The analogue part of the circuit consists of a differential input sampling circuit, a differential DAC and a comparator. For the lowest sampling resistance and the best linearity, a pair of bootstrapped MOS switches [12, 13], shown in figure 2, was used to sample the input signal. The key feature

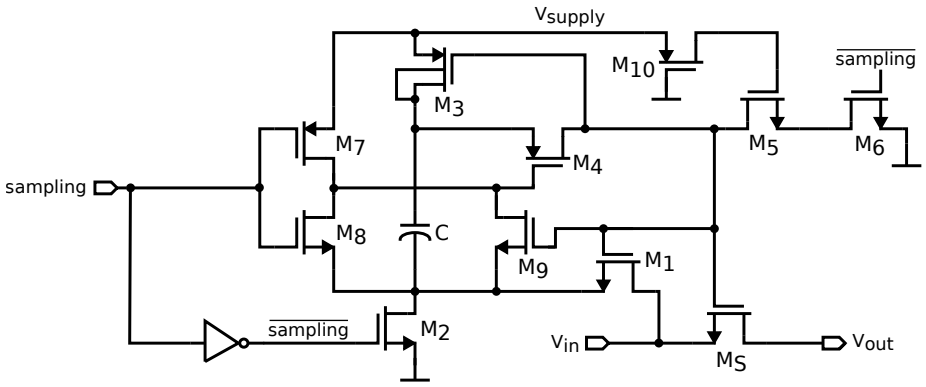

Figure 2. Schematic diagram of the bootstrap switch.

of the bootstrap switch is to make its resistance independent of the amplitude of the input signal, which is achieved by keeping V_{gs} constant in the M_S transistor. This is obtained by keeping the voltage across the capacitance C constant (roughly equal to the supply voltage).

In the literature, numerous capacitive switching DACs schemes have been proposed to achieve the highest power efficiency [14]. In this paper, the Merged Capacitor Switching (MCS) [15, 16] scheme was used. Furthermore, since the best capacitance matching in the chosen CMOS process is provided by relatively large Metal-Insulator-Metal (MIM) capacitors, a split capacitor DAC scheme was applied (see figure 3). Thus, a much lower effective unit capacitance than the physical one C_u= 26.2 fF, can be obtained. It was possible to use the physical capacitance much smaller than the one used in previous design (C_u= 40 fF) [11], because the present CMOS process has much better matching than the previous one. On the other hand, the total DAC capacitance is high enough so that the kT/C noise is still negligible.

Three versions of the ADC have been designed, differing in the segmentation of the capacitive DAC. The default 6-1C-3 (6-bit sub-DAC for the most significant bits, C-split capacitance, and 3-bit sub-DAC for the least significant bits) showed the lowest dispersion in Monte Carlo simulations. The other two DAC segmentations, namely 6-2C-3 and 5-1C-4, were designed to verify the ADC performance with reduced input capacitance to about half of the default one.

All ADC versions use a high precision dynamic comparator to eliminate static power. The designed circuit, shown in figure 4, consists of two gain stages and an output latch [17].

2.2 SAR control logic

The control logic was implemented as asynchronous and dynamic. Asynchronous logic eliminates the need for the generation and distribution of fast bit-cycling clocks and, therefore, greatly simplifies

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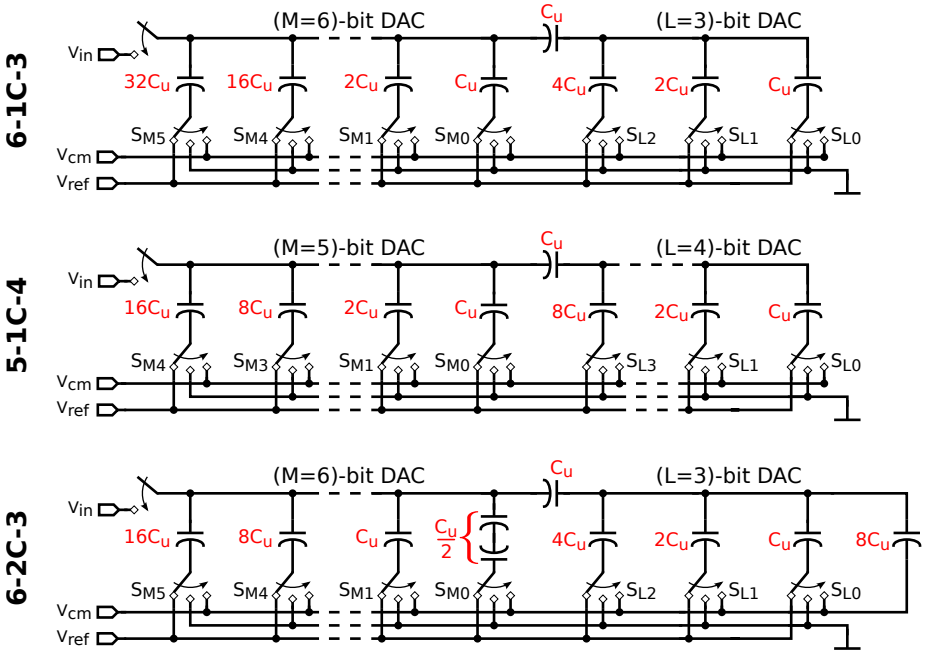

Figure 3. Capacitive DACs with 6-1C-3, 5-1C-4, and 6-2C-3 segmentations (C_u= 26.2 fF). The total input capacitance of the DAC is 1.674 pF for 6-1C-3, 0.837 pF for 5-1C-4, and 0.85 pF for 6-2C-3.

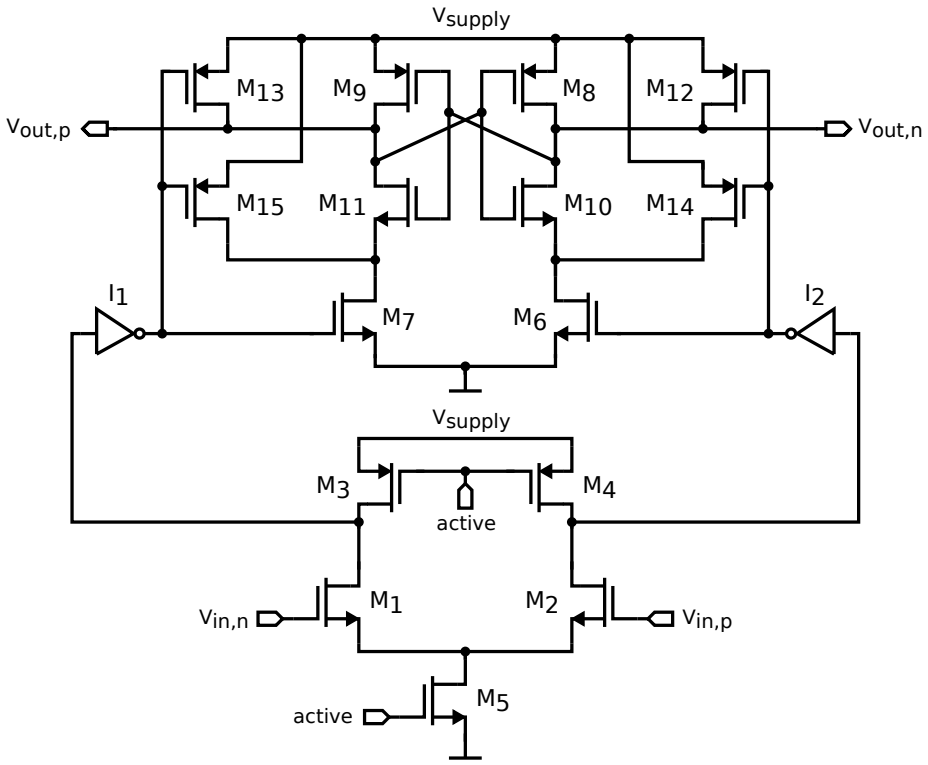

Figure 4. Schematic diagram of dynamic comparator. Adapted from [11]. ©CERN 2015. CC BY 3.0.

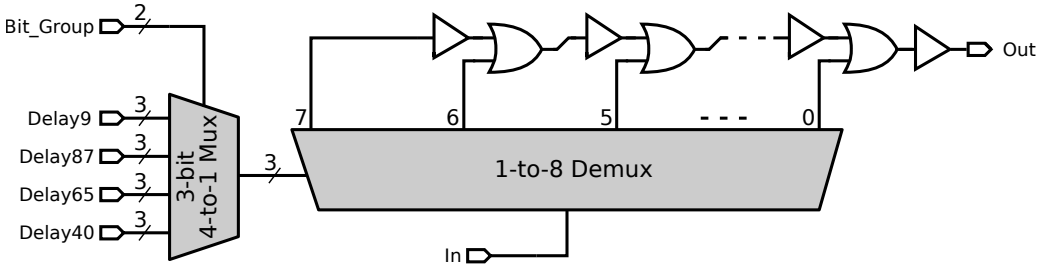

Figure 5. Simplified block diagram of the variable delay block.

the design of a multi-channel ASIC and significantly improves the power budget. Moreover, in the asynchronous design, the conversion time of consecutive bits may be individually controlled, which gives the ability to find the best trade-off between effective resolution and speed. After the input signal is sampled, an analogue-to-digital conversion is performed. The main sequence that is repeated during each bit conversion (except the last one) consists of the following steps:

1. activation of the comparator and awaiting its decision,
2. saving the result of the processed bit,
3. changing the configuration of the switches in the capacitive DAC,
4. waiting for DAC voltage settling before the next activation of the comparator.

For the last bit, only steps 1 and 2 are performed. Although steps 1, 2, and 3 should be executed as quickly as possible, the delay in step 4 is critical to achieve the required ADC resolution. The DAC should have enough time to settle the output voltage to the required precision, before the next activation of the comparator. The required settling time is the longest for the most significant bit and decreases for consecutive bits since the switched capacitance of the DAC lowers with the bit number. Thus, the more significant bits can borrow the conversion time from the least significant bits.

To obtain the requested resolution at the highest possible conversion rate, the delay before the comparator activation can be optimised separately for the comparison steps corresponding to successive bits. Therefore, in this design, a dedicated variable delay line was added for this purpose. The simplified block diagram of the implemented solution is shown in figure 5. The delay before the next comparator activation can be set to one of eight different values, with a unit delay step of about 175 ps. There are four internal 3-bit registers that allow one to control the delay value for four groups of processed bits. The first group contains only the most significant bit and is typically set to the longest delay. The second register controls the delay for bits 8–7, the third for bits 6–5, and the fourth for bits 4–0, which is usually the shortest. Delays should be experimentally tuned after ASIC fabrication for a given process corner to attain the fastest conversion while still maintaining the desired ADC resolution.

2.3 Configurable resolution

As already mentioned, the ADC resolution can be configured from 10 bits down to 5 bits. This is achieved by stopping the ADC after the required number of bits has been converted, and so

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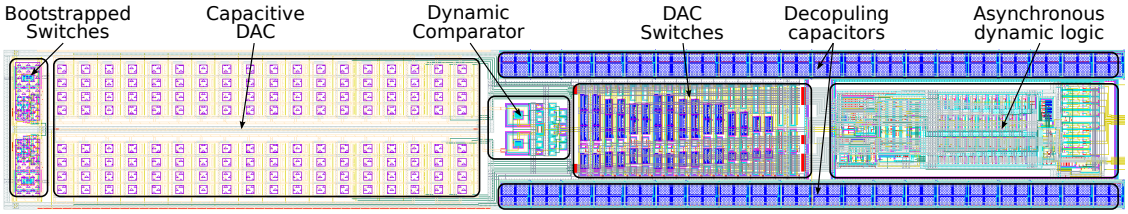

Figure 6. Layout of the ADC with 6-1C-3 DAC segmentation.

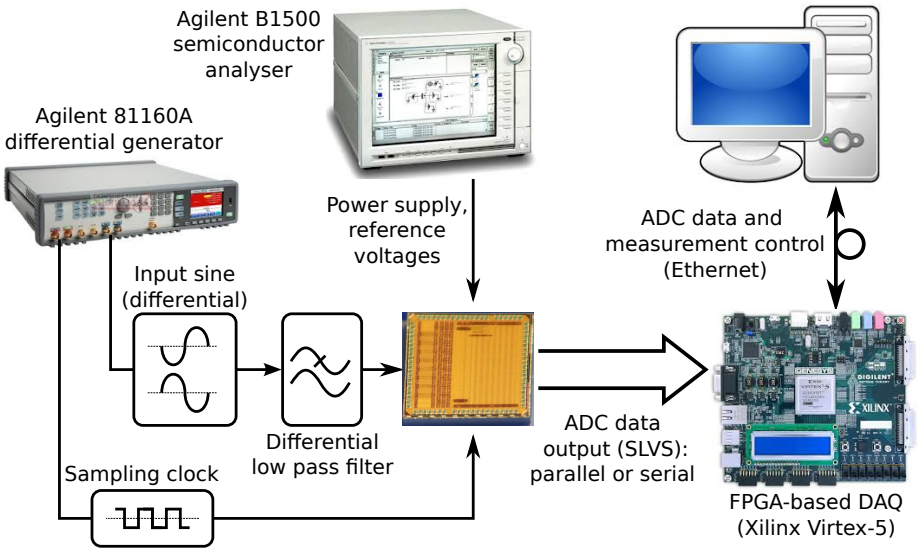

Figure 7. Setup for static and dynamic ADC measurements.

requires only a little modification of the SAR control logic. With such a simple implementation, the performance (power and speed) obtained for the resolution of 9 bits or less is not optimised as well as for 10 bits, but the ADC functionality is significantly extended and the trade-off between speed and resolution can be explored.

2.4 Layout

One of the key requirements for the ADC layout in multi-channel readout ASIC is a small pitch and area in general. In this design, the pitch for each ADC version was set to 80 µm. The layout of the default 6-1C-3 ADC version of size 560 µm × 80 µm is shown in figure 6. The blocks from left to right are: bootstrap switches, capacitive DACs, comparator, switches to reference voltages for subsequent DAC bits, and control logic. The 5-1C-4 and 6-2C-3 ADC versions have the same pitch and lengths 490 µm and 500 µm, respectively.

3 ADC measurements

The ADC measurements were performed using the set-up shown in figure 7. The Agilent B1500 semiconductor parameter analyser delivers supply, reference voltages, and input signals for static measurements, while the Agilent 81160A generates the sampling clock and input signal for dynamic

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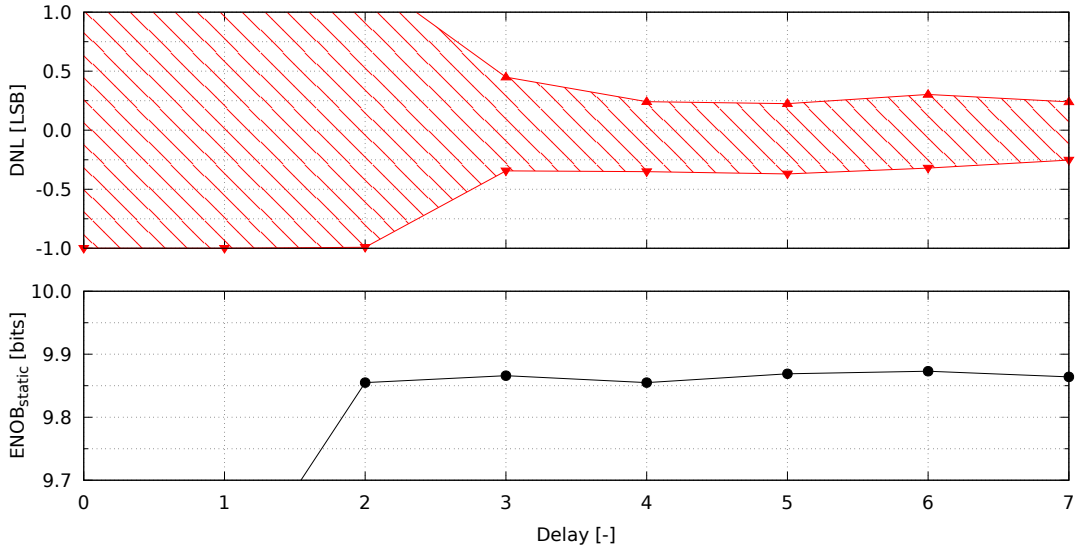

Figure 8. Example results of delay configuration procedure for bits 8–7 for DAC segmentation 6-1C-3. Maximum and minimum values of DNL (top) and $\mathrm{ENOB}_{\mathrm{static}}$ (bottom).

measurements. The data acquisition system was built on the Digilent Genesys evaluation board, which includes Xilinx Virtex-5 FPGA.

3.1 Static parameters and internal delays configuration

Static characterisation was performed based on the well-known histogram technique [18] with 10 MHz sampling frequency. In the first series of measurements, the static metrics Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) were measured for different settings of the ADC internal delays (DAC settling time). On the basis of INL results, one can calculate also a Static Effective Number of Bits ($\mathrm{ENOB}_{\mathrm{static}}$) [19]:

$$\mathrm{ENOB}_{\mathrm{static}} = \log_2\left(\frac{N}{\sqrt{12 \cdot \left[\frac{1}{12} + \frac{1}{N-2} \cdot \sum_{k=1}^{N-2} \mathrm{INL}_k^2\right]}}\right), \tag{3.1}$$

where N is the number of ADC codes. This initial characterisation was the basis for tuning the delays for each group of bits, to achieve the best ADC performance. The goal was to obtain the highest sampling rate while keeping the $\mathrm{ENOB}_{\mathrm{static}}$ and DNL at acceptable low levels. In this analysis, it was assumed that the $\mathrm{ENOB}_{\mathrm{static}}$ should not deteriorate by more than 5% compared to the values obtained using the maximum possible delay, and the maximum DNL error should stay within ±0.5 LSB. The example results obtained by scanning the delay value for bits 8–7 are shown in figure 8. The delay corresponding to code 3 is seen to be sufficient to achieve a DNL below 0.5 LSB, and this delay has been selected for bits 8–7. Increasing this delay further would degrade ADC speed without significantly improving resolution. Similar delay scans were performed for other groups of bits to tune the delays for these bits. The measurements carried out confirmed that

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the optimisation of internal delays was a very effective way to achieve the best speed-resolution ADC performance. All subsequent measurements for each ADC version, presented in this section, were performed using the optimal delay values obtained according to the discussed procedure.

The static performance for all ADC DAC segmentations, evaluated after internal delays configuration, is shown in figure 9 (DNL) and figure 10 (INL). The best results are obtained for the 6-1C-3

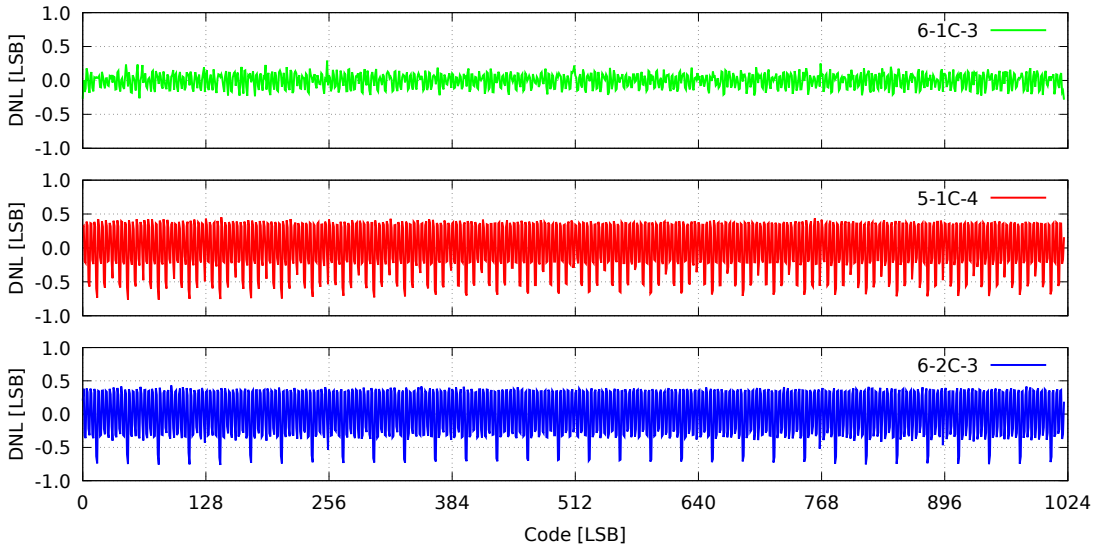

Figure 9. DNL for ADCs with 6-1C-3 (top), 5-1C-4 (middle), and 6-2C-3 (bottom) DACs segmentation, measured at 10 MHz sampling frequency.

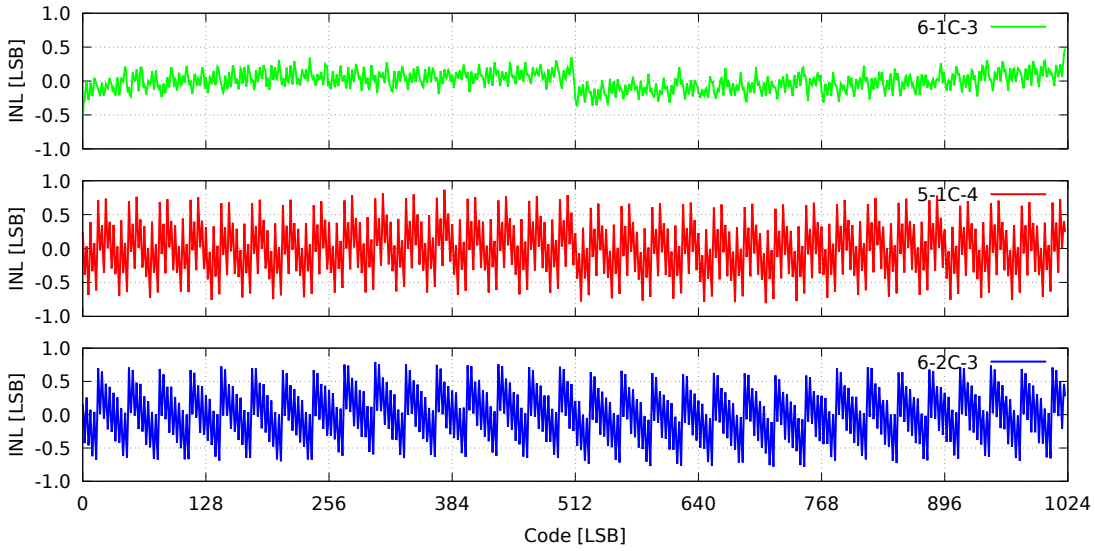

Figure 10. INL for ADCs with 6-1C-3 (top), 5-1C-4 (middle), and 6-2C-3 (bottom) DACs segmentation, measured at 10 MHz sampling frequency.

DAC segmentation showing absolute values of INL below 0.4 LSB and DNL below 0.3 LSB. The 5-1C-4 and 6-2C-3 DACs have also good linearity, but worse than the 6-1C-3 DAC, with maximum

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absolute values of INL and DNL errors of about 0.8 LSB. Since the ADC use asynchronous control logic, the linearity should not depend on the sampling frequency. This was verified for the 6-1C-3 DAC up to above 50 MHz.

3.2 Dynamic parameter measurements

Dynamic performance was evaluated for different sampling and input frequencies. In figure 11 (top) the standard ADC metrics: Signal-to-Non Harmonic Ratio (SNHR), Total Harmonic Distortion (THD), Spurious-Free Dynamic Range (SFDR), Signal-to-Noise-and-Distortion ratio (SINAD), and Effective Number of Bits (ENOB) [18] versus the sampling frequency, measured at low input signal frequency (0.1 Nyquist), are shown for the 6-1C-3 DAC segmentation. In figure 11 (bottom) the measured SINADs — and corresponding ENOBs — for three ADC versions, with different DAC segmentations, are compared. All of them work well with ENOB above 9 bits up to sampling frequencies over 45 MHz. By far the best results are obtained for the ADC with 6-1C-3 DAC segmentation, which keeps the ENOB at about 9.6 bits even above 50 MHz sampling.

The ADC dynamic metrics versus sampling frequency for high input signal frequency (up to Nyquist frequency) were measured only for the ADC version with the 6-1C-3 DAC segmentation and are shown in figure 12. Since high-frequency measurements at Nyquist input frequency are much more demanding in terms of setup preparation, only this configuration was tested. The ADC works well up to the sampling frequency of 55 MHz with the ENOB above 9 bits, while up to 50 MHz the ENOB does not fall below 9.45 bits.

3.3 Power consumption

As ultra-low power consumption is the main ADC demand for the considered applications, it was studied in detail in measurements. In figure 13 (left) main contributions to power consumption, namely, from the digital ADC part, from the analogue part, and from the reference voltage supply, are shown as a function of the sampling frequency, for the 6-1C-3 ADC version. As expected, the dissipated power of each contribution is proportional to the sampling frequency. It is clearly seen that the largest contribution comes from the digital part, about three times less from the analogue part, and the smallest contribution comes from the reference voltage supply. All ADC versions have similar power dissipation for each contribution, and therefore also the total power dissipation, as seen in figure 13 (right). Even at a sampling frequency of 55 MHz, the total power consumption is below 1 mW per channel.

3.4 The ADC figure of merit

A key parameter commonly used to show how efficiently the consumed ADC power is transformed into the ADC resolution and speed, is the Walden ADC Figure of Merit (FOM) [20]:

$$\mathrm{FOM} = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}} \cdot f_{\mathrm{sample}}}, \tag{3.2}$$

where ENOB is measured at the Nyquist frequency of the input signal. Low-frequency Figure of Merit ($\mathrm{FOM_{LF}}$) is also often used to show the power efficiency at lower input signal frequencies. The FOMs versus sampling frequency for different ADCs, calculated from the performed measurements, are shown in figure 14. As expected the ADC with 6-1C-3 DAC segmentation shows the best power

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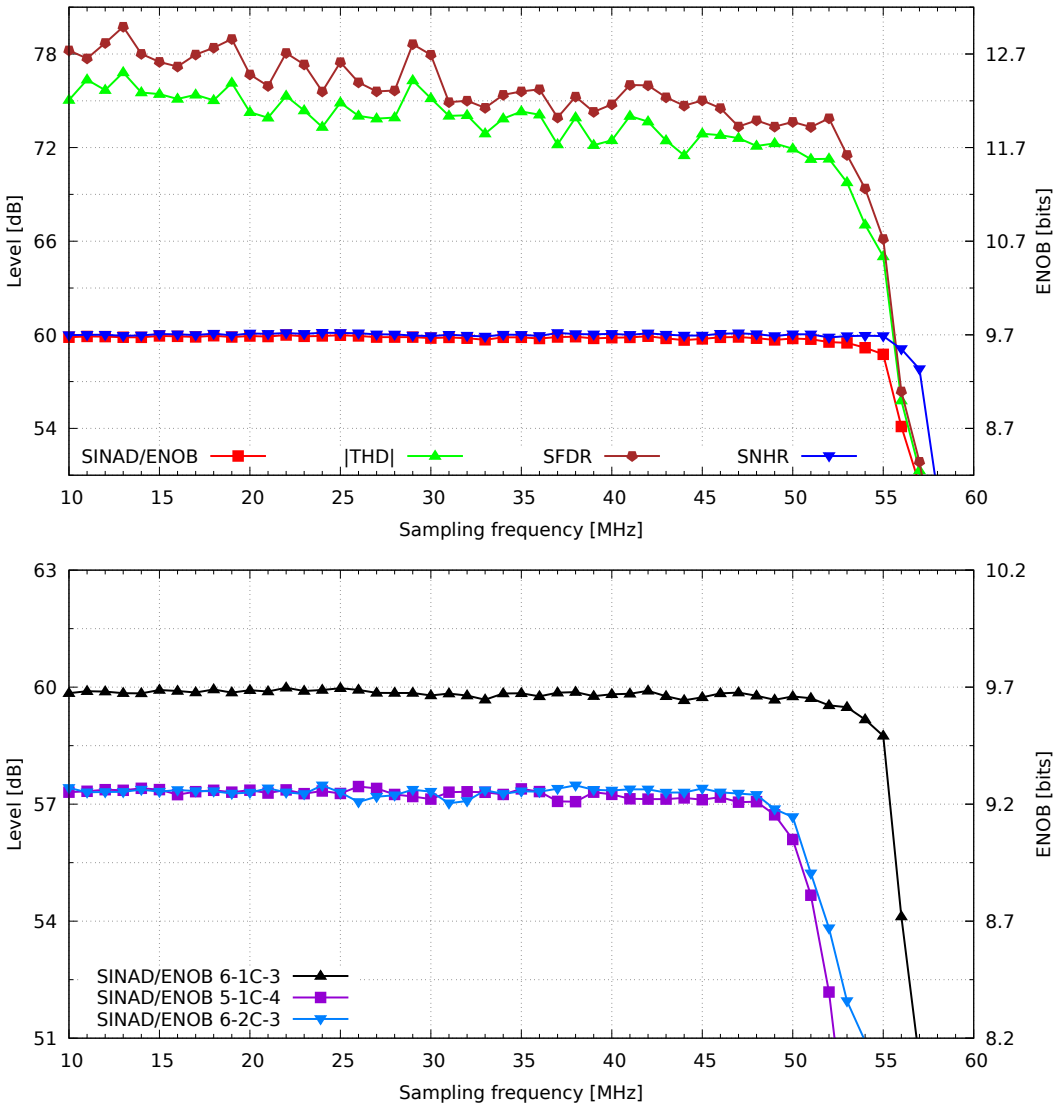

Figure 11. Dynamic metrics measured at 0.1 Nyquist input frequency, for ADCs with 6-1C-3 DAC segmentation (top). SINAD/ENOB for 6-1C-3, 5-1C-4, and 6-2C-3 DACs (bottom). At SINAD/ENOB curve SINAD is shown on the left axis and ENOB on the right axis.

efficiency, with $\mathrm{FOM_{LF}} \approx 21.5\,\mathrm{fJ/}\textit{conv.-step}$ and $\mathrm{FOM} = 24\,\mathrm{fJ/}\textit{conv.-step}$ at 50 MHz sampling frequency. The other two ADC versions have slightly worse, but still very good, $\mathrm{FOM_{LF}}$ of about $27\,\mathrm{fJ/}\textit{conv.-step}$ for sampling frequencies up to almost 50 MHz.

3.5 Configurable ADC resolution

The ADC performance was also evaluated for different settings of the ADC resolution. The standard set of static and dynamic parameter measurements was done for the resolution set from 5 to 10 bits. For these measurements, the delay settings optimised for 10-bit resolution were used. Here, only summary results presenting the ENOB versus sampling frequency, measured at low input signal frequency, are given in figure 15 (left) for the ADC with 6-1C-3 DAC segmentation. It is seen that

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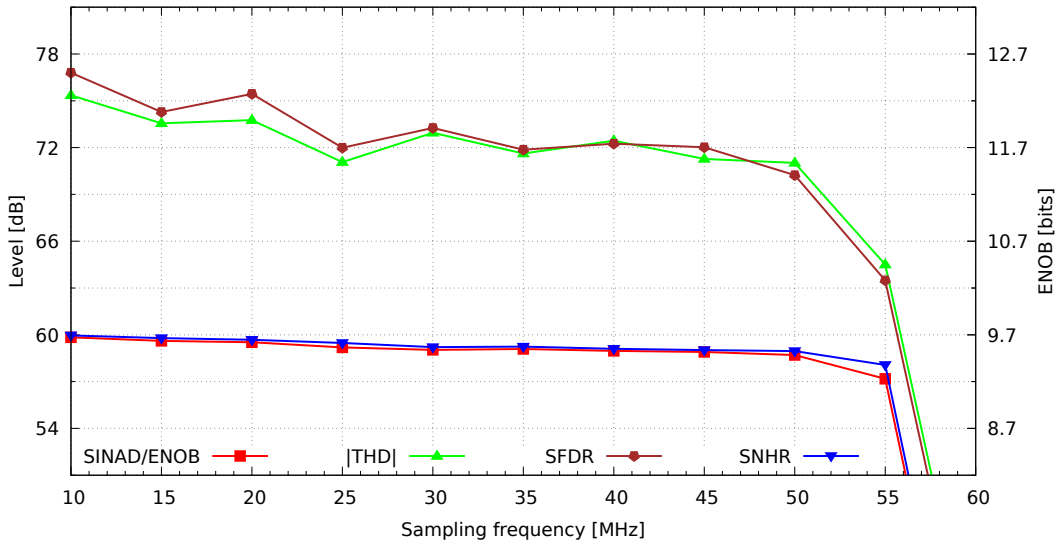

Figure 12. Dynamic metrics measured at Nyquist input frequency for 6-1C-3 ADC version.

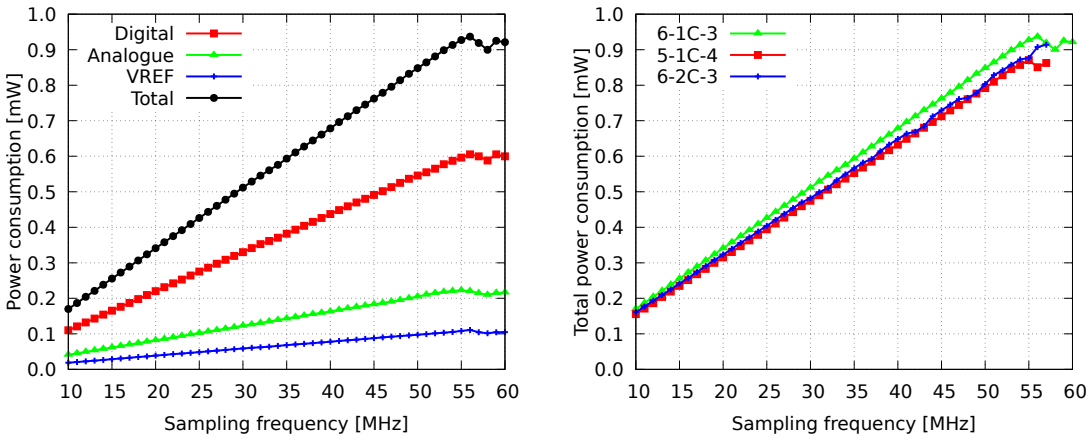

Figure 13. Different contributions to power consumption for ADC with 6-1C-3 DAC segmentation (left) and total power consumption for ADCs with 6-1C-3, 5-1C-4, and 6-2C-3 DACs (right).

the effective resolution approaches the nominal one for the resolution set to less than 10 bits. Apart from the expected ENOB improvement (compared to the resolution set) with decreasing number of bits, it can be seen that the maximum sampling frequency increases from 55 MHz at 10-bit to 95 MHz at 5-bit.

In figure 15 (right) main contributions to power consumption versus the resolution set are shown for the ADC with 6-1C-3 DAC, at 40 MHz sampling frequency. Power consumption decreases as the number of bits decreases. The decrease is less than potentially possible because the ADC design was optimised for 10 bits.

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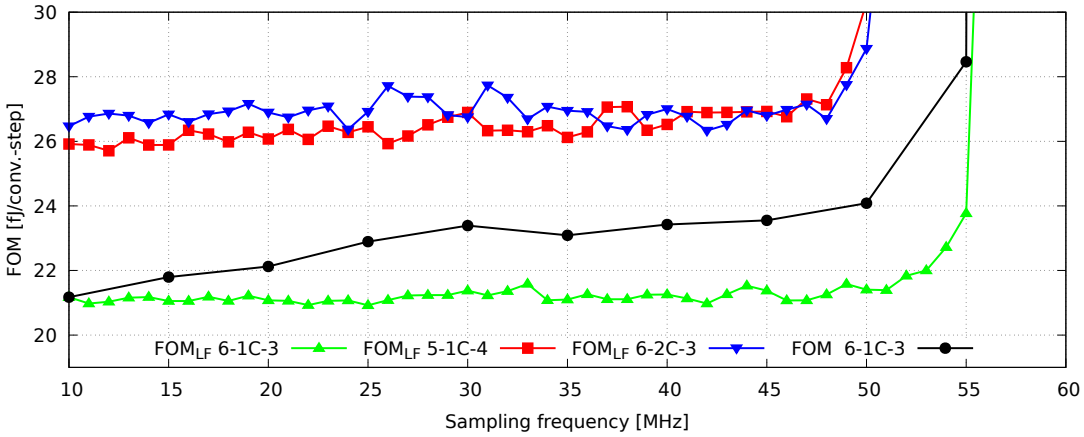

Figure 14. FOM$_{LF}$ for ADCs with 6-1C-3, 5-1C-4, and 6-2C-3 DACs and Walden FOM for ADC with 6-1C-3 DAC.

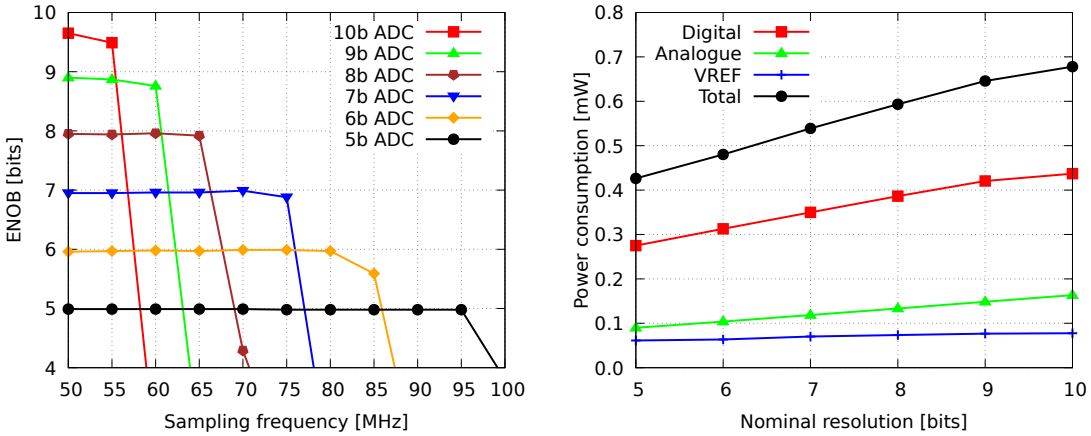

Figure 15. ENOB versus sampling frequency for different resolution settings (left) and power consumption contributions versus nominal resolution for 40 MHz sampling frequency (right); results for the ADC with 6-1C-3 DAC segmentation.

4 Comparison to the state of the art

In table 1 the key parameters of the best performing ADC version, with 6-1C-3 DAC segmentation, are compared with the State of the Art 10-bit ADCs designed in similar technologies and with similar specifications. One should be aware that better performance can be found for some ADCs designed in smaller feature size technologies, like CMOS 65 nm or less.

The designed ADC is very efficient in converting power to resolution and speed as its FOM is the lowest among published ADCs designed in CMOS 130 nm and 90 nm technologies. The size of the designed ADC is also among the smallest, second after the ADC designed in 90 nm [5]. As already said, for this work, it was no less important than the small size to achieve a very small pitch, allowing for easy multi-channel implementation.

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Table 1. Comparison with the State of the Art 10-bit ADCs.

	[11]	[21]	[4]	[22]	[15]	[23]	[5]	This work
Architecture	SAR	SAR	SAR	SAR	SAR	SAR	SAR	SAR
Technology [nm]	130	130	130	130	90	90	90	130
Supply [V]	1.2	1.2	1.2	1.2	1.2	1	1.2	1.2
Area [mm^2]	0.088	0.095	0.052	0.32	0.18	0.1	0.024	0.048
f_{sample} [MHz]	30	20	50	40	100	30	50	50
Power [μW][a]	660	620	826	550	3000	980	664	850
Max INL [LSB]	~0.5	0.47	1.36	1.55	0.86	1.32	0.45	0.4
Max DNL [LSB]	~0.5	0.34	0.91	0.78	0.79	0.88	0.36	0.3
$ENOB_{LF}$ [bits]	9.4	9.56	9.18	8.35	9.1	9.16	9.26	9.6
FOM_{LF} [fJ/*conv.-step*]	34	41	29	42	55	57	21.68	21.5
ENOB [bits]	9.25	9.32	$\lesssim$9[b]	8.11	8.6	8.68	~8.75[b]	9.45
FOM [fJ/*conv.-step*]	37	48	~32[b]	50	77	79	~30[b]	24

[a]In the quoted papers an external reference voltage is used. No internal reference buffers are used.

[b]Exact ENOB and FOM are not given at the Nyquist input frequency. A rough estimation from the plot is done.

5 Conclusion

In this article, the design and measurements of an ultra-low power 10-bit SAR ADC, ready for multi-channel integration, were presented. Performed measurements confirm very good functionality reflected in the ENOB of 9.45 bits, maximum sampling frequency 55 MHz, and excellent FOM of 24 fJ/*conv.-step* and FOM_{LF} of almost 21.5 fJ/*conv.-step* at 50 MHz sampling frequency. Ultra-low power and high sampling frequency, together with small pitch (and area), make the ADC a very attractive block for dedicated multi-channel readout systems in particle physics experiments. In fact, this ADC has been already implemented in the readout ASICs for the High Granularity Calorimeter [24] and for the MTD Barrel Timing layer [25] in the Upgraded CMS experiment at LHC.

Acknowledgments

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