Nuclear Instruments and Methods in Physics Research A 1057 (2023) 168787

Contents lists available at ScienceDirect

Nuclear Inst. and Methods in Physics Research, A

journal homepage: www.elsevier.com/locate/nima

MALTA monolithic pixel sensors in TowerJazz 180 nm technology

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ARTICLE INFO

Keywords:
Depleted Monolithic Active Pixel Sensors
Monolithic pixel detectors
MALTA

ABSTRACT

Depleted Monolithic Active Pixel Sensors are of highest interest at the HL-LHC and beyond for the replacement of the Pixel trackers in the outermost layers of experiments where the requirement on total area and cost effectiveness is much bigger. They aim to provide high granularity and low material budget over large surfaces with ease of integration. Our research focuses on MALTA, a radiation hard DMAPS with small collection electrode designed in TowerJazz 180 nm CMOS imaging technology and asynchronous read-out. Latest prototypes are radiation hard up to 2×10^{15} 1 MeV n_{eq}/cm^2 with a time resolution better than 2 ns.

1. Introduction

The MALTA Pixel (Fig. 1) has a pitch of 36.4 μm^2 that allows for good spatial resolution, a small collection electrode size (3 μm) that provides minimal capacitance (<5 fF), and enough spacing to the electronics (3.4 μm) to avoid cross-talk. The read-out of the pixel is asynchronous, without any clock distribution over the matrix [1], which reduces the power consumption per pixel below 1 μW. The total power consumption per area is 10 mW/cm^2 for the digital domain and 70 mW/cm^2 for the analog domain.

MALTA prototypes designed in TowerJazz 180 nm CMOS imaging technology were produced on high resistivity 25 μm and 30 μm thick epitaxial silicon. Before irradiation these samples reach full depletion around 10 V, have a high signal to noise ratio (~20), where the expected energy deposition of a MIP is 1500 electrons, and the noise is lower than a few hundred electrons. The implant design is modified to include an additional low dose n- blanket layer under the deep p-well to improve depletion as shown in Fig. 2, which is referred to as the standard modified process [2]. Additional process modifications at the pixel edges were introduced to increase the lateral field configuration and reduce charge collection time based on TCAD simulations [3]. This is either a 4 μm gap in the n- blanket (aka NGAP), or the addition of a 5 μm wide extra-deep p-well (aka EDPW).

Additionally, MALTA prototypes have been processed on high resistivity Czochralski substrates (3–4 kΩ cm), that can be biased up to 50 V leading to deeper depletion levels, and increased charge collection. All implant designs (standard, NGAP, and EDPW) are available on Cz substrates [4].

2. MALTA prototypes

2.1. MALTA

The first MALTA submission in 2018 was a 22 × 20 mm^2 full size demonstrator with 512 × 512 matrix arranged in 8 different sectors with slight modifications in the reset mechanism, electrode size, spacing to the electronics, and p-well cut-out. This submission featured only the standard modified process. As reported in [5], it suffered from efficiency degradation at the pixel edges already after 10^{14} 1 MeV n_{eq}/cm^2 irradiation.

2.2. Mini-MALTA

The Mini-MALTA prototype submitted in 2019 is a 5 × 1.7 mm^2 demonstrator with a matrix of 64 × 16 pixels, and a single pixel

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https://doi.org/10.1016/j.nima.2023.168787
Received 20 November 2021; Received in revised form 13 May 2022; Accepted 11 October 2023
Available online 16 October 2023

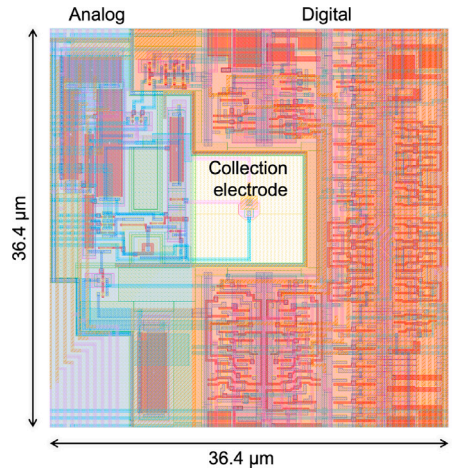

Fig. 1. MALTA Pixel cell.

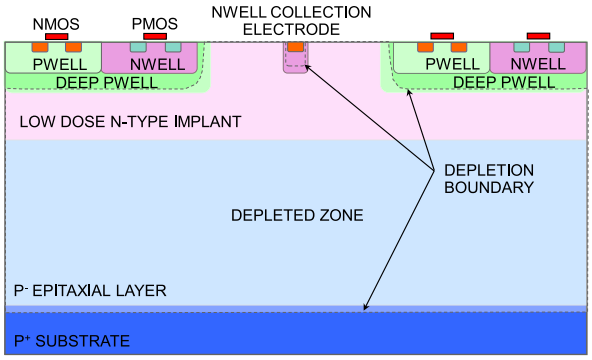

Fig. 2. Cross section of the standard modified process implementing a small electrode pixel as used for the MALTA prototypes.

design compatible with sector 3 of the original MALTA submission. It featured the three different implant designs (standard, NGAP, EDPW) and two different sizes (same as MALTA and 2.7 times larger) for the low frequency feedback NMOS transistor in order to address the radiation hardness shortcomings and the large RTS noise observed on the previous prototype. Additionally, this design included an on-chip data synchronization unit and a single output line at 40 MHz. This prototype was extensively tested with beam tests in ELSA [6], and Diamond [7], where radiation hardness of the modified processes (NGAP and EDPW) with enlarged transistors could be demonstrated up to 10^{15} 1 MeV n_{eq}/cm^2. Furthermore, enlarged transistors allowed to reach lower thresholds (150 electrons), and the additional process modifications had slightly higher efficiency. No noticeable difference was observed in performance between 25 µm and 30 µm thick epitaxial samples.

2.3. MALTA on Czochralski substrate

By the second half of 2019, MALTA prototypes with enlarged feedback NMOS transistor tested in Mini-MALTA and revised power distribution in the periphery were manufactured on epitaxial and high-resistivity Czochralski (Cz) substrates. Extensive tests were carried out at DESY [4]. As observed on the Mini-MALTA design, the corner efficiency after 1×10^{15} 1 MeV n_{eq}/cm^2 was fully recovered with Czochralski samples with extra process modifications (NGAP and EDPW) as shown in Fig. 3. Additionally, it was observed that before irradiation the efficiency of epitaxial samples decreases with bias voltage beyond 12 V due to the increasing leakage current as opposed to

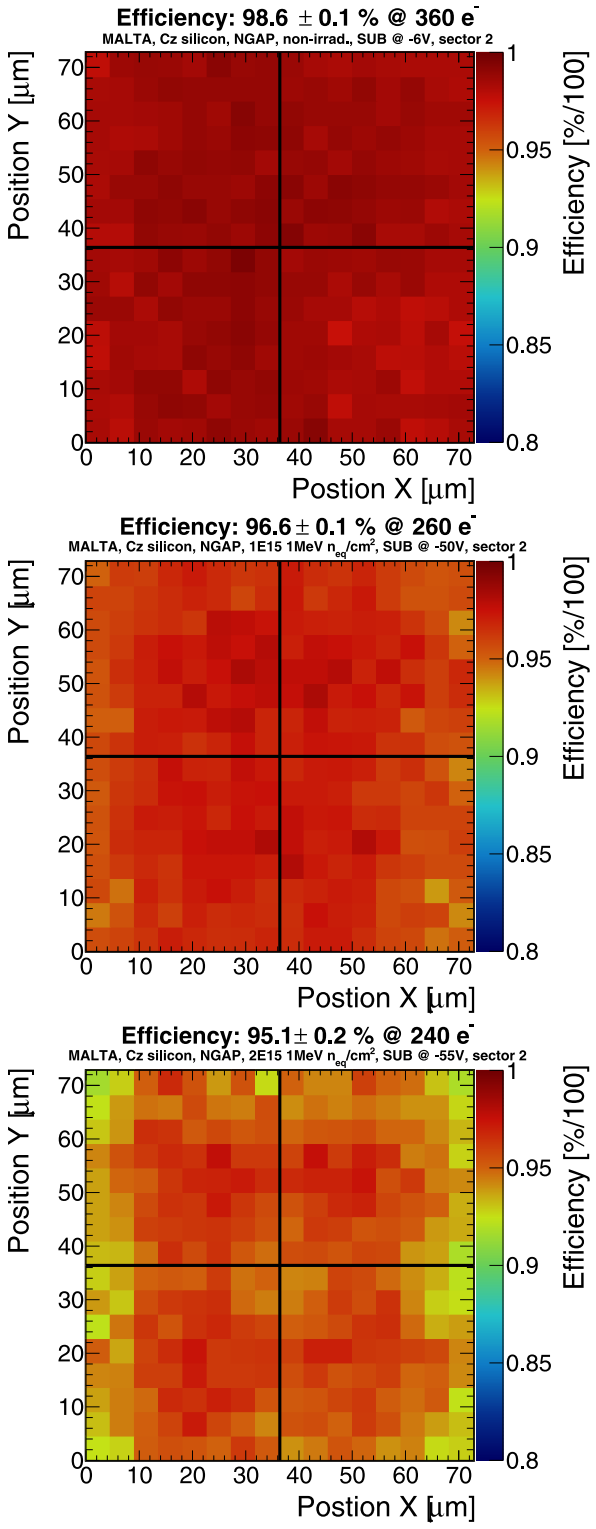

Fig. 3. In-pixel efficiency of MALTA samples on Czochralski silicon with the n-gap modification to the planar n-layer at low threshold configuration before irradiation (top), after 1×10^{15} (center), and at 2×10^{15} 1 MeV n_{eq}/cm^2 (bottom).

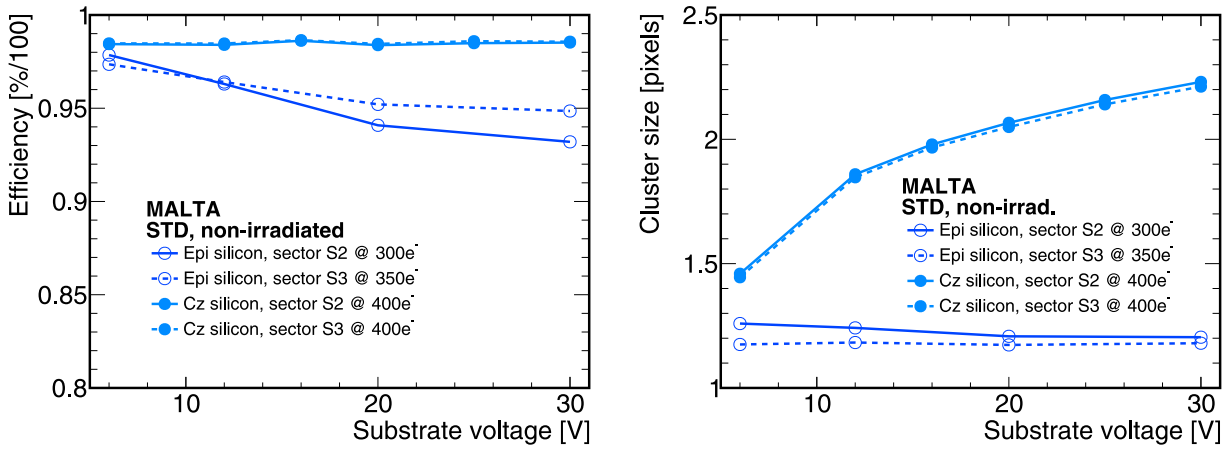

Fig. 4. Efficiency (left) and cluster size (right) for non-irradiated MALTA samples manufactured on epitaxial (Epi) and Czochralski (Cz) silicon with the standard (STD) modification versus substrate bias. Indicated are the respective thresholds, and the sector of the Pixel matrix. The sectors differ in the extension of the deep p-well, being medium for Sector 2 and maximum for Sector 3.

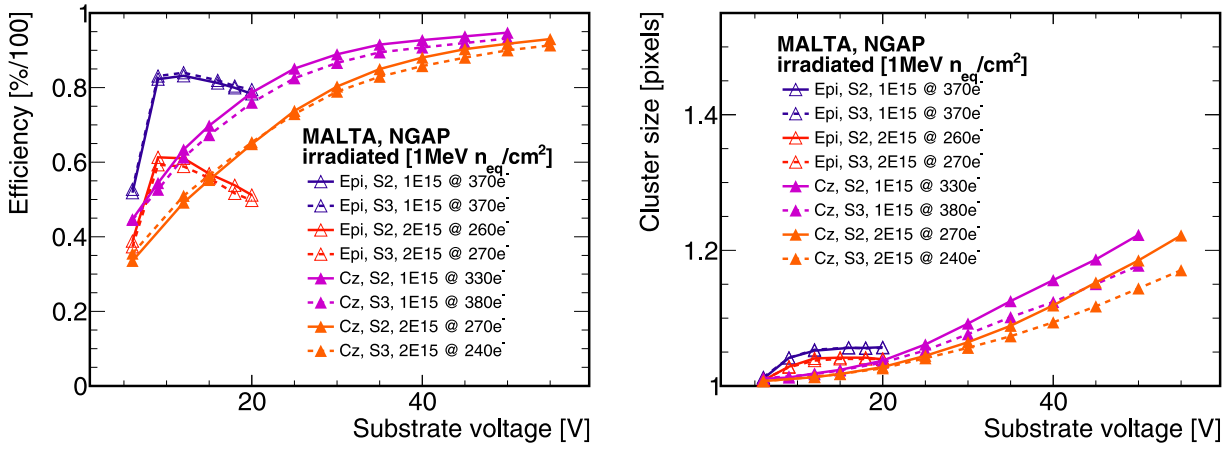

Fig. 5. Efficiency (left) and cluster size (right) for MALTA samples irradiated to 1×10^{15} 1 MeV n_{eq}/cm^2 and 2×10^{15} 1 MeV n_{eq}/cm^2 manufactured on epitaxial (Epi) and Czochralski (Cz) silicon with the n-gap (NGAP) modification versus substrate bias. Indicated are the respective thresholds, and the sector of the Pixel matrix. The sectors differ in the extension of the deep p-well, being medium for Sector 2 and maximum for Sector 3.

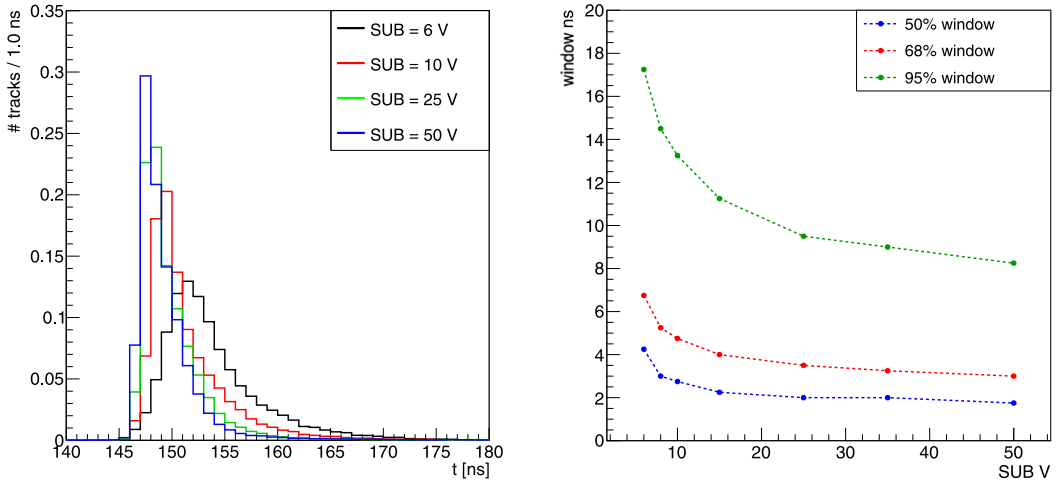

Fig. 6. Difference in time (left) and integral of the difference in time (right) of the fastest hit of the cluster (matched with the track in the DUT) and the time of the hit in the scintillator for a non-irradiated MALTA sample on Czochralski silicon with standard process versus substrate bias.

Czochralski sensors where it remains constant up to 30 V as shown in Fig. 4, and that the cluster size on Czochralski samples reaches 2.2 at 30 V, as opposed to epitaxial samples where it remains constant. After irradiation, epitaxial samples show a maximum cluster size of 1.05 and reach maximum efficiency at 12 V, whereas Czochralski sensors reach cluster sizes of 1.2 and reach full efficiency (>95%) at 50 V as shown in Fig. 5. Time resolution on the epitaxial silicon sample is 2.60 ± 0.05 ns at 6 V, while the time resolution on the Czochralski sample is compatible with 1.7 ± 0.1 ns between 10 V and 30 V [8]. Faster signal and higher amplitude at large substrate voltages reduce time-walk and narrow the time difference distribution between trigger scintillator and non-irradiated MALTA Czochralski STD sample. 50% of the hits arrive within 2 ns at a substrate voltage above 15 V as shown in Fig. 6.

2.4. Mini-MALTA split 7

Mini-MALTA was reprocessed in 2020 on epitaxial substrate with a modification to the front-end circuit introducing a new transistor in series with the input node that increases the output impedance of the amplifier leading to a higher gain. This design is referred to as cascoded front-end, and decouples the feedback loop transistor from the output node, effectively decoupling the size of this transistor from the threshold settings as shown in Fig. 7, where the measured threshold is plotted as a function of the IDB DAC that directly controls the discriminator voltage (threshold), for different values of the ITHR DAC that controls the speed of the return to the baseline of the signal. The higher the IDB, the higher the threshold. The higher the ITHR the faster the return to baseline. In the standard front-end, the pixels with larger size low frequency feedback NMOS transistor (L) have lower threshold than the ones with smaller size (R). In the cascoded front-end, the size of the low frequency feedback NMOS transistor is not relevant, and the threshold can be set to much lower values. This front-end design was selected for the front-end of MALTA2.

2.5. MALTA2

MALTA2 was submitted by the end of 2020 as a half size demonstrator, 20 × 10 mm^2 in size, with 224 × 512 MALTA pixels. It is based on a single pixel design with 2 μm collection electrode size, a 4 μm spacing to the electronics, and the cascoded front-end from Mini-MALTA split 7, with an even larger size of the transistor responsible for the RTS noise, and improved jitter in time propagation down the column. Thus, the pixel matrix is no longer divided into different sectors. The standard deviation of the noise distribution at a threshold of 350 electrons of MALTA2 is almost half of the one of MALTA (2.0 vs 3.5) as it is less affected by RTS noise. Threshold dispersion is similar to the original MALTA (~10% of the mean).

MALTA2 was extensively tested with particle beams at CERN SPS collider during 2021 using a custom MALTA telescope composed of 6 reference planes and up to two devices under test. The MALTA planes are used both for triggering, through a combination of their reference signals, and for track reconstruction. A scintillator was added for better time reference. This allows to test radiation hardness and measure cluster sizes.

3. Module studies

MALTA includes 40 CMOS pads on each side which can be used for chip-to-chip data transmission with 1 ns wide pulses as well as power transmission. This allows for larger sensing surfaces to be designed and the reduction of the services necessary on a module made out of multiple MALTA sensors. Silicon bridges have been studied to interconnect two MALTA samples. The bridge is attached to the chips with an-isotropic conductive film glue that requires 1 kg of pressure and cures at 150 C for 10 s, along with 10 μm positioning precision on the pads. First tests are promising, and structures with up to four MALTA sensors are being developed [9].

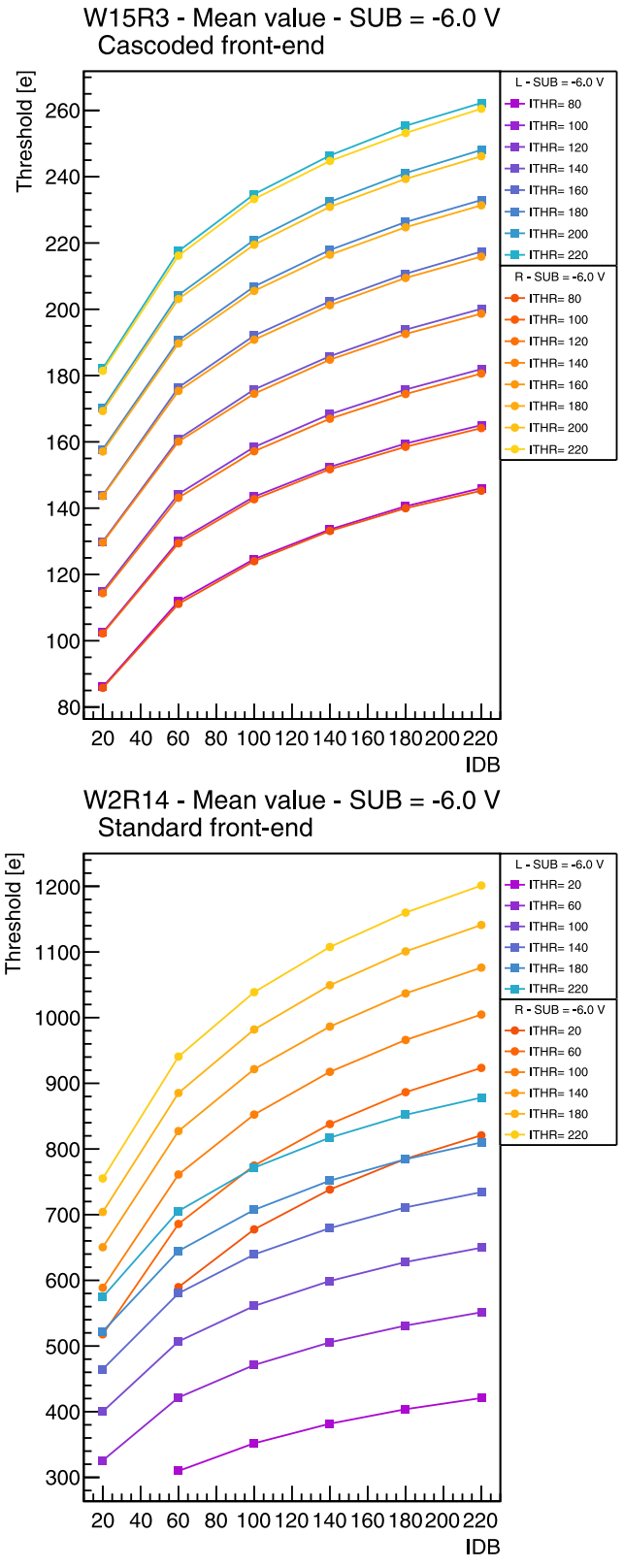

Fig. 7. Mean threshold of the Mini-MALTA pixel detector with the cascoded (top) and standard (non-cascoded) (bottom) front-end as a function of the IDB DAC that controls the threshold setting, for different values of the ITHR DAC that controls the speed of the return to the baseline. Depicted are the values for the left (L) side of the chip with larger size feedback loop transistor, and the values for the right (R) side of the chip with standard size transistor.

4. Conclusions and outlook

MALTA is an interesting candidate for future high energy physics experiments due to its relative small pixel pitch (36.4 μm^2), low power consumption (80 mW/cm^2), radiation hardness up to 1×10^{15} 1 MeV n_{eq}/cm^2 (NGAP and EDPW process modifications), and large cluster sizes (Czochralski substrates).

MALTA 3, under design at the time of writing, will merge the latest process modifications and a front-end design with improved resolution and asynchronous read-out architecture. It will have on-chip data synchronization with 1 ns time resolution and be designed with full reticle size to study integration options with existing LHC trackers where the focus is radiation hardness and high granularity.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement number 101004761 (AIDAinnova), and number 654168 (AIDA-2020). Furthermore it has been supported by the Marie Sklodowska-Curie Innovative Training Network of the European Commission Horizon 2020 Programme under contract number 675587 (STREAM). The measurements leading to these results have been performed at the TestBeam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF). Measurements leading to these results have been performed at the E3 beam-line at the electron accelerator ELSA operated by the university of Bonn in Nordrhein-Westfalen, Germany.

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