Journal of Instrumentation

PAPER • **OPEN ACCESS**

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To cite this article: C. Borca on behalf of the CMS collaboration 2024 *JINST* **19** C03024

Published by IOP Publishing for Sissa Medialab

Received: *November 20, 2023*
Accepted: *December 4, 2023*
Published: *March 12, 2024*

16TH Topical Seminar on Innovative Particle and Radiation Detectors
Siena, Italy
25–29 September 2023

Test and performance of the CMS ECAL barrel data conversion and digital processing ASIC for HL-LHC

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Abstract: In preparation for the high luminosity upgrade of the Large Hadron Collider, a new data conversion and digital processing ASIC, called LiTE-DTU, was designed. Implemented in a 65 nm CMOS technology, the LiTE-DTU features two 12-bit 160 MS s^{-1} successive approximation register time-interleaved ADCs, a data processing unit and enables efficient data transmission at 1.28 Gbps. The LiTE-DTU has undergone extensive testing in both laboratory and beam tests, demonstrating excellent performance in the pre-production version, showing the production readiness of the design. The results of this comprehensive series of tests will be presented.

Keywords: Data acquisition circuits; Digital electronic circuits; Front-end electronics for detector readout; Calorimeters

https://doi.org/10.1088/1748-0221/19/03/C03024

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1 Overview of the HL-LHC upgrade of the ECAL barrel

The Compact Muon Solenoid (CMS) [1] is a general purpose detector designed to investigate a broad spectrum of fundamental physics phenomena at the Large Hadron Collider (LHC). An essential element of the CMS is its electromagnetic calorimeter (ECAL), a precision detector that measures the energy of photons and electrons with high accuracy. It is composed of 75,848 lead tungstate scintillating crystals, organized into a central barrel section (EB) and two endcaps (EEs). Specifically, the focus of this discussion will be on the EB, which consists of 61,200 crystals organized into 2,448 readout units. These units feature 5×5 arrays of crystals, each crystal read by a pair of avalanche photo-diodes (APDs).

The forthcoming transition of the LHC to the High-Luminosity LHC (HL-LHC) [2], scheduled to commence collisions in 2029, will amplify the luminosity by a factor of 5, reaching approximately $5\times10^{-34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. Consequently, there will be an increase in the number of proton-proton interactions per bunch crossing (pile-up), rising from 60 to 200, creating a more challenging radiation environment.

Regarding the EB specifically, the consequences will be twofold. Firstly, concerning the degradation caused by the radiation damage of APDs and crystals, which will not be replaced. Indeed, in the former the leakage current will increase with ageing, the latter instead will loose transparency. Secondly, the elevated pile-up will pose challenges in distinguishing authentic scintillation signals from spikes, aberrant signals resulting from direct ionization of APDs, particularly prevalent at higher energies. These two kinds of signals differ only by a slightly different time development. For these reasons, mitigation strategies and a significant upgrade of the ECAL are necessary [3]. In the EEs the radiation damage is unsustainable and a newly designed detector, the High-Granularity Calorimeter (HGCAL), will be installed in replacement. To minimize the radiation-induced damage to the APDs, the operating temperature will be lowered from 18° to 9° and the old crystals will stay in place since their radiation damage is relatively limited. To address pileup challenges and to allow an effective spike discrimination, a new and faster front-end electronics has been developed. Further elaboration on this will be provided in detail in section 2.

Furthermore, in the upgraded CMS the trigger requirements will be different and more demanding: the latency of Level-1 trigger is set to rise from approximately 4 µs to 12.5 µs accompanied by an increase in the rate to 750 kHz, compared to the current 150 kHz. This transition is one of the main motivating factors for a complete redesign of the readout chain, front-end and back-end. Therefore, a new and more powerful back-end board, the Barrel Calorimeter Processor (BCP) [4], was also designed for this purpose. A trigger-less front-end approach was adopted, completely moving the

trigger primitive generation off-detector, where the BCP will be able to handle the information for individual crystals, in contrast to the existing granularity of a single 5×5 unit.

2 The new front-end and the LiTE-DTU ASIC

The geometry of the front-end electronics will remain unchanged from the current configuration. This setup, illustrated in figure 1, consists of five very-front-end (VFE) boards, each equipped with 5 channels, and a low voltage regulator. These boards are connected to a motherboard on the crystal side. On the other end, they interface with the front-end (FE) board, where 4 low-power gigabit transceiver (lpGBT) ASICs [5] gather data from the 25 channels, serialize it at 10 Gbit s^{-1} and transmit it off-detector using the versatile link plus (VTRx+) optical transceiver [6].

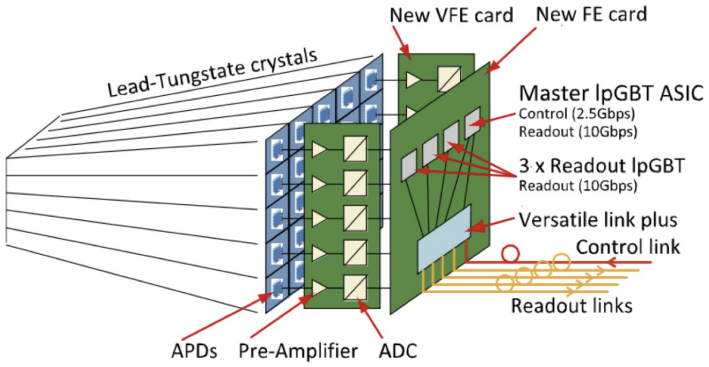

Figure 1. The upgraded readout unit of the ECAL barrel.

The new VFE cards will feature two new ASICs: one designed to amplify signals from the APDs, and a second tasked with analog-to-digital conversion, data serialization and transmission, incorporating minimal digital processing. Their position in a scheme focusing on the single channel can be seen in figure 2.

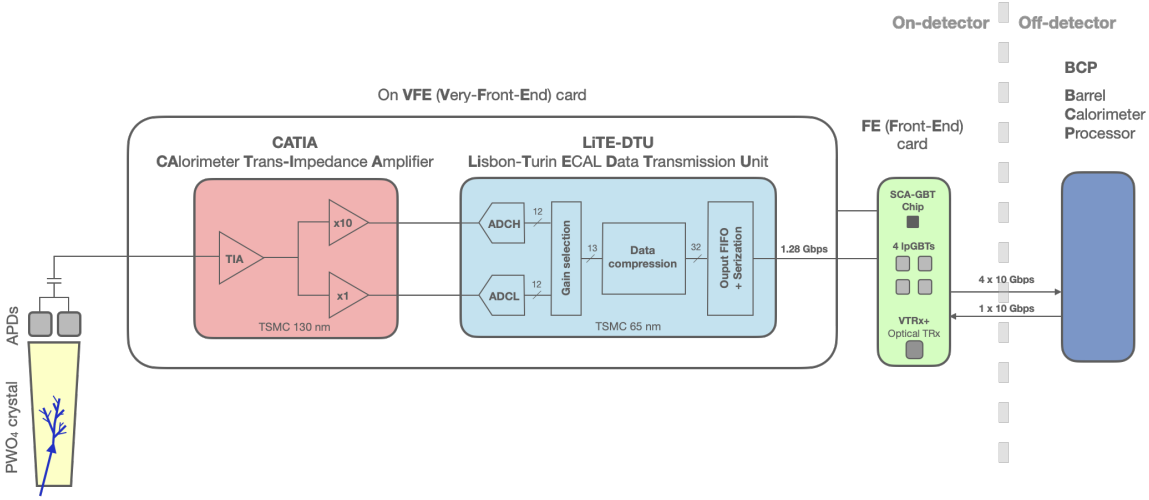

Figure 2. The upgraded readout of the ECAL barrel for HL-LHC focusing on a single channel.

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The first component, the calorimeter trans-impedance amplifier (CATIA) [7] is a trans-impedance amplifier built with a 35 MHz bandwidth in a 130 nm CMOS process. Its design is focused on maintaining the distinctive features, particularly the faster rising time and shorter duration, that differentiate actual scintillation signals from APD spikes. Employing a regulated cascode input stage, it is followed by two voltage amplification stages operating in parallel, providing a gain of 1 and 10, respectively. This configuration ensures optimal energy reconstruction for signals ranging from 50 MeV up to 2 TeV. Its radiation hardness has been tested for doses up to 10 Mrad.

The second ASIC, named Lisbon-Turin ECAL data transmission unit (LiTE-DTU) [8], incorporates two 12-bit analog-to-digital converters (ADCs) operating at 160 MS s^{-1} to digitize signals from the two CATIA output stages. These two ADCs consist of identical custom IP cores designed by the Portuguese company Adesto (now Renesas). They employ a successive approximation register (SAR) architecture with time interleaving, which means that each ADC comprises two cores working together at 80 MS s^{-1} with a phase difference of 180°.

The samples from the two ADCs undergo a sequence of digital processing steps, beginning with the digital subtraction of a configurable baseline value. Following this step, a look-ahead algorithm allows the selection of the highest non-saturated sample as part of the gain selection mechanism. This approach enables the acquisition of a sample window of configurable length from the low gain ADC around a saturated sample when the highest gain is saturated. This strategy ensures the selection of the optimal sample and the entire pulse shape to which it belongs. An additional bit is appended to the sample to indicate the chosen gain.

The data rate of raw output from the LiTE-DTU, following the sample selection logic, stands at 2.08 Gbps, whereas the available bandwidth towards the lpGBT is limited to 1.28 Gbps. Consequently, data compression becomes necessary. The devised compression algorithm is a simplified version of Huffman encoding [9], exploiting the statistical properties of the expected signals. In fact, given that the majority of signals will fall within the CATIA baseline, samples (in gain 10) that can be represented in less than 6 bits are truncated to 6-bit samples without losing information. Essentially, this involves eliminating most significant bits that are 0. This compression technique reduces the bandwidth to 1.08 Gbps, fitting the specified requirements.

The compressed data, organized into 32-bit data words, is subsequently placed in a 16-cell output FIFO. This FIFO is essential to counterbalance data rate fluctuations caused by the compression algorithm. The data words are then serialized at a rate of 1.28 Gbps. At intervals of every 50 words, a frame delimiter word is transmitted, serving as a checkpoint for data integrity. This delimiter word includes the cyclic redundancy check, the number of samples, and a frame word counter.

A phase-locked loop (PLL) circuit, taken from the lpGBT design, generates the 1.28 GHz clock required by the ADCs and serializer, starting from the primary 160 MHz clock via clock multiplication.

The LiTE-DTU operation is controlled by a series of fast commands transmitted through a 160 Mbps serial link. These commands include resets for the single blocks, calibration commands and synchronisation commands. Additionally, the LiTE-DTU can be programmed through an I^2C interface (slow control), facilitating the configuration of various operational parameters.

A detailed overview of the performance and tests conducted on the LiTE-DTU will be given in the section 3.

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3 LiTE-DTU performance: on-bench tests, radiation tolerance and system tests

To validate its performance, the LiTE-DTU underwent thorough testing, both standalone in a dedicated laboratory setting and under beam conditions, assessing its radiation tolerance. Furthermore, it was integrated into the new VFE cards for system tests and beam tests.

The on-bench test setup, arranged in the laboratories of the physics institute of Torino, comprises a custom test board designed to accommodate the device under test, with an external signal generator supplying input stimuli and clock. The transmission of fast and slow controls, as well as the data acquisition, is managed by an FPGA (Xilinx Kintex UltraScale KU040 Development Board), which communicates with the computer through a UDP-based Ethernet link. A Python-based custom test interface enables the initiation of a complete automated sequence or the execution of individual scripts for debugging purposes. Two types of test boards are employed: the first is utilized for assessing the performance of the ASIC embedded ADCs, with the package directly soldered onto the PCB. In contrast, the second board is equipped with a zero insertion force (ZIF) socket, that allows automated testing to validate a large number of devices.

To evaluate the performance of the ADCs, the effective number of bits (ENOB) was assessed using the standard methodology outlined in the literature [10]. High purity sine waves were injected into the input line at various frequencies, as illustrated in figure 3. An ENOB of 9.4 was measured at an input frequency of 50 MHz for both ADCs. This value, achieved using the internal PLL clock, is slightly below the design target of 10.2. Further measurements employing an external clock source and yielding an ENOB of 10.2 suggest that this degradation is attributed to the jitter in the PLL clock. Even if the overall performance of the LiTE-DTU already fits the system requirements, efforts have been made to improve the PLL clock jitter for the new and final version of the ASIC.

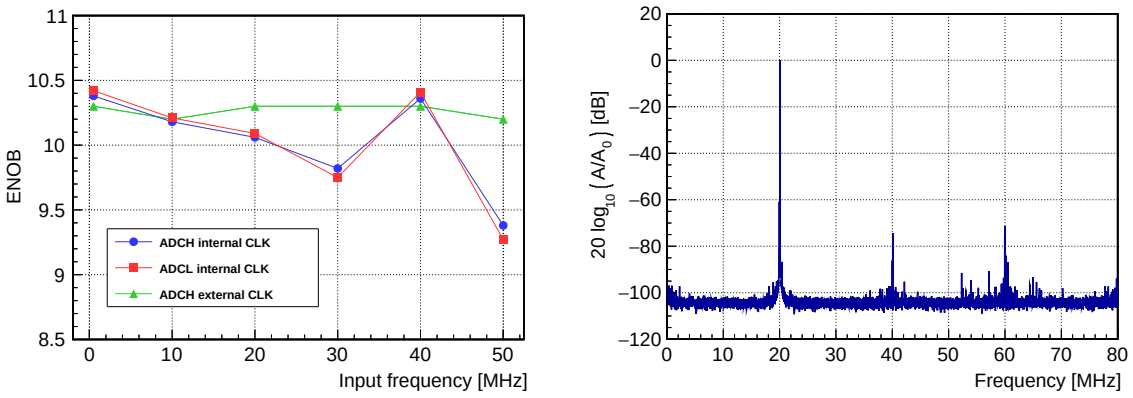

Figure 3. On the left the effective number of bits (ENOB) evaluated for the two ADCs with internal and external clock. On the right an example fast Fourier transform of the digitized signal with a 20 MHz input sine wave and internal clock used in the procedure to calculate it. The enhancement in the ENOB observed at 40 MHz is attributed to the alignment of the main harmonic of the signal and the spurious harmonics caused by the time-interleaved architecture.

In early 2022, the 600 dies pre-production batch of the ASIC (LiTE-DTU v2.0) underwent comprehensive testing in the laboratory, employing an automated test procedure. This procedure consisted of a supply current check, PLL lock scan, bit and data alignment, ADCs calibration and validation using ENOB measurements. Additionally, in the test sequence test-pulse injection for both

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gain ×1 and gain ×10 inputs was included to verify the correct encoding of the data and the gain selection mechanism. The batch, utilizing conservative rejection-acceptance criteria, achieved a yield of almost 97%. An improved version of the same test software has been provided to the company responsible for mass-production testing. The verification engineers at the company are currently using it for preliminary testing, and the integration with their system is well underway.

Specific tests were also conducted to evaluate the LiTE-DTU tolerance to total ionizing dose (TID) at the INFN Padova X-ray irradiation facility using 10 keV X-rays. A cumulative dose of 50 kGy, approximately 2.5 times higher than the expected dose at the end of HL-LHC operation, was delivered. No variations were observed in the performance after the irradiation.

The LiTE-DTU was also tested for robustness against single-event upsets (SEU) at the Louvain-la-Neuve Cyclotron Resource Centre (CRC) Heavy Ion Facility (HIF) and at the Laboratori Nazionali di Legnaro SIRAD irradiation facility. Various heavy ions with a linear energy transfer (LET) ranging from 6.37 to 38.6 MeV cm^{-2} mg^{-1} were utilized. The occurrence of bit flips was consistently monitored in both the I^{2}C registers of all devices and in the data path, where the input was deliberately set to a known value. The experimental data, reported in figure 4, were utilized to estimate the SEU cross section for protons through the application of a Weibull function fit as described in [11]. The extrapolated cross section is approximately 6.8×10^{-18} cm^2 bit^{-1} for the I^{2}C registers and 9.4×10^{-13} cm^2 chip^{-1} for the data path. Notably, the ADC data registers are not SEU-protected, as they are considered less critical. This translates into approximately 6 I^{2}C errors and 600 data errors per hour for the entire EB. This is a completely acceptable performance for the conditions in the HL-LHC.

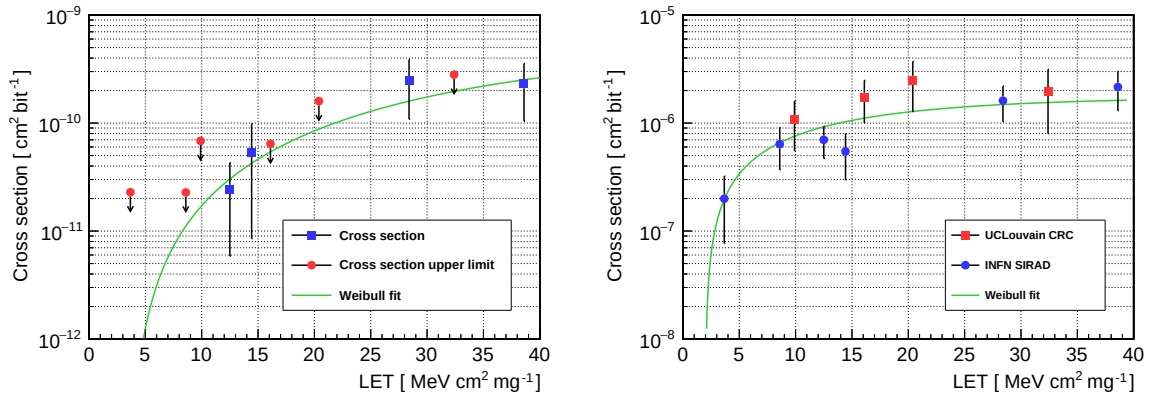

Figure 4. On the left and on the right, respectively, the SEU cross section as function of the LET for the I^{2}C interface and for the data path. The points marked with an upper limit did not exhibit any SEU during the irradiation period.

Finally, a portion of the pre-production dies, whose performance was verified in the laboratory before installation, were employed to equip 250 channels of a spare ECAL module for extensive integration tests and beam testing. Two beam test campaigns were conducted at CERN H4 facility in November 2022 and July 2023, utilizing electron beams ranging from 20 to 300 GeV. These campaigns confirmed that the ASIC, when integrated into the system, behaves as expected and delivers adequate performance in terms of stability, time and energy resolution.

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4 Conclusion

To meet the demanding conditions foreseen for the HL-LHC, a complete redesign of the ECAL barrel readout is required. In this context, two ASICs have been developed for the new front-end electronics: a faster trans-impedance amplifier, the CATIA, and a new data conversion and digital processing ASIC, the LiTE-DTU. The operation of these two ASICs, combined with the new back-end, ensures that the specified requirements are fulfilled. This includes maintaining energy resolution comparable to the current system, achieving a time resolution of less than 30 ps for electrons and photons above 50 GeV, and effectively discriminating spikes, anomalous signals resulting from APD direct ionization.

The LiTE-DTU ASIC, an essential component for this upgrade, will handle the 12-bit 160 MS s^{-1} analog-to-digital conversion of the two CATIA outputs, along with gain selection, data compression, and 1.28 Gbps serialization. Designed to be radiation-tolerant, the ASIC underwent extensive testing, both in laboratory settings and when integrated into the readout chain for system tests and beam tests. The test results indicate that the ASIC performance fits entirely the EB upgrade requirements. Radiation tests, which yielded successful outcomes, were conducted to validate the radiation tolerance of the ASIC. The final iteration of the ASIC, LiTE-DTU v3, was submitted for the final production run of approximately 85000 chips in March 2023. A comprehensive fully automated test procedure has been developed and successfully integrated into the final industrial test system, which is currently in an advanced stage of development.

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