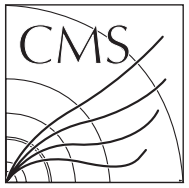
Available on CMS information server

CMS CR -2023/243



The Compact Muon Solenoid Experiment

Conference Report

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

30 October 2023 (v4, 03 November 2023)

Test and performance of the LiTE-DTU ASIC for the HL-LHC upgrade of the CMS ECAL barrel

Fabio Cossio for the CMS Collaboration

Abstract

A data conversion and compression ASIC, named LiTE-DTU, has been developed for the upgrade of the CMS electromagnetic calorimeter (ECAL) for the High-Luminosity phase of LHC. The ASIC integrates two 12-bit 160 MS/s ADCs, a data processing unit for gain selection and data compression, and a 1.28 Gb/s serializer.The ASIC has been extensively tested in laboratory and in beam tests showing excellent yield and performance. The radiation tolerance has been verified with dedicated test campaigns for both total ionizing dose and single event effects. Results from these tests, showing the design readiness for mass production, will be presented.

Presented at *TWEPP2023 Topical Workshop on Electronics for Particle Physics*

Prepared for submission to JINST

Test and performance of the LiTE-DTU ASIC for the HL-LHC upgrade of the CMS ECAL barrel

Fabio Cossio for the CMS Collaboration

INFN, Sezione di Torino,
Via Pietro Giuria, 1, 10125 Torino, Italy

E-mail: fcossio@to.infn.it

Abstract: A data conversion and compression ASIC, named LiTE-DTU, has been developed for the upgrade of the CMS electromagnetic calorimeter (ECAL) for the High-Luminosity phase of LHC. The ASIC integrates two 12-bit 160 MS/s ADCs, a data processing unit for gain selection and data compression, and a 1.28 Gb/s serializer. The ASIC has been extensively tested in laboratory and in beam tests showing excellent yield and performance. The radiation tolerance has been verified with dedicated test campaigns for both total ionizing dose and single event effects. Results from these tests, showing the design readiness for mass production, will be presented.

Keywords: HL-LHC, CMS, Calorimeters, Front-end electronics for detector readout, Data processing methods, Data reduction methods, Radiation-hard electronics

Contents

1 The HL-LHC ECAL upgrade

The Electromagnetic Calorimeter (ECAL) of the Compact Muon Solenoid (CMS, [1, 2]) detector is a crucial component that plays a significant role in the experiment's physics program. It is responsible for identifying and reconstructing photons and electrons, and also for measuring jets and missing transverse energy. The ECAL consists of a total of 75,848 scintillating crystals made of lead tungstate ($PbWO_4$), arranged in a central cylindrical barrel (BCAL) and two endcap disks.

For the forthcoming upgrade of the Large Hadron Collider (LHC) to the High Luminosity LHC (HL-LHC), it is planned to increase the accelerator instantaneous luminosity by a factor of 5 to 7.5 with respect to the LHC nominal value, thus leading to an average number of 140-200 concurrent interactions per LHC bunch crossing (pileup) [3]. The greater radiation damage and higher particle rates due to the increased luminosity pose new challenges to the detectors and their readout electronics. As a consequence, in order to fully exploit the HL-LHC physics potential and keep the ECAL current performance, a number of important upgrades are foreseen, with distinct approaches for the detector and the electronics.

In the case of the BCAL, the existing crystals and Avalanche Photo-Diode (APD) sensors will be retained and the APD dark current increase due to radiation damage will be mitigated by reducing the operating temperature from 18°C to 9°C [4]. On the contrary, because of the higher transparency loss of the crystals, the endcap regions will feature a completely new and different detector, the High-Granularity Calorimeter (HGCAL) [5].

The LHC upgrade, with the more demanding Phase-2 trigger requirements, requires also a complete redesign of the BCAL electronics. The trigger latency will be extended from around 4.5 µs to a maximum of 12.5 µs while the Level-1 (L1) trigger rate will increase from 100 kHz to approximately 750 kHz [6]. Furthermore, the single crystal information will be used to generate the L1 trigger with respect to the previous 5x5 crystal sums. The new electronics will also need to sustain the increased pileup and the higher rate of fake signals due to the direct interaction of collision particles with the APDs (referred to as "APD spikes").

2 The new ECAL Barrel front-end electronics

A schematic representation of the new electronics readout chain is displayed in Figure 1. The very front-end (VFE) board hosts two single-channel ASICs to amplify and digitize the signals coming from one crystal.

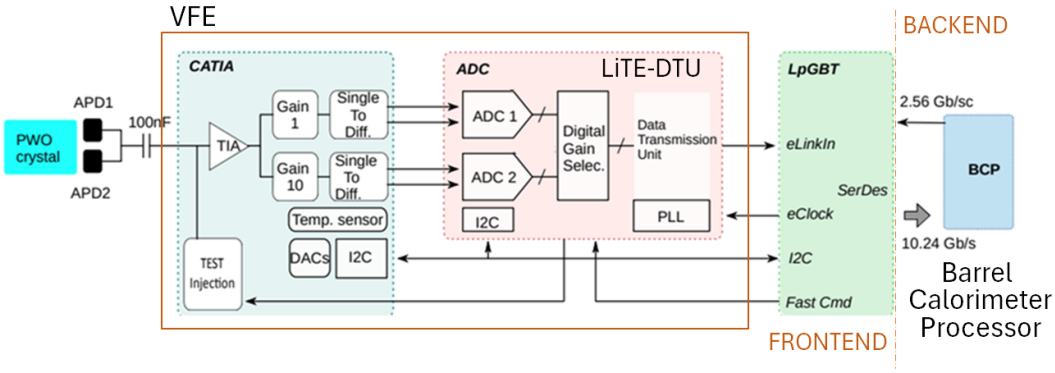


Figure 1. Scheme of the new ECAL readout electronics for the Phase 2 upgrade.

The first one, CATIA (CAlorimeter Trans-Impedance Amplifier[7]), is a transimpedance amplifier (TIA) designed with a bandwidth of 35 MHz to retain the swift pulse shape of the scintillator-APD signals, making it more robust against noise increases resulting from radiation-induced APD leakage current. The TIA-based architecture also offers improved rejection of signals originating from "APD spikes" since they have a faster rise time and shorter duration compared to the scintillation light signals. Designed in a 130 nm CMOS process, CATIA incorporates two differential outputs, with x1 and x10 gain configuration ensuring accurate energy and time resolution for signals from 50 MeV to 2 TeV. Its radiation hardness has been tested for doses up to 10 Mrad.

The second ASIC is called LiTE-DTU (LIsbon-Turin Ecal Data Transmission Unit, [8]) and features two 12-bit Analog-to-Digital Converters (ADCs) working in parallel to sample the two CATIA outputs at a 160 MHz rate. These data streams are processed by the digital logic of the LiTE-DTU, which incorporates a time window-based sample gain selection mechanism, allowing the transmission of the highest non-saturated gain channel of CATIA and a lossless data compression algorithm in order to fit the data in a single 1.28 Gb/s serial link. The 1.28 GHz clock required by the ADCs and serializers is generated on-chip from the 160 MHz master clock by a phase-locked loop (PLL) circuit. The LiTE-DTU is designed in a commercial CMOS 65 nm technology and to be radiation-tolerant up to 5 Mrad. It employs error-correction coding and triple modular redundancy to cope with single event upsets (SEU). Figure 2 shows a schematic of the LiTE-DTU architecture and a photograph of the ASIC assembled in its package.

The LiTE-DTU data is transmitted via the lpGBT optical transceiver [9] to the off-detector Barrel Calorimeter Processor (BCP [10]) FPGA-based electronics, where the L1 trigger primitives are generated. The new BCAL electronics, with faster signal processing, will provide a much-improved time resolution of 30 ps for photons and electrons with energies above 50 GeV, thus enabling precise primary-vertex determination by disentangling events associated with pileup.

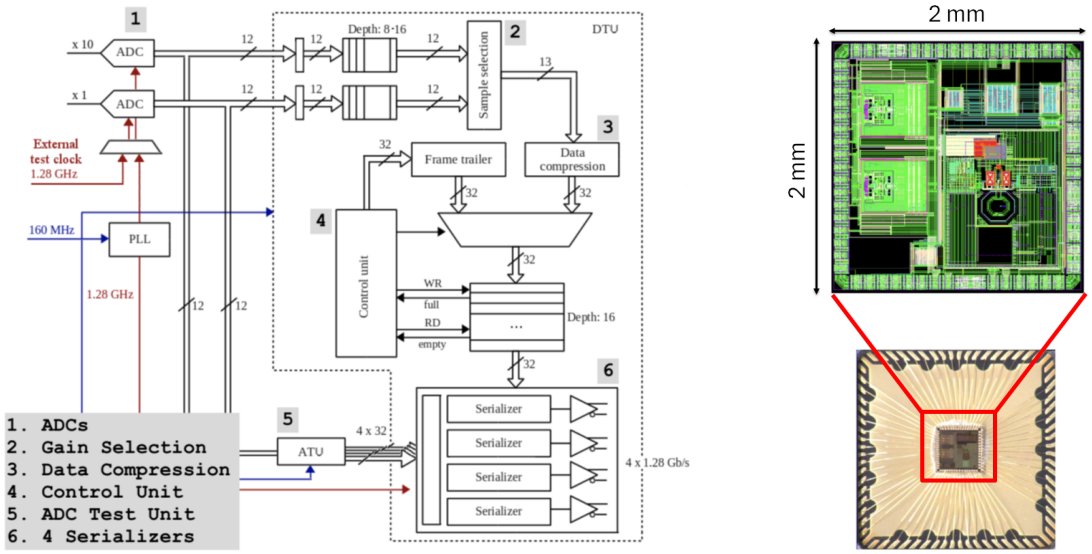


Figure 2. LiTE-DTU architecture scheme (left) and layout view with QFN72 package photograph (right): the die size is 2×2 mm^2, the two ADC cores are placed on the left side of the chip, while the PLL and the DTU logic are respectively on the bottom right and on the top right of the chip.

3 Test results

The LiTE-DTU ASIC has been extensively tested both in laboratory and with beam test campaigns. For the laboratory tests, a standalone setup has been arranged to test and evaluate the performance of the ASIC even when the CATIA amplifier is not connected. In this setup, as shown in Figure 3, the input signal is provided by external signal generators, while output data are read by an FPGA (Xilinx Kintex UltraScale KU040 Development Board) and sent to the acquisition computer using a UDP-based Ethernet link and a Python-based custom test interface. This computer also remotely controls the external instruments used to deliver the 160 MHz clock and provide the power supply to the system, as well as the external waveform generators connected at the ADCs inputs. Two different versions of the LiTE-DTU test-board have been designed: the first one is used to measure the performance of the ASIC and in this case the ASIC package is directly soldered on PCB, while the other board features a zero insertion force (ZIF) socket to perform a fast automated test to validate a large number of devices. Both versions provide DC- and AC-coupling to the ADCs inputs, via dedicated relays controlled by the FPGA, to deliver both the low-noise DC voltage references, for the ADCs calibration, and the sine waveforms, for the ADCs characterization.

The performance of the ADCs embedded in the LiTE-DTU ASIC has been measured following the methods for the testing and evaluation of ADCs described in [11]. The effective number of bits (ENOB) has been measured using an input sine wave of specified amplitude and for different input frequencies, as displayed in Figure 4. An ENOB of 9.4 has been measured at 50 MHz input frequency for both ADCs. This value, obtained using the internal PLL clock, is slightly lower than the design value of 10.2. Measurements using an external clock source and delivering an ENOB of 10.2 indicate that this degradation is due to the PLL clock jitter. The improvement observed at 40 MHz when using the internal clock can be ascribed to an interference coming from the 40 MHz

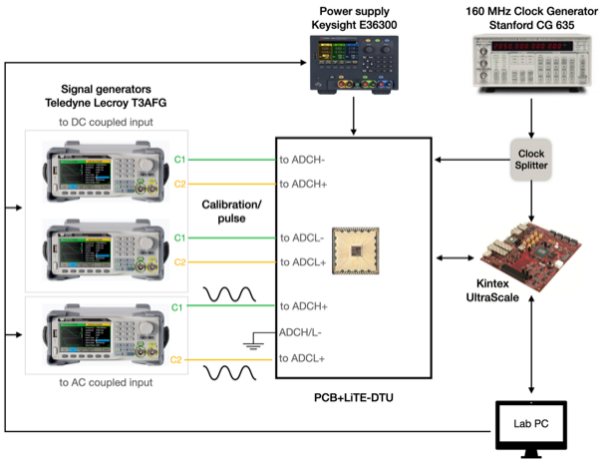


Figure 3. LiTE-DTU standalone setup used for the ASIC characterization and the pre-production version validation tests.

clock signal from the PLL making it a significant component of the jitter. For a 40 MHz input sine wave, the resulting spurs are either superimposed on the input tone or pushed to 0 and 80 MHz. The overall performance is already adequate for the system requirements, nevertheless the PLL clock jitter will be improved in the ASIC next version.

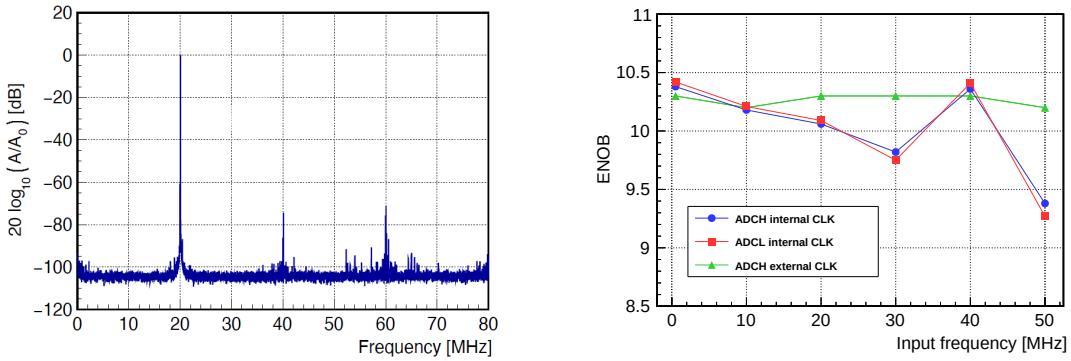


Figure 4. FFT of the digitized signal using an input sine wave of about 20 MHz frequency and the internal clock generated by the on-chip PLL (left) and resulting ENOB as a function of the input frequency with a comparison between internal and external clock (right).

Radiation tests have been carried out to assess the LiTE-DTU tolerance to total ionizing dose (TID) damage with 10 keV X-rays up to 50 kGy, which is approximately 2.5× higher than the BCAL expected dose in ten years of operation. No variation has been observed in the performance of the ASIC after irradiation. The LiTE-DTU has been tested also for SEU tolerance with two data taking campaigns using heavy ions beam, at Louvain-la-Neuve Cyclotron Resource Centre (CRC) Heavy Ion Facility (HIF) and at Laboratori Nazionali di Legnaro SIRAD irradiation facility. In Figure 5, the cross sections per bit for the I^2C registers and the data path are presented as a function of the linear energy transfer (LET) of the beam particles. The experimental data have been used to extrapolate the SEU cross section for protons using the Weibull function, as described in [12]. A cross section

of about $6.8 \cdot 10^{-18}$cm^2/bit is measured for the I^{2}C registers, while a value of $9.4 \cdot 10^{-13}$cm^2/chip is obtained for the data path, which is significantly higher as the ADC data registers are not SEU-protected since they are less critical. These results correspond to 5.5 I^{2}C errors/h and 627 data errors/h for the entire BCAL and are more than adequate for the LHC environment.

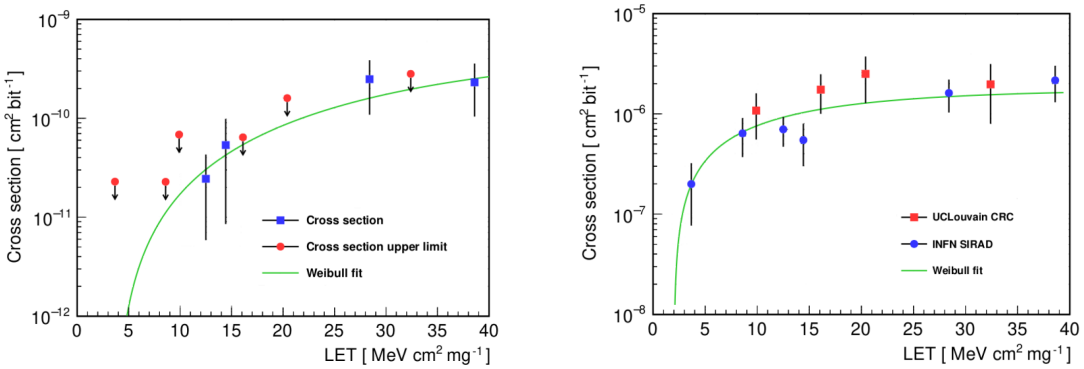


Figure 5. Cross section and Weibull fit for the I^{2}C interface (left) and for the data path (right).

A 600 dies pre-production has been employed to equip a ~200 channels ECAL module for large-scale integration tests and measure the performance and stability of the full readout chain. Before the assembly on the VFE cards, each LiTE-DTU chip has been tested and validated using an automated test sequence. The procedure included supply current check, PLL lock scan, bit and data alignment, ADCs calibration and validation, test-pulse injection for both gain ×1 and gain ×10 inputs and delivered a yield of about 97%. Two test-beam campaigns at the CERN H4 facility in November 2022 and July 2023 with 20-200 GeV electron beams allowed a full validation of the performances of the LiTE-DTU ASIC when integrated in the experiment readout chain.

4 Conclusions

The challenging conditions of the high luminosity upgrade of LHC have required a comprehensive overhaul of the CMS ECAL front-end electronics with two new ASICs: a fast trans-impedance amplifier (CATIA) and a data conversion and compression ASIC (LiTE-DTU). This upgrade will ensure high-precision energy measurements for the HL-LHC phase and the improved time resolution, of about 30 ps for photons and electrons above 50 GeV, will cope with the increased pileup level and enhance the rejection of spike signals produced from direct interaction with the APDs.

The LiTE-DTU ASIC integrates two 12-bit SAR ADCs to sample the CATIA outputs at 160 MHz. A gain selection mechanism and a lossless data compression algorithm allow data to be transmitted using only one 1.28 Gb/s serial link. The pre-production version of the ASIC has been thoroughly tested both in laboratory and in beam tests, showing excellent yield and performance. The radiation tolerance has been verified for TID and SEU with dedicated test campaigns. The ASIC final version has been submitted for mass production in May 2023. The first wafers were received in October 2023 and packaging operations are currently ongoing. A fully automatic test equipment for the test and validation of the LiTE-DTU mass production, which will deliver more than 100 thousand chips, has been developed and it is foreseen to start in November 2023.

References

[1] CMS Collaboration, *The CMS experiment at the CERN LHC*, *Journal of Instrumentation* **3** (2008) S08004.

[2] CMS Collaboration, "Development of the CMS detector for the CERN LHC Run 3." submitted to JINST, 2023. arXiv:2309.05466, https://cds.cern.ch/record/2870088.

[3] CMS Collaboration, *High-Luminosity Large Hadron Collider (HL-LHC): Technical design report*, CERN Yellow Reports: Monographs, CERN, Geneva (2020), 10.23731/CYRM-2020-0010.

[4] CMS Collaboration, *The Phase-2 Upgrade of the CMS Barrel Calorimeters*, Tech. Rep. CERN-LHCC-2017-011, CMS-TDR-015, CERN, Geneva (Sep, 2017).

[5] CMS Collaboration, *The Phase-2 Upgrade of the CMS Endcap Calorimeter*, Tech. Rep. CERN-LHCC-2017-023, CMS-TDR-019, CERN, Geneva (Nov, 2017).

[6] F. Thiant, Y. Geerebaert, F. Magniette, T. Romanteau, A. Zabi and A. Zghiche, *New development in the CMS ECAL Level-1 trigger system to meet the challenges of LHC Run 2*, *PoS* **TWEPP2018** (2019) 052.

[7] O. Gevin, P. Baron, M. Dejardin and F. Guilloux, *CATIA: APD readout ASIC for the CMS phase 2 ECAL electronics upgrade*, *PoS* **TWEPP2019** (2020) 001.

[8] G. Mazza, S. Argirò, C. Borca, S. Cometti, F. Cossio, M. Dejardin et al., *The LiTE-DTU: A Data Conversion and Compression ASIC for the Readout of the CMS Electromagnetic Calorimeter*, *IEEE Transactions on Nuclear Science* **70** (2023) 1215.

[9] S. Biereigel, S. Kulis, R. Francisco, P.V. Leitao, P. Leroux, P. Moreira et al., *The lpGBT PLL and CDR Architecture, Performance and SEE Robustness*, *PoS* **TWEPP2019** (2020) 034.

[10] N. Loukas, S. Goadhouse, T. Anderson, A. Belloni, T. Gorski, T. Grassi et al., *The CMS Barrel Calorimeter Processor demonstrator (BCPv1) board evaluation*, *Journal of Instrumentation* **17** (2022) C08005.

[11] *IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters*, *IEEE Std 1241-2010 (Revision of IEEE Std 1241-2000)* (2011) 1.

[12] M. Huhtinen and F. Faccio, *Computational method to estimate Single Event Upset rates in an accelerator environment*, *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* **450** (2000) 155.