Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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on behalf of the ATLAS LAr Calorimeter Group

Bundesministerium für Bildung und Forschung

FIS ATLAS

PUNCH 4NFDI

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Cape Town
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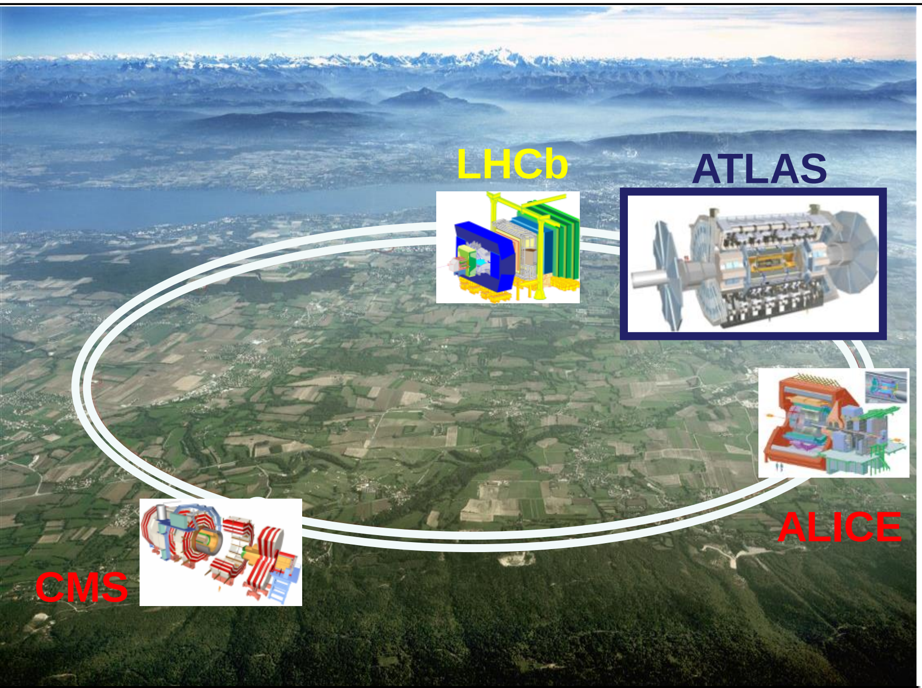
The ATLAS Experiment



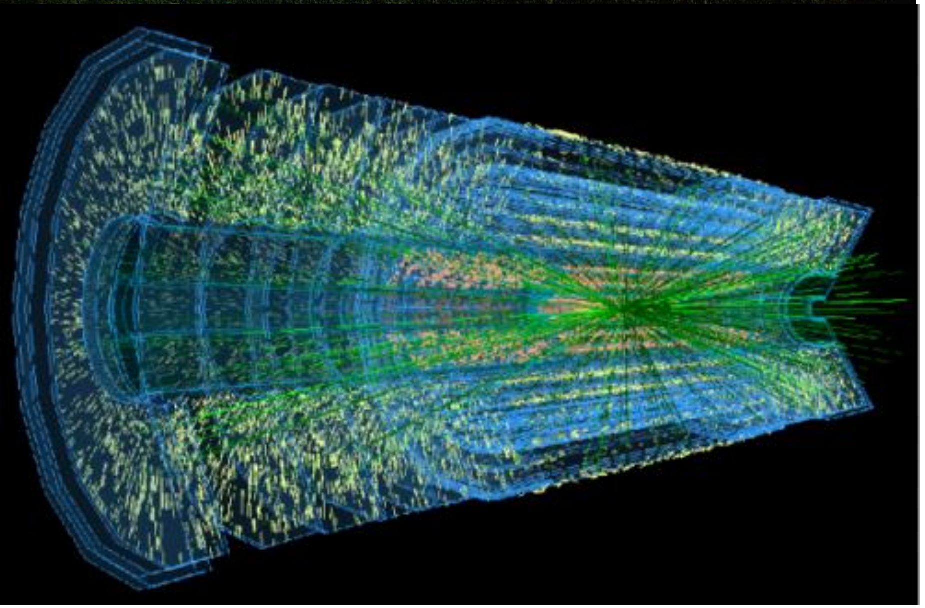
- ATLAS is one of the particle detectors at the Large Hadron Collider

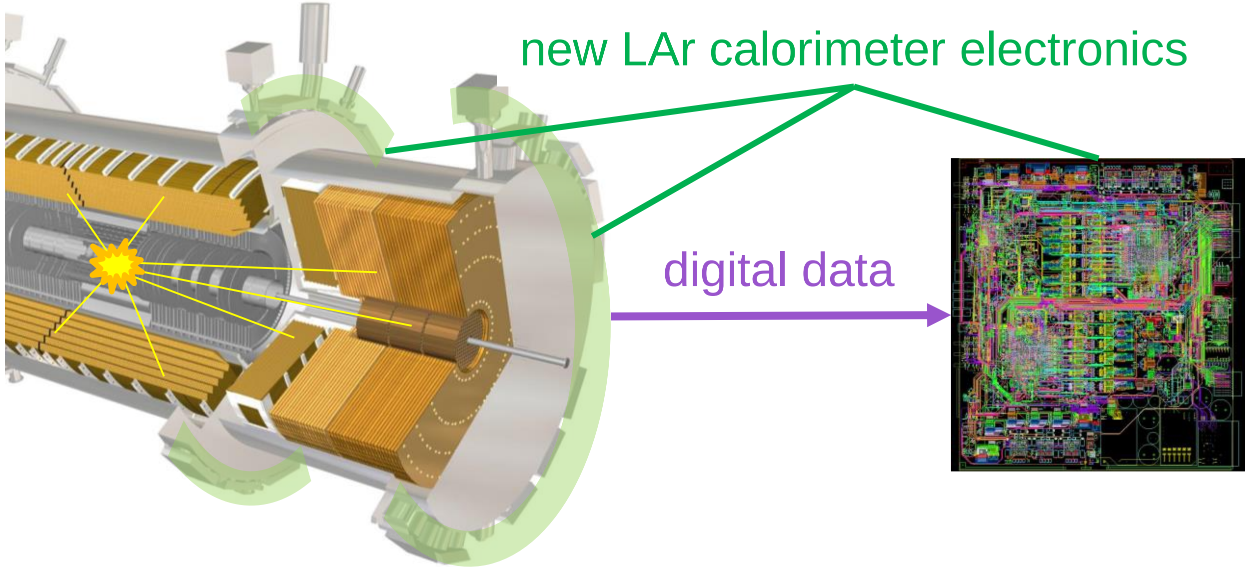
- A collider upgrade in 2026-2028 will increase the luminosity up to 7x the design value → High-Luminosity LHC (HL-LHC)
- 140-200 simultaneous proton-proton collisions are expected every 25 ns

- The liquid-argon (LAr) calorimeters will measure the energy of electrons, photons and hadronic particles in each of the 182.000 calorimeter cells

- New calorimeter electronics is needed to cope with improved ATLAS trigger system:

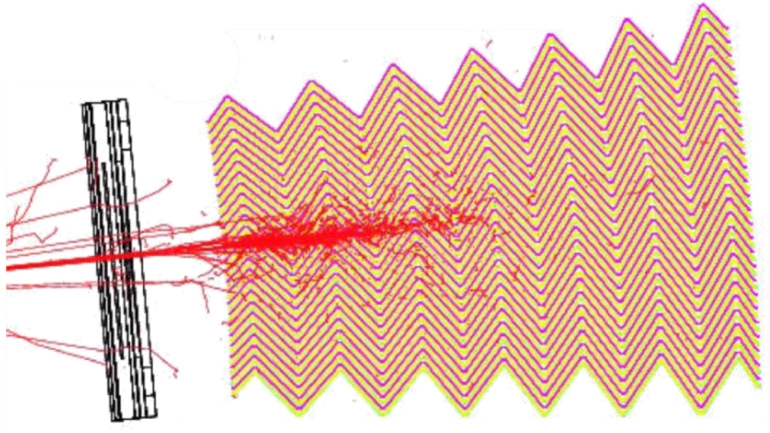
trigger rate	100 kHz (today) ⟶ 1 MHz (HL-LHC)
trigger latency	2.5 µs (today) ⟶ 10 µs (HL-LHC)

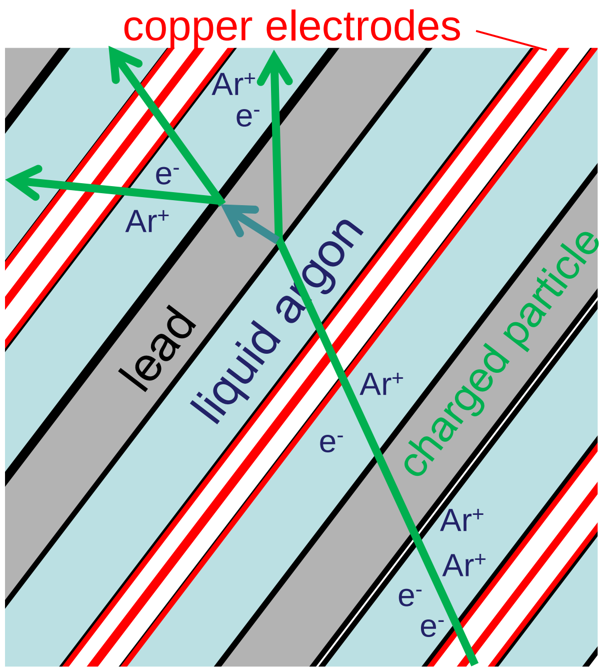


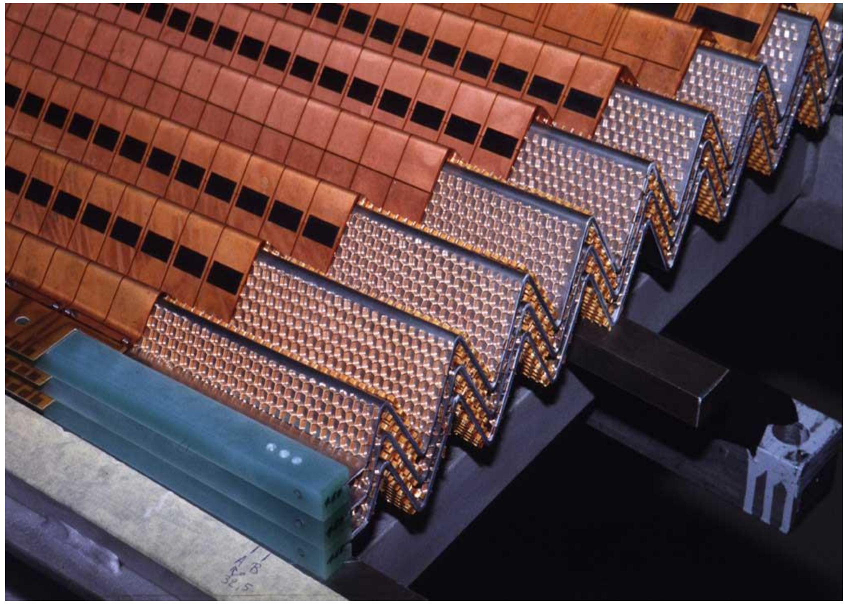


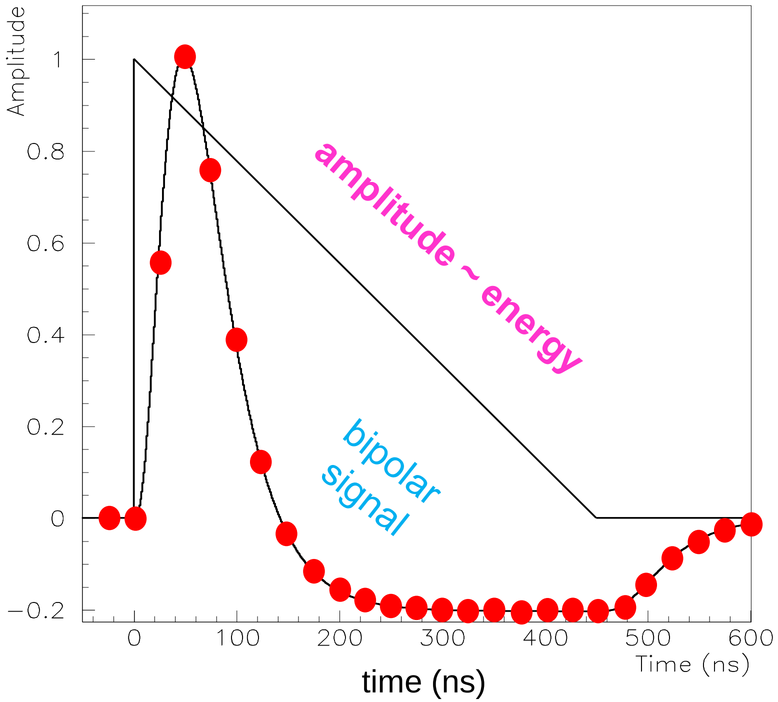
The Liquid-Argon Calorimeters

- The liquid-argon calorimeters are made of lead, copper and tungsten absorbers with narrow liquid argon gaps
- Charged particles of electromagnetic and hadronic showers ionize the liquid argon which induces a triangular drift signal on copper electrodes
- Signals are amplified, shaped and digitized



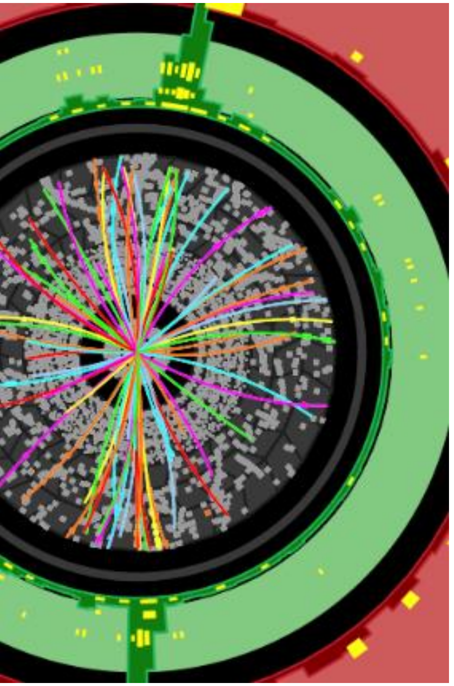






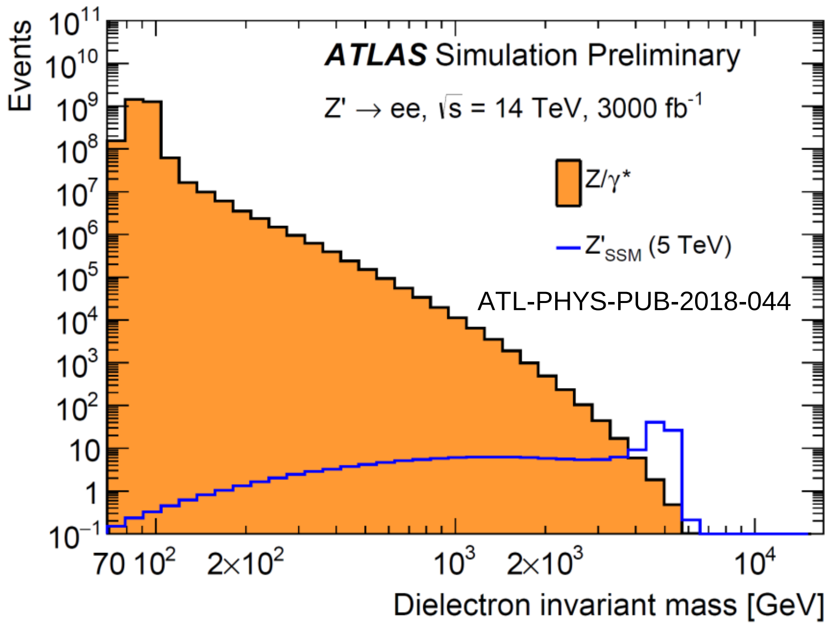
- The LAr calorimeters are intrinsically radiation tolerant and do not need to be replaced for HL-LHC operation

New Readout Electronics for the LAr Calorimeters

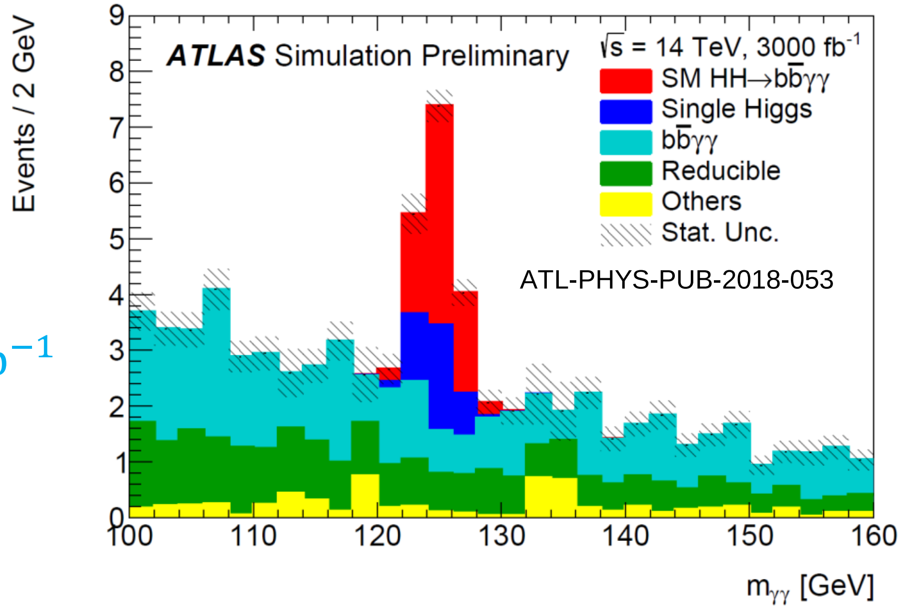


Run 427394 Event 3038977

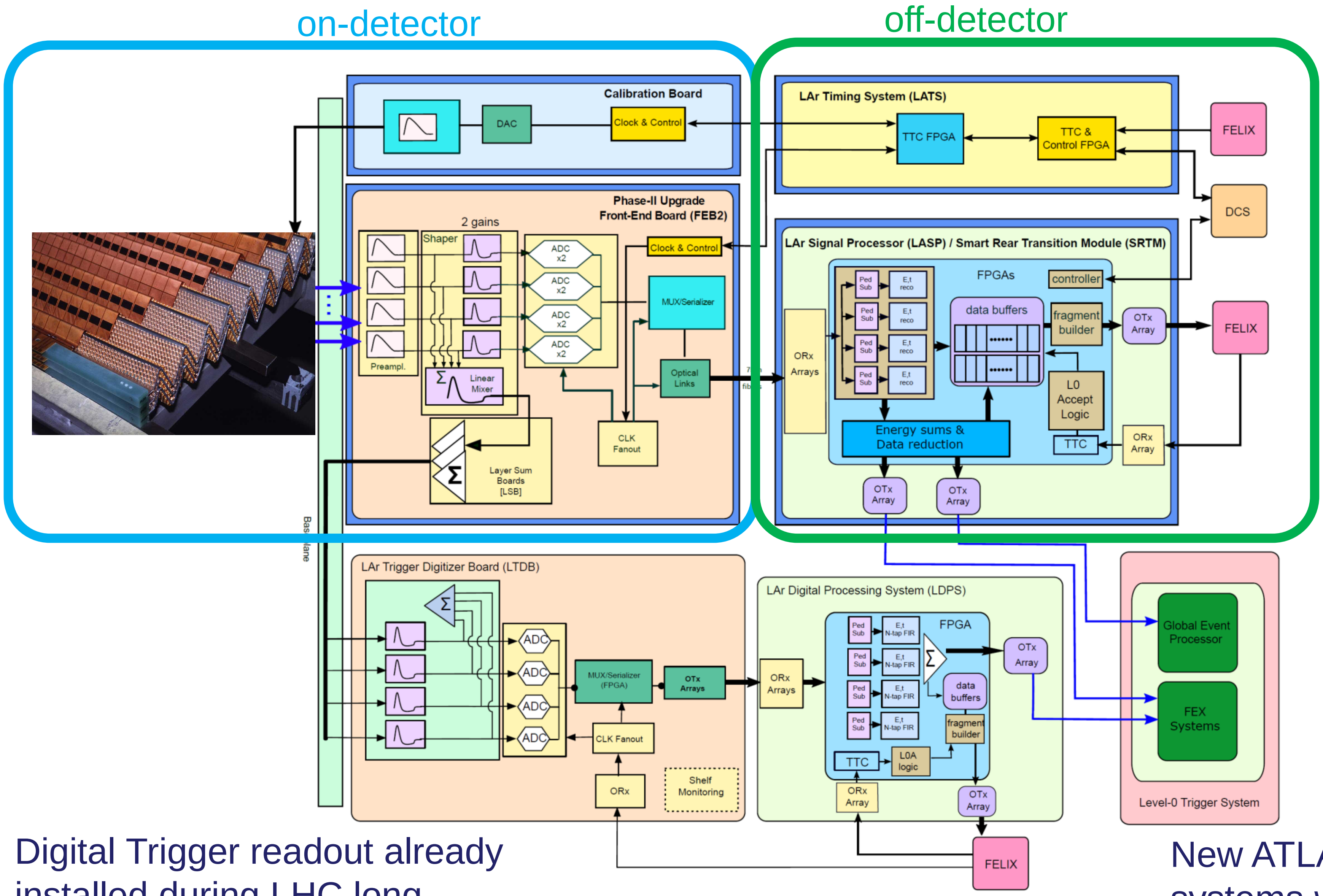
- 16 bit dynamic range of cell energies from 50 MeV to 2-3 TeV
- Electronic noise must stay below intrinsic calorimeter resolution
- Very low noise preamplifier with 2 amplification gains:
  - Electrons with $E_T = m_Z/2$ and photons with $E_T = m_H/2$ are in same high-gain range to reduce energy calibration systematics
- Non-linearity below 0.1% up to energies of 300 GeV



- Analog-to-digital conversion in every cell by two 14-bit ADCs with overlapping energy range to measure noise level and capture highest energy physics signals
- Radiation tolerance for 10 years of HL-LHC operation and $L_{\text{int}} = 3000\ \text{fb}^{-1}$



Components of the Future LAr Calorimeter Readout



- 1524 new front-end boards (FEB2) with pre-amplifier, shaper, ADC, layer sum-boards (LSB2) and digital data transmission
- 122 calibration boards for direct electronic signal injections
- Full-granularity, trigger-less readout with 36.000 optical fibers at 10.24 Gb/s each
- 278 LAr Signal Processors (LASP) with 2 FPGAs each
- LAr timing system (LATS) for trigger/time/control (TTC)

Digital Trigger readout already installed during LHC long-shutdown 2 (2019-2021)

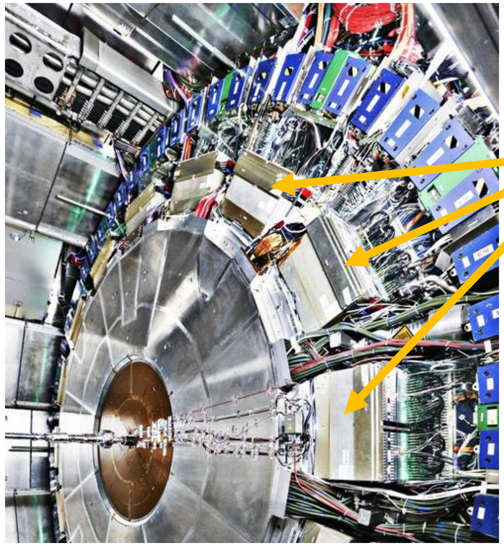
New ATLAS global and forward trigger systems will receive full-granularity calorimeter data at 40 MHz

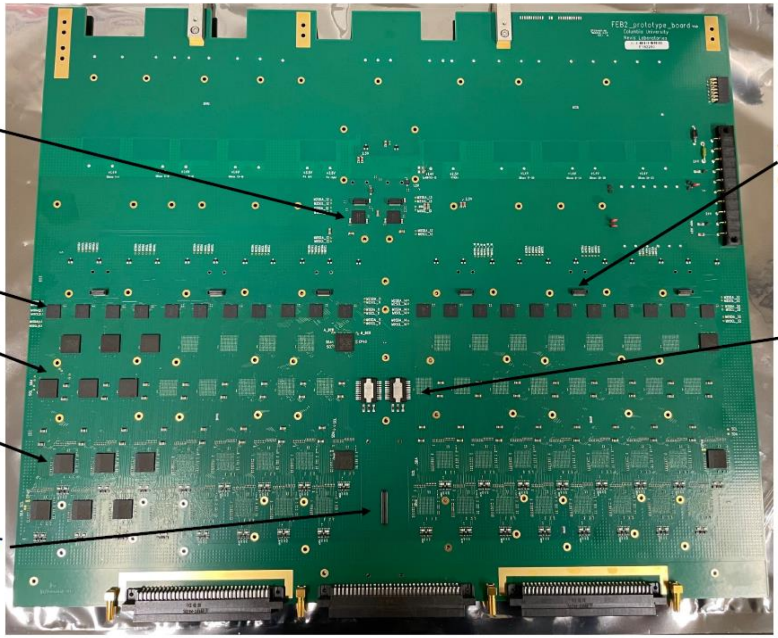
Front-end Board (FEB2)

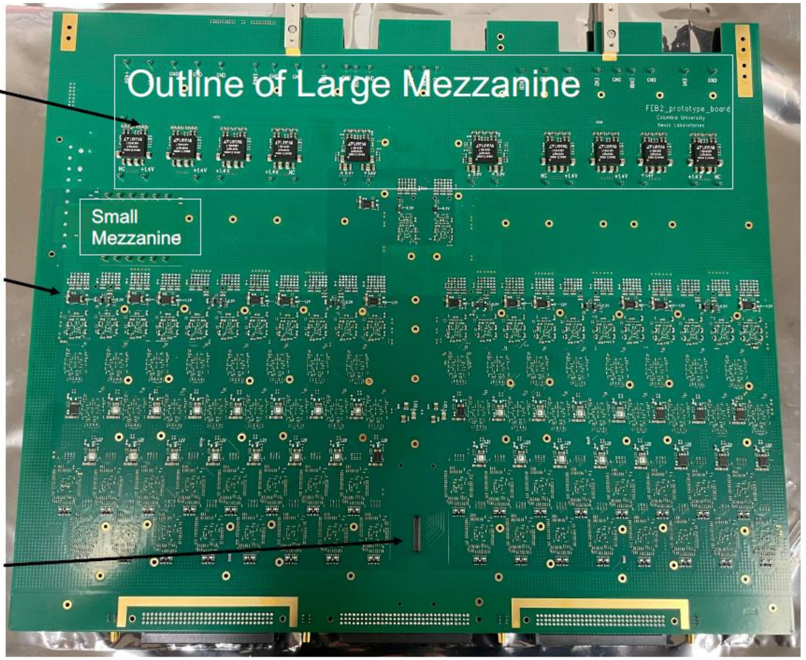
- Each front-end board covers up to 128 calorimeter cells

- Performance requirements:
  - coherent noise <5% of the total noise in each channel
  - electronics contribution to the crosstalk of less than 1%
  - clock distribution with <5 ps jitter for stable ADC operation
  - power consumption <1 W per channel

- First full prototype version in production:



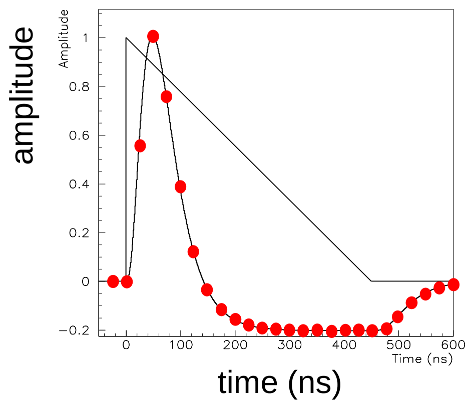




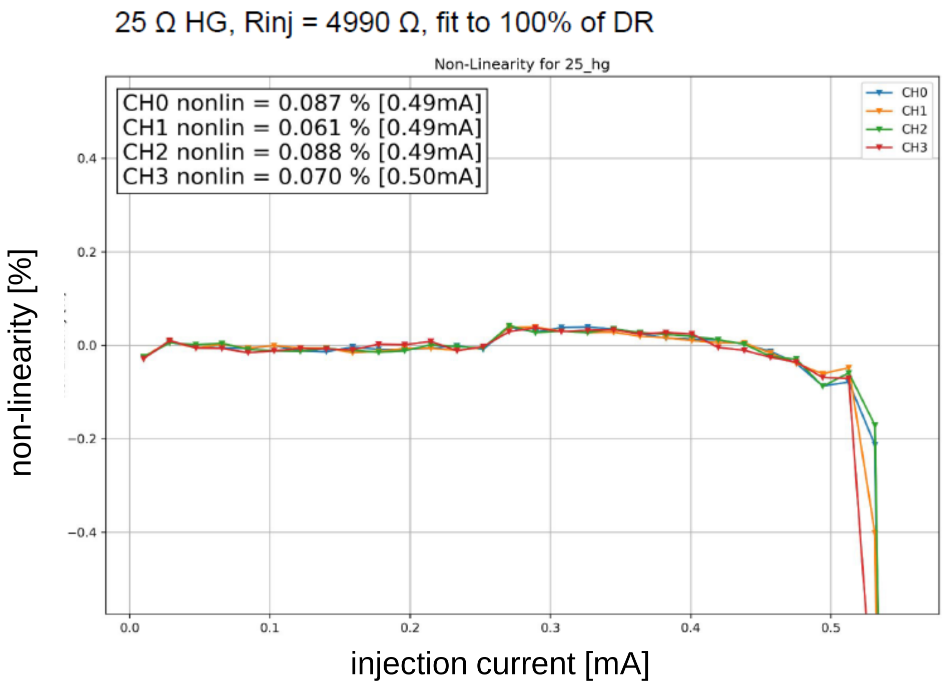
ALFE2 Pre-amplifier/Shaper ASIC

- ALFE2: dedicated ASIC developed for LAr calorimeter readout in 130 nm CMOS (50k pc.)
  - amplification with 2 gain scales and bipolar CR-(RC)^2 shaping

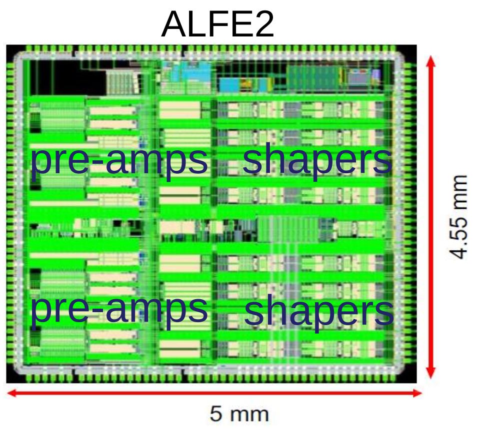
gain ratio 24:1	high gain (HG)	low gain (LG)
dynamic input range (DR)	2 mA	10 mA
integral non-linearity (INL)	±0.2% in 80% of DR ±5% in 100% DR	±0.5% in 80% of DR ±5% in 100% DR



- 4 channel analog input, 9 channel differential output to ADCs (4 x 2 gains and trigger sum of 4 channels)
- Shaping time 15±5 ns tunable in 1ns steps
- HPS2 ASIC variant as pre-shaper for hadronic calorimeter readout (pre-amplifier inside LAr cryostat)

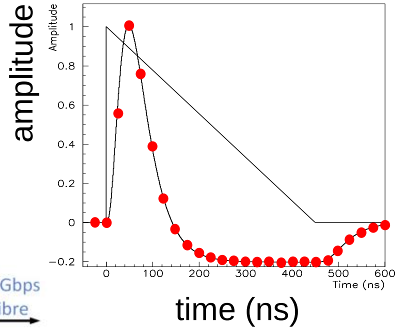


- ALFE2 ASIC meets the specifications
- Engineering production run is completed
- Radiation tests ongoing
- Series testing in preparation

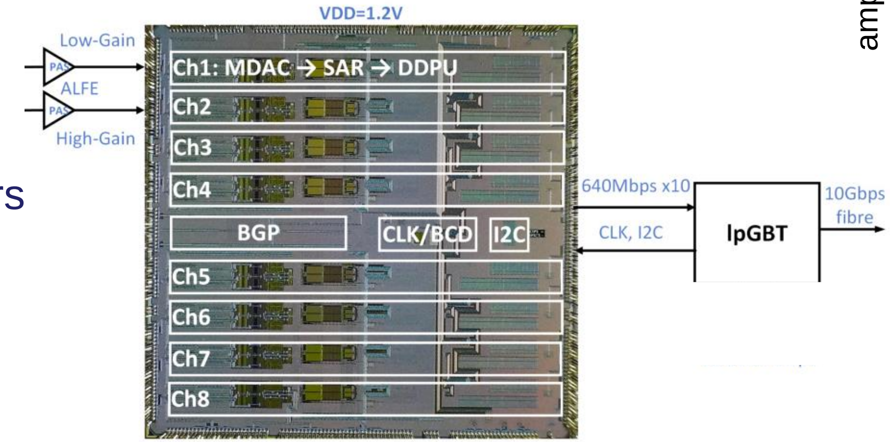


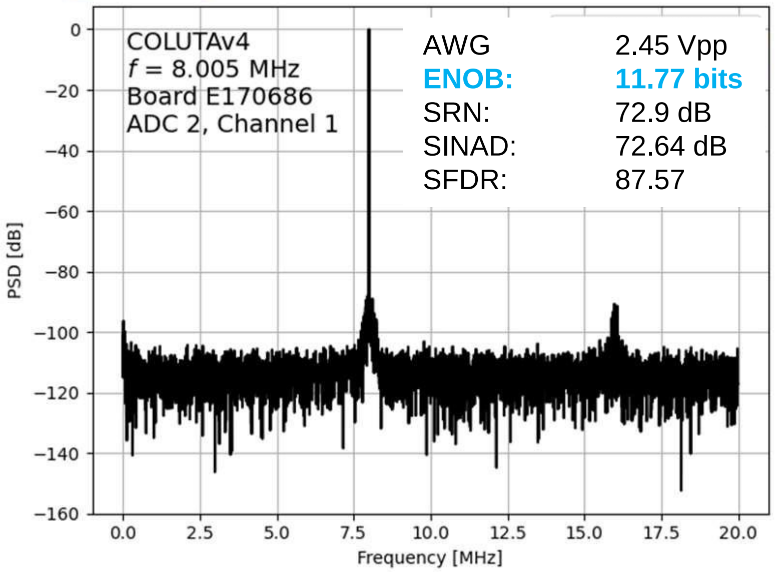
Analog-to-Digital Conversion: COLUTA ADC

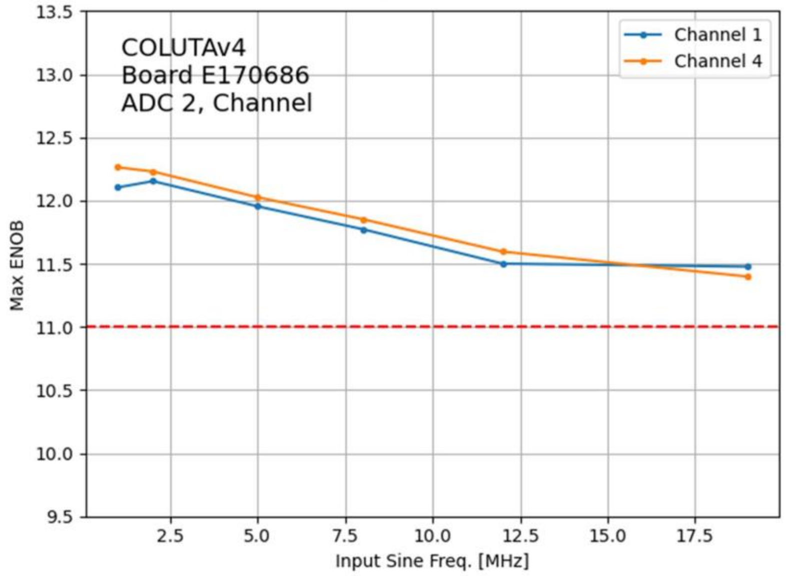
- 8-channel ADC with 40 MHz sampling rate,14-bit dynamic range and >11 bit resolution
- COLUTA: custom ASIC designed in 65 nm CMOS - 50k devices needed

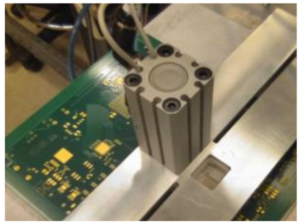


- Multiplying DAC (3 bits) and 12 bit Successive Approximation Register (SAR) → 15-bit ADC
- analog channels adapted to ALFE2 preamp/shaper: 4 HG/LG pairs
- Digital Data Processing Unit (DDPU) applies calibration and transmits data at 640 Mbps to lpGBT
- 140 mW per channel







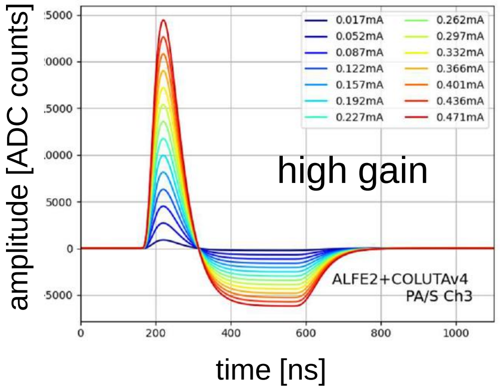


- Pre-production of COLUTA ADC is completed - preparation of mass production and automated series testing

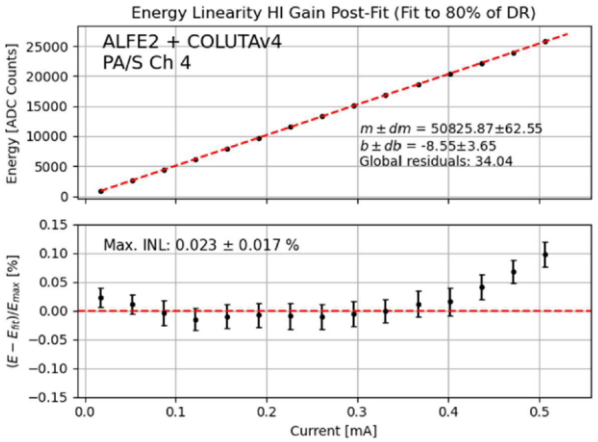
Combined Preamp/shaper and ADC Performance

- ALFE2 preamp/shaper and COLUTA ADC have been operated on a dedicated testboard
- Pulses are injected with arbitrary waveform generator (AWG)

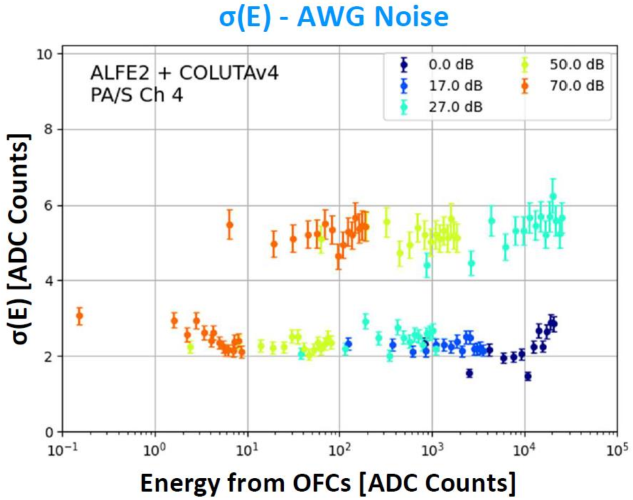
- Highly uniform pulse shapes



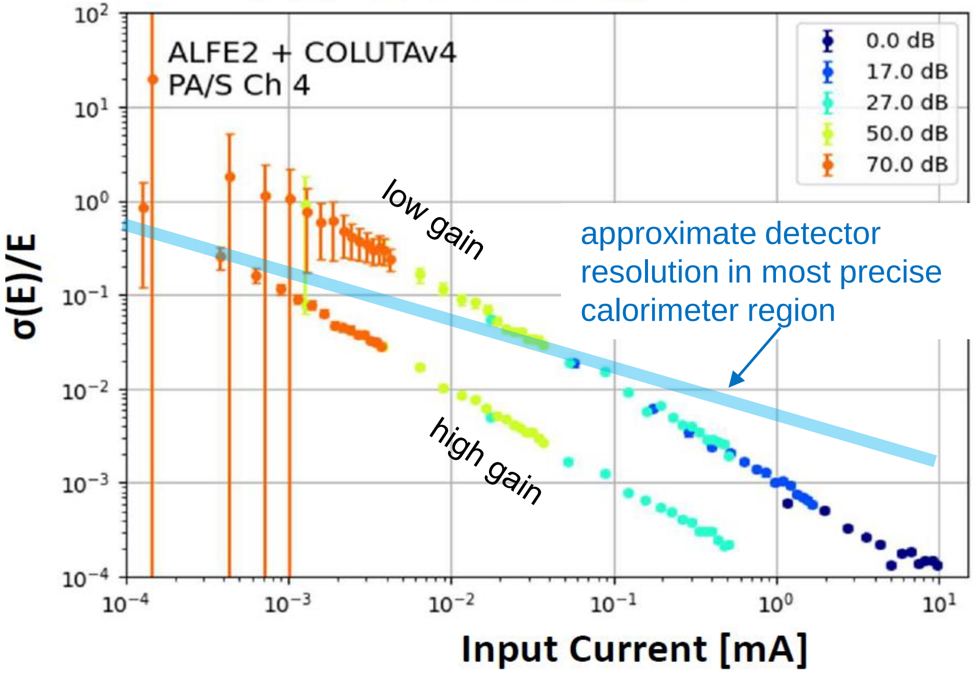
- Integral non-linearity (INL) in high gain < 0.05% for 80% DR, < 0.1% full DR
- Cross-talk <0.12% on all channels

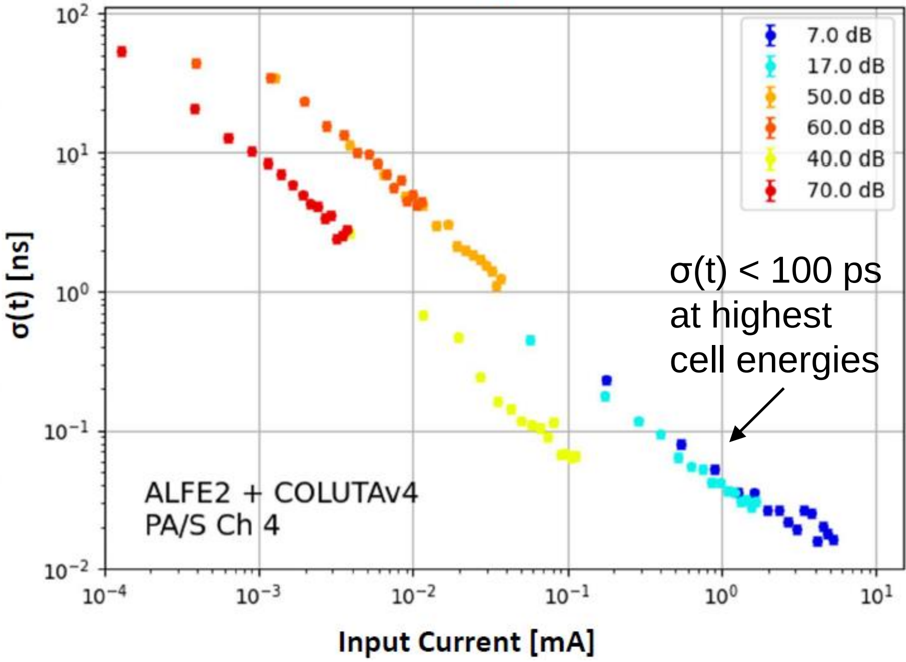


- typical noise level below ≃ 6 (3) ADC counts for HG (LG)



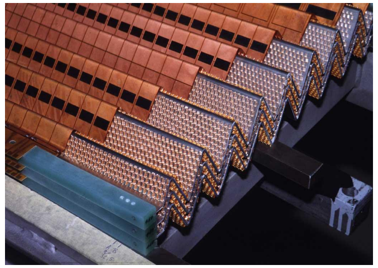
- electronic noise contribution to detector energy and time resolution:



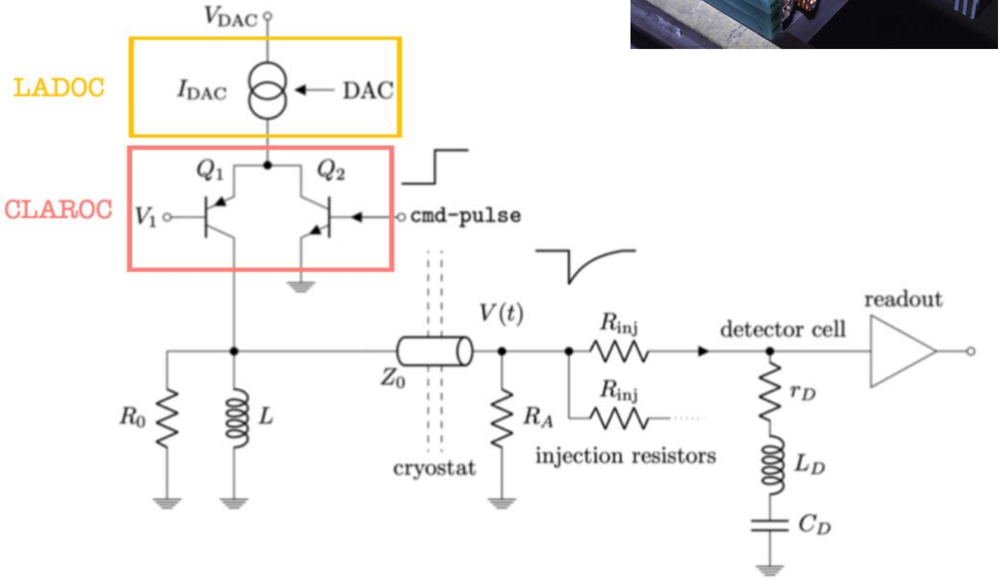


Calibration System

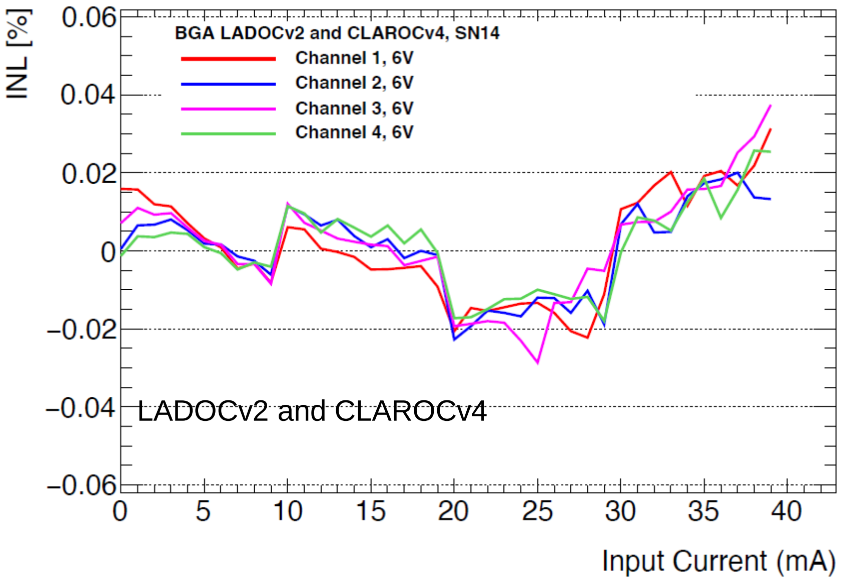
- Calibration boards inject well defined pulses at the LAr copper electrodes with 16 bit dynamic range
- Pulse is created by opening of HF-switch → CLAROC ASIC in 180nm HV-CMOS(XFAB)
- Controlled by digital to analog converter (DAC) → LADOC ASIC in 130nm (TSMC)

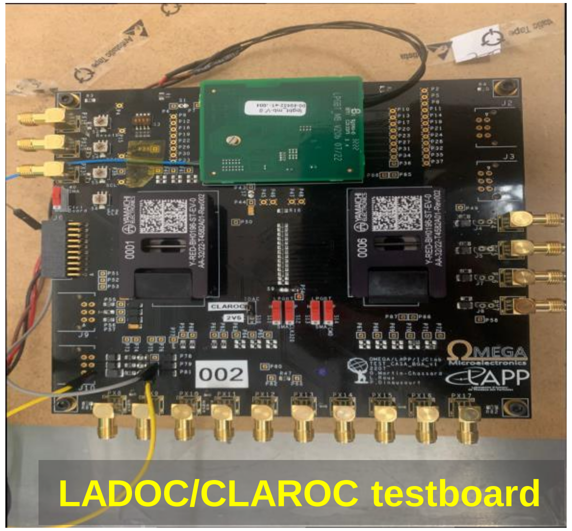


- Integral non-linearity specifications:
  - 0.1% in high-gain (0-5mA)
  - 0.2% in intermediate range (0-200mA)
  - 1-2% in high and very high current range (0-300/320 mA)



- LADOCv2 and CLAROCv4 perform a factor 2-10 better than specs





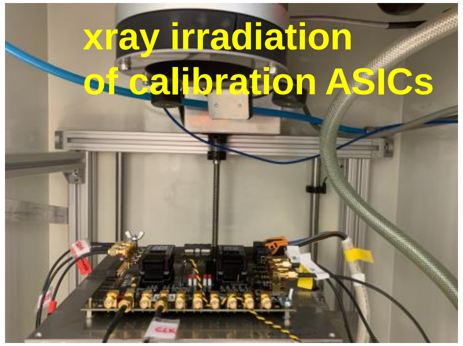
- 128-channel full-scale calibration board prototype (CABANE) is in preparation

Radiation Testing

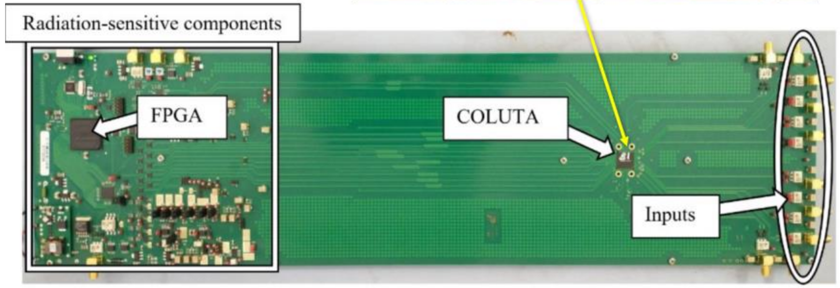
- All on-detector components are operated in radiation environment (safety factors are applied):

	TID [Gy]	NIEL [n_{eq}/cm^2]	SEE [$h_{>20\,MeV}/cm^2$]
FEC (barrel)	1400 (1.5)	4.1×10^{13} (2)	1.0×10^{13} (3)
FEC (endcap)	210 (1.5)	6.0×10^{12} (2)	1.2×10^{12} (3)
LVPS between TileCal fingers (barrel)	430 (1.5)	1.1×10^{13} (2)	2.8×10^{12} (3)
HEC and FEC LVPS (endcap)	81 (1.5)	2.0×10^{12} (2)	4.1×10^{11} (3)
LVPS new position (barrel)	18 (1.5)	5.1×10^{11} (2)	1.1×10^{11} (3)
LVPS new position (endcap)	33 (1.5)	5.2×10^{11} (2)	8.6×10^{10} (3)

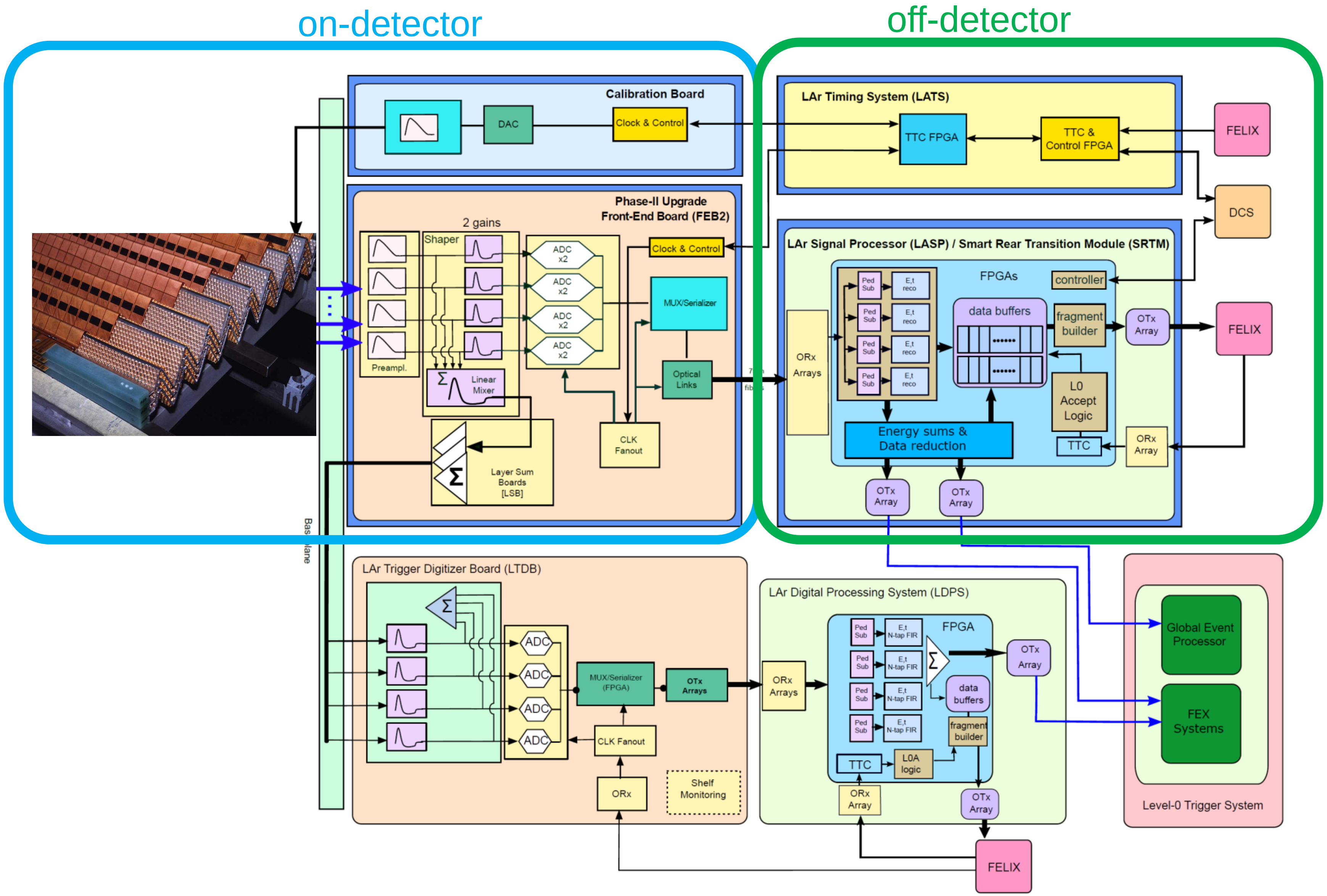
- Extensive irradiation program of ASIC prototypes and components
- Example results:
  - ALFE2 preamp/shaper single-event effects (SEE):
    - $\sigma_{SEE/bit} = 1.1 \times 10^{-15} cm^2 \rightarrow$ < 7 SEE expected/day @95 C.L.
  - COLUTAv4 ADC:
    - $\sigma_{SEE/ch} = 3.7 \times 10^{-10} cm^2 \rightarrow$ 6140 SEE/channel during HL-LHC
  - TID results of calibration ASICs under investigation
  - components of low-voltage power supplies (LVPS) tested successfully in neutron beam:
    - point-of-load converter bPOL48V, DC-DC converter EPC2152, GaN power stage LMG5200, ProAsic3 FPGA



proton beam test of COLUTA ASIC



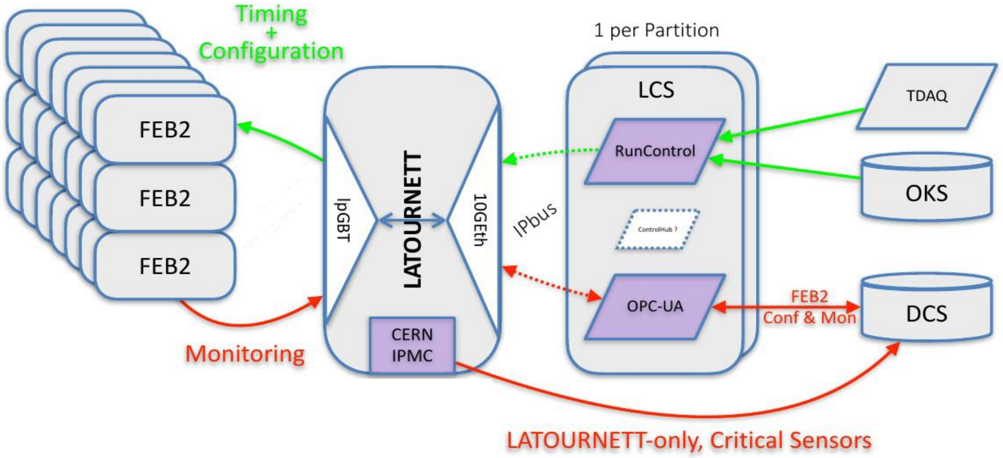
Components of the Future LAr Calorimeter Readout

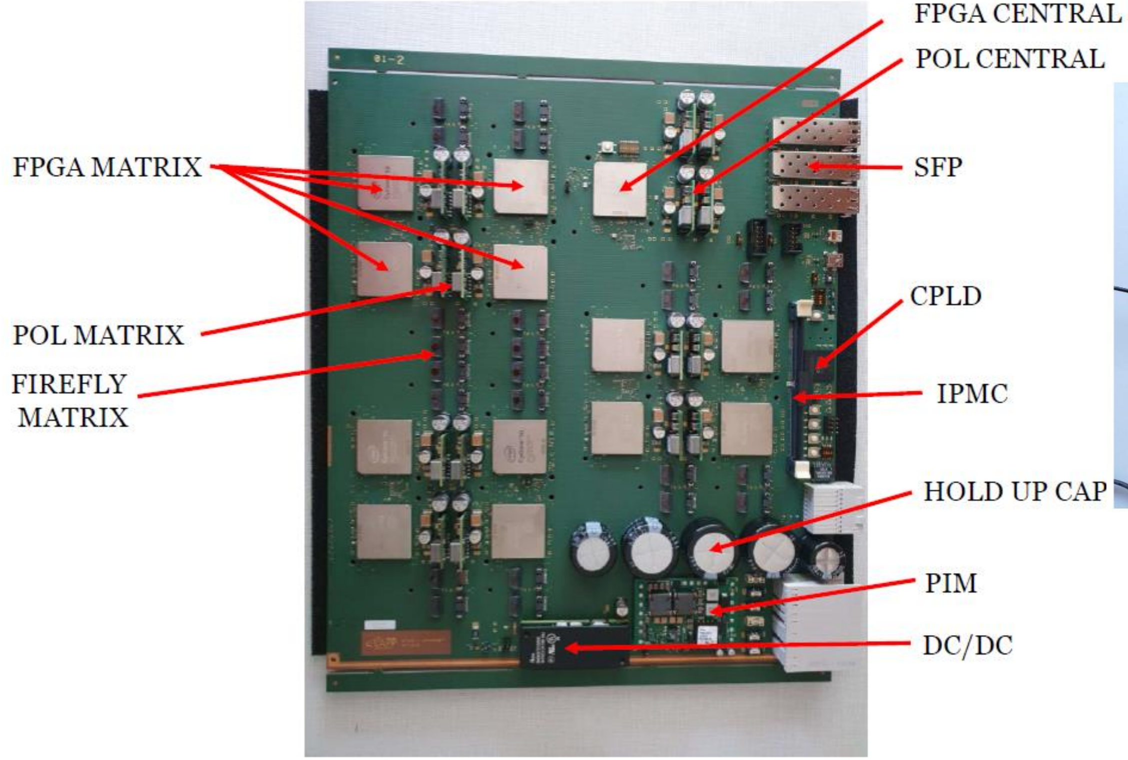


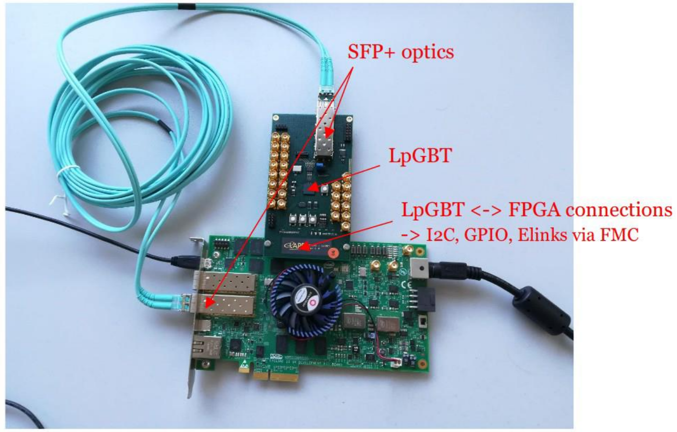
LAr Timing System

- ADCs on front-end boards (FEB2) require low-jitter timing signal → digital clock distribution using lpGBT
- LAr Timing System (LATS) provides clock to 1524 FEB2 and control functionality for FEB2 and Calibration boards

- 30 LATS ATCA blades each be equipped with 13 Cyclone10 GX FPGAs
- First full prototype cabled and basic electrical tests passed:





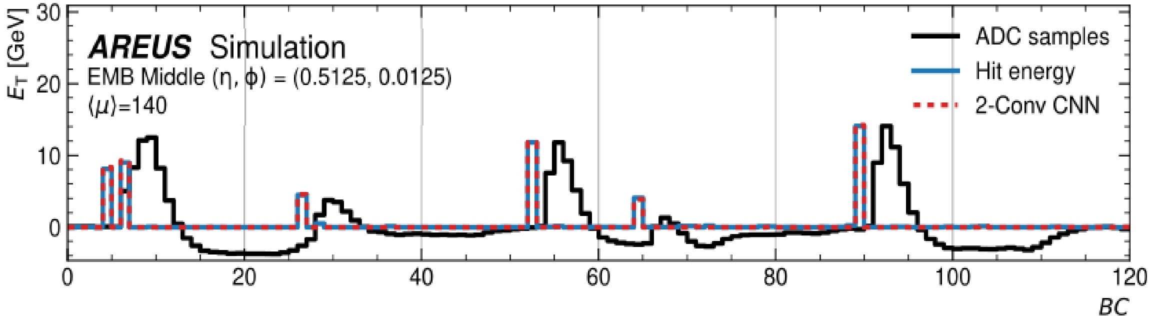


- Work on FPGA firmware and system infrastructure using FPGA devkit

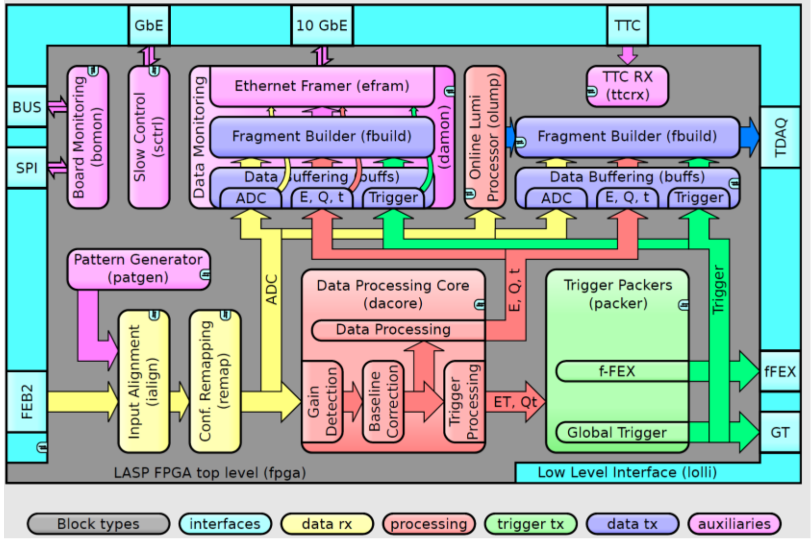
- lpGBT configuration and communication established
- next steps:
  - clock recovery with jitter cleaner
  - communication with FELIX system (ATLAS TTC)
  - communication with FEB2 and calibration board

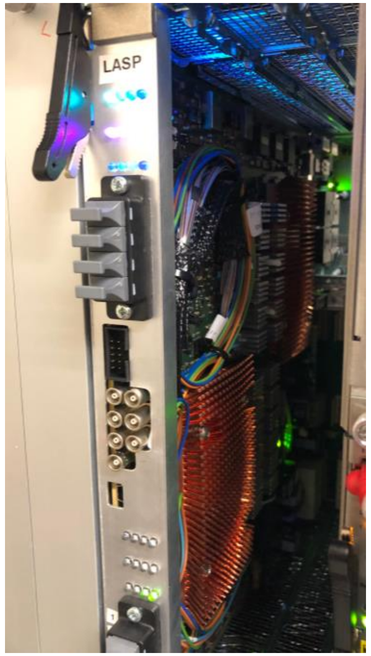
LAr Signal Processor

- Digital processing system with 556 FPGAs to handle 250 Tbps of input
- LAr Signal Processor (LASP) ATCA blades with 2 Intel Agilex FPGAs
    - data reception from up to 6 FEB2 per blade using lpGBT protocol
    - real-time cell energy and pulse-time determination
    - transmit calculated energies to new ATLAS trigger systems at 25 Gbps:
        - ATLAS Global trigger and forward feature extractor (fFEX)
    - data buffering until L0 trigger accept signal
- Complemented by Smart Rear Transition Module (SRTM) for readout data transmission and trigger+time+control (TTC) interface
- Advanced signal filtering is foreseen to suppress out-of-time signal pile-up: Artificial Neural Networks on FPGA*



- Firmware is evaluated on testboards and FPGA devkits
    - Main challenges: FPGA resource limitations and FPGA power dissipation
- Design of LASP and SRTM hardware prototypes is in progress





LASP testboard

SRTM testboard

*Thursday morning session F1 (E. Fortin)

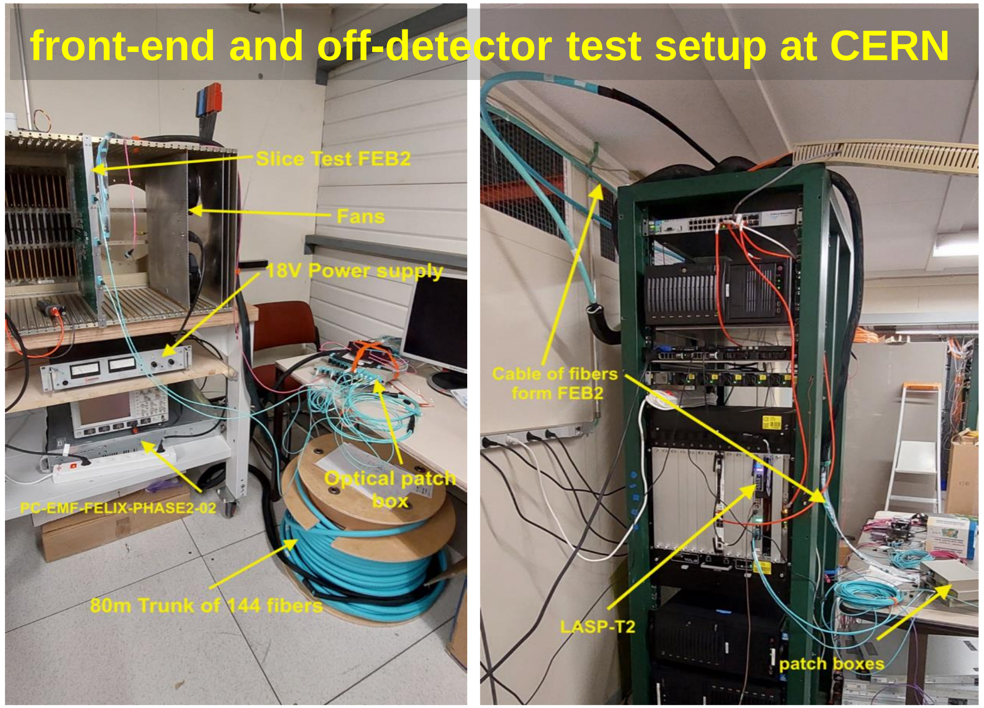
Conclusion and Outlook

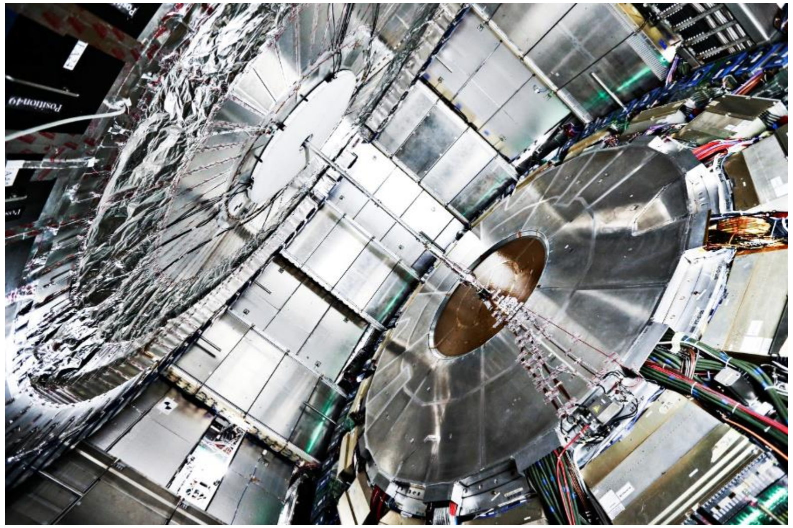
- The readout electronics of the ATLAS LAr calorimeters will be replaced by a more radiation tolerant system which supports 1 MHz trigger rates and longer trigger latencies

- All components are in advanced prototype stage or about to start series production
- All ASICs and readout boards are expected to be ready for installation in 2026

- System integration becomes a more and more important activity
- The full readout must be ready on day-1 of HL-LHC operation

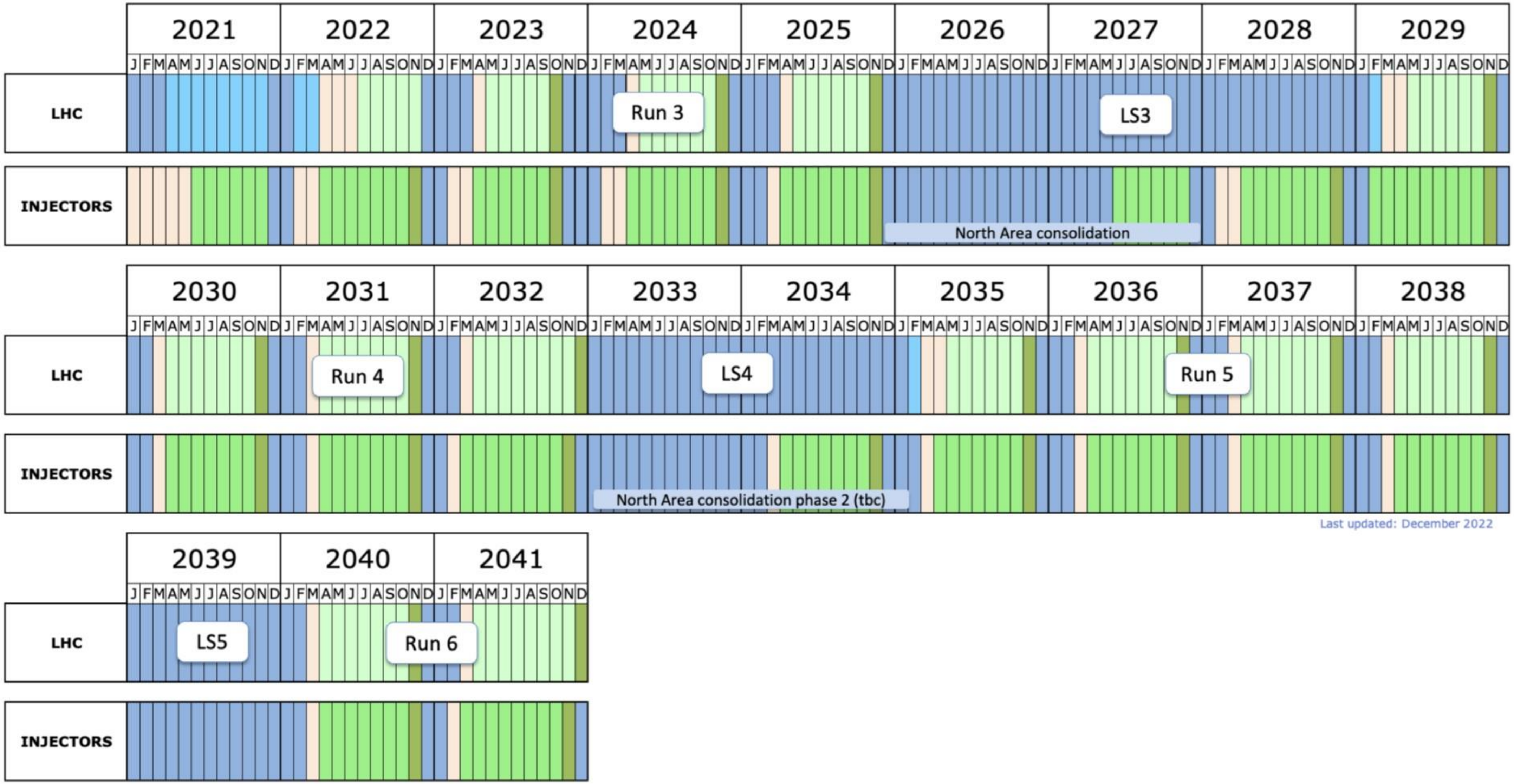
- We are looking forward to interesting physics measurements with much improved signal processing capabilities adapted to high luminosity data taking

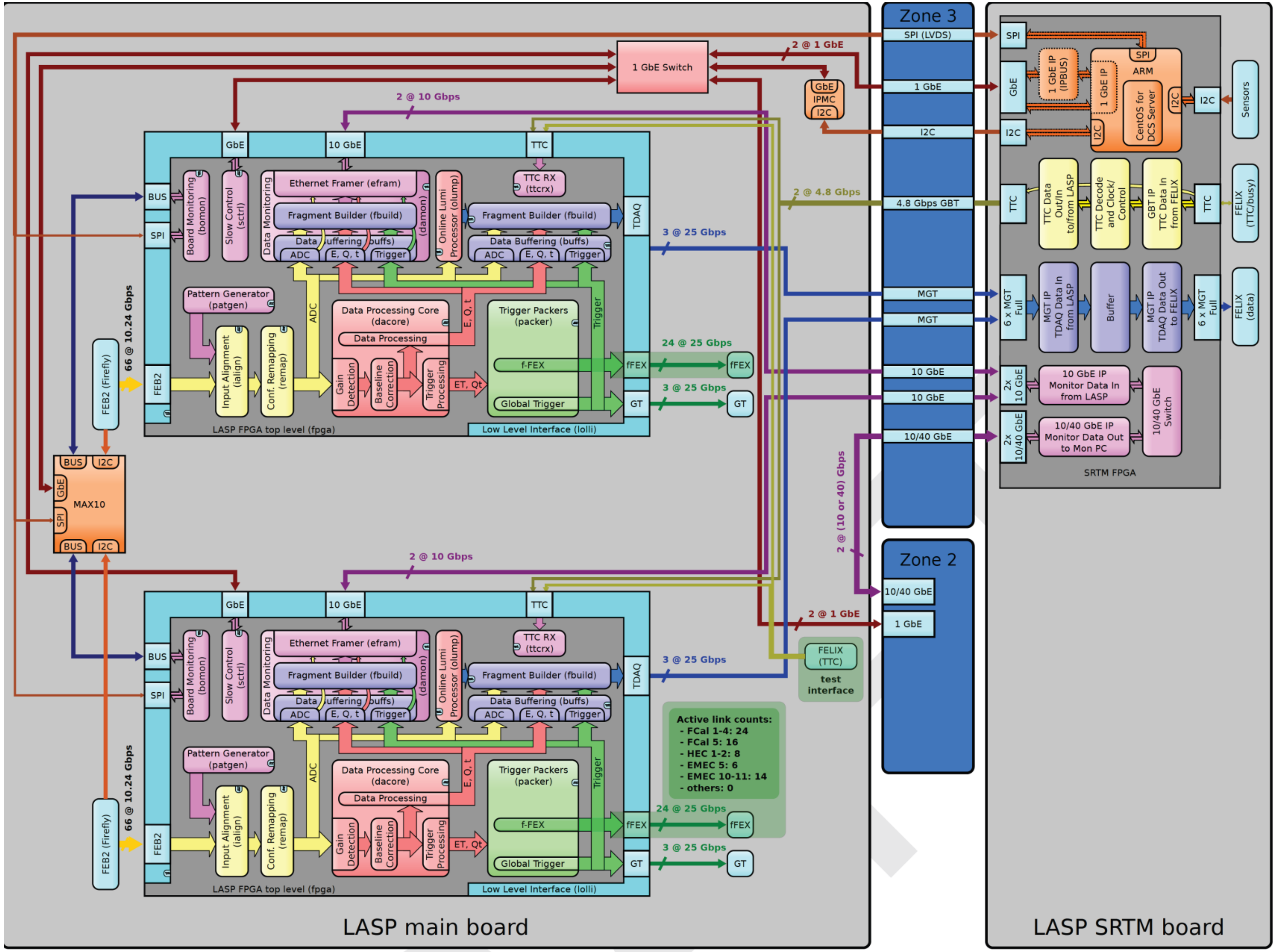




More Information

More Information





LASP main board
LASP SRTM board
Zone 3
Zone 2
1 GbE Switch
2 @ 1 GbE
2 @ 10 Gbps
2 @ 4.8 Gbps
3 @ 25 Gbps
24 @ 25 Gbps
66 @ 10.24 Gbps
2 @ (10 or 40) Gbps
GbE
IPMC
I2C
SPI (LVDS)
1 GbE
4.8 Gbps GBT
MGT
10 GbE
10/40 GbE
GbE
10 GbE
TTC
BUS
SPI
TDAQ
fFEX
GT
FEB2
FEB2 (Firefly)
MAX10
Board Monitoring (bomon)
Slow Control (sctrl)
Data Monitoring (damon)
Ethernet Framer (eframe)
Fragment Builder (fbuild)
Data Buffering (buffs)
ADC
E, Q, t
Trigger
Online Lumi Processor (olump)
TTC RX (ttcrx)
Pattern Generator (patgen)
Input Alignment (ialign)
Conf. Remapping (remap)
Data Processing Core (dacore)
Data Processing
Gain Detection
Baseline Correction
Trigger Processing
ET, Qt
Trigger Packers (packer)
f-FEX
Global Trigger
LASP FPGA top level (fpga)
Low Level Interface (lolli)
FELIX (TTC)
test interface
Active link counts:
- FCal 1-4: 24
- FCal 5: 16
- HEC 1-2: 8
- EMEC 5: 6
- EMEC 10-11: 14
- others: 0
SPI
1 GbE IP (IPBUS)
1 GbE IP
ARM
CentOS for DCS Server
I2C
Sensors
TTC Data Out/In to/from LASP
TTC Decode and Clock/ Control
GBT IP TTC Data In from FELIX
FELIX (TTC/busy)
6 x MGT Full
MGT IP TDAQ Data In from LASP
Buffer
MGT IP TDAQ Data Out to FELIX
FELIX (data)
2x 10 GbE
10 GbE IP Monitor Data In from LASP
2x 10/40 GbE
10/40 GbE IP Monitor Data Out to Mon PC
10/40 GbE Switch
SRTM FPGA