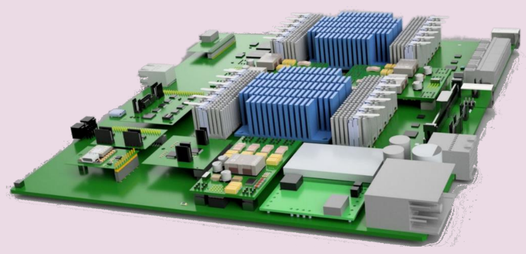
ATLAS Trigger and Data Acquisition Upgrades for the High-Luminosity LHC

Nuno dos Santos Fernandes on behalf of the ATLAS Collaboration
(nuno.dos.santos.fernandes@cern.ch)

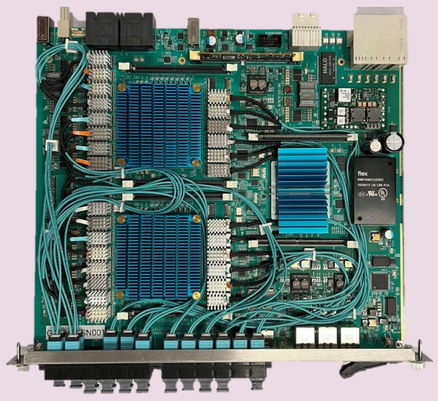
L0Calo

- Coarse calorimeter reconstruction
- Four components: **e**lectron (e, γ, τ), **j**et (τ, jets and E_T^{miss}), **g**lobal (large-R jets and E_T^{miss}) and **f**orward **F**eature **EX**tractors.
- eFEX, jFEX and gFEX inherited from Phase I with firmware upgrades
  - eFEX needs extensive firmware changes
- fFEX will be a new addition, covering $|\eta| > 2.5$ for EM and $|\eta| > 3.3$ for jet triggers
  - Hardware design under development



Global Trigger

- Firmware-based implementation of more complex algorithms based on L0Calo, L0Muon and higher granularity calorimeter information
- Reconstructs clusters, e/γ, τ, jets, E_T^{miss} and topological quantities
- Three parts: **MU**ltiple**X**ers, **G**lobal **E**vent **P**rocessors and a CTP interface, all based on the **G**lobal **C**ommon **M**odule (GCM)
- GCM v2b allowed successful tests of MUX → GEP, GCM v3 expected this year



- Algorithm development well on the way (topological clustering, anti-kT jets and E_T^{miss} demonstrated)

Data Handlers

- Receive data from FELIX and potentially perform detector-dependent processing
- Current prototype is the Phase I **s**oft**w**are **R**ead**O**ut **D**river (SWROD)
- Prototype tested with 1 MHz Level 0 rate

Dataflow

- Buffers, transports and builds event data from Readout to the Event Filter
- Formats, aggregates, compresses and buffers accepted event data from the Event Filter to permanent storage
- Prototype software supports expected rate
- Simulation studies under way to optimize network and buffer usage
- Actively monitoring existing and new technologies, for network and storage

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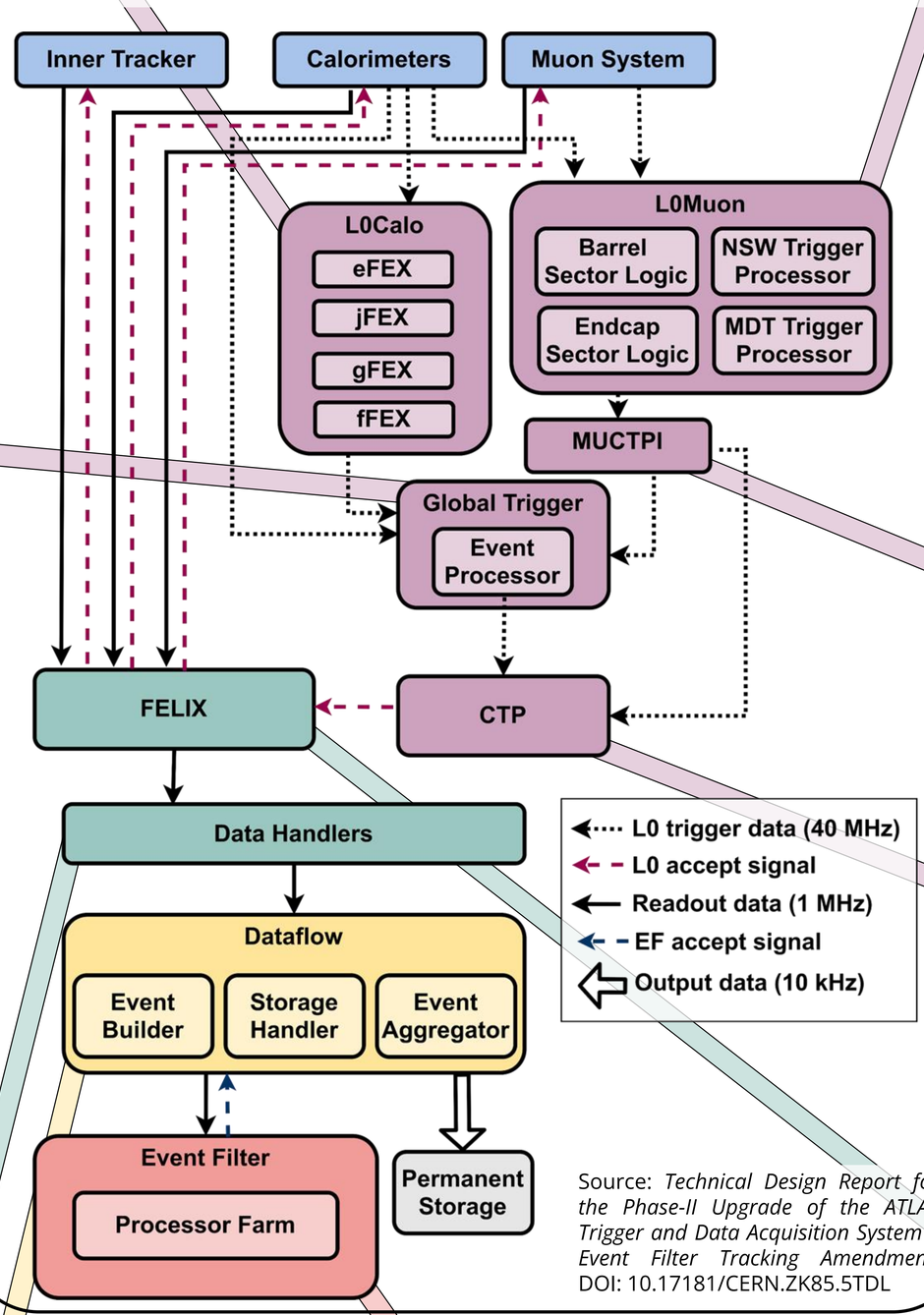
ATLAS Phase II Trigger

Set of upgrades to ATLAS TDAQ to handle the increased luminosity and pile-up and new detectors, focusing on four areas:

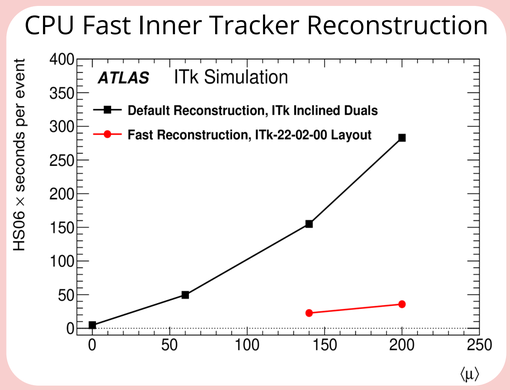
- Level 0: low-latency boards with FPGAs for coarse reconstruction
- Readout: interface between detector I/O and Dataflow
- Dataflow: event data management for Event Filter and persistent storage
- Event Filter : software-based event reconstruction and selection



Source: *Technical Design Report for the Phase-II Upgrade of the ATLAS Trigger and Data Acquisition System – Event Filter Tracking Amendment*, DOI: 10.17181/CERN.ZK85.5TDL

Event Filter

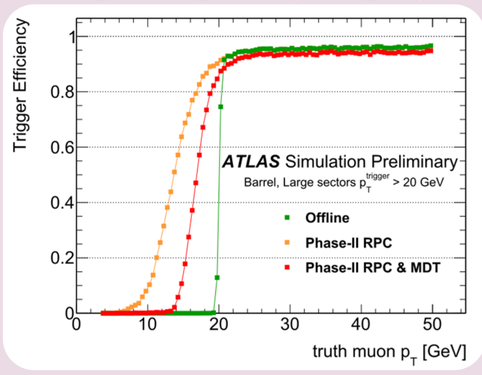
- Near offline quality software-based event reconstruction, classification and event selection, to reduce the 1 MHz input rate to 10 kHz for offline storage and analysis
- Significant R&D efforts in hardware acceleration, decision due 2025



- Major focus on track reconstruction with **I**nner **T**rac**K**er (ITK):
  - Integration with ACTS (**A** **C**ommon **T**racking **S**oftware)
  - Neural networks for extrapolation in hit pattern recognition, finding track candidates, and more.
  - Studies of GPU and FPGA acceleration well under way
    - GPU clustering, seeding and track parameter estimation show preliminary speed-ups of up to 5 at ⟨μ⟩ = 200 (run 4)
    - Several promising FPGA projects: Hough transforms, neural networks, track fitting.
- Muon reconstruction has two main areas of development:
  - Development of machine-learning based algorithms for the NSW, with GPU- and FPGA-accelerated implementations
  - Coordinating efforts with tracking to migrate to ACTS

L0Muon

- Identifies muon candidates
- Four processors:
  - **N**ew **S**mall **W**heels **T**rigger **P**rocessor
  - **M**onitored **D**rift **T**ubes **T**rigger **P**rocessor
  - Barrel and Endcap Sector Logic
- Design of the second prototype for a common platform for Sector Logic started
- Firmware validation well under way
- MDT TP prototype under test, firmware implementation going well
- NSW TP prototype design in progress



MUCTPI

- **MU**on-**CTP** **I**nterface
- Reuses Phase I hardware, but with an additional board and improved firmware
- Firmware studies and the capture of requirements and specifications ongoing

CTP

- **C**entral **T**rigger **P**rocessor
- Makes the final accept/reject decision based on the other parts of the Level 0 and distributes it to the rest of the trigger
- The number of possible triggers will be doubled from Phase I, from 512 to 1024
- Preliminary design in progress

FELIX

- **F**ront-**E**nd **LI**nk e**X**change
- Custom PCIe card to interface detector readouts and commodity DAQ network
- Already saw partial use for Phase I
- New FLX-182 card prototype produced, tests ongoing, with promising results
- Phase II firmware already available, with more improvements coming

- Calorimeter reconstruction also progressing:
  - GPU-accelerated topological clustering mostly integrated within the software framework
    - First version had speed-ups ~3.5 for di-jets at ⟨μ⟩ = 20 and ~5.5 for tt̄ at ⟨μ⟩ = 80 (run 3)
    - Latest speed-ups ~12 for tt̄ at ⟨μ⟩ = 80 (run 3) and ~6 for di-jets at ⟨μ⟩ = 200 (run 4)
  - FPGA acceleration studies have started
  - Machine learning algorithms being developed